SN5440, SN54LS40, SN54S40 SN7440, SN74LS40, SN74S40 DUAL 4-INPUT POSITIVE-NAND BUFFERS SDLS108A – APRIL 1985 – REVISED OCTOBER 2004

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

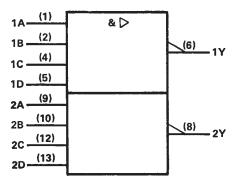
These devices contain two independent 4-input NAND buffer gates.

The SN5440, SN54LS40, and SN54S40 are characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN7440, SN74LS40, and SN74S40 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

	INP	UTS		OUTPUT
A	В	С	D	Y
н	н	н	н	L
L	X	х	X	н
X	L	х	X	н
x	х	L	x	н
X	х	х	L	н

logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

SN5440 . . . J PACKAGE SN54LS40, SN54S40 . . . J OR W PACKAGE SN7440 . . . N PACKAGE SN74LS40, SN74S40 . . . D OR N PACKAGE

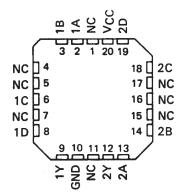
(TOP VIEW)

1A [1 1B [2 NC [3 1C [4 1D [5	14 VCC 13 2D 12 2C 11 NC 10 2B
	10 2B
	9]]2A 8[]2Y

SN5440	W	PACKAGE
(TOP	VIE	W)

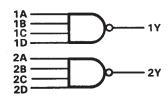
	T T T	
	$\bigcup 14$	1D
1Y [2	13	<u>ן 1C</u>
	12] 1B
/cc ◘₄	11	
	10] 2Y
2A 🛛 6	9] 2D
2B [7	8] 2C

SN54LS40, SN54S40 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

logic diagram



positive logic

 $Y = \overline{A \cdot B \cdot C \cdot D} \text{ or } Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



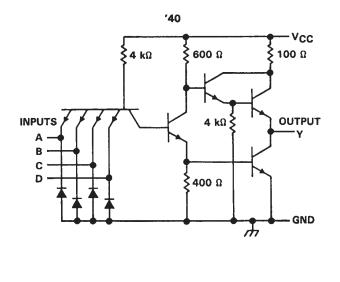
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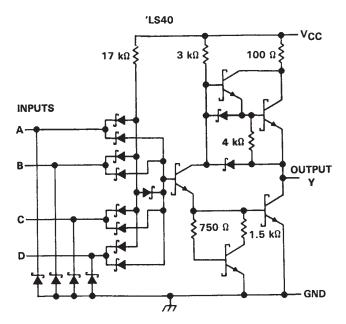
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SN5440, SN54LS40, SN54S40 SN7440, SN74LS40, SN74S40 DUAL 4-INPUT POSITIVE-NAND BUFFERS

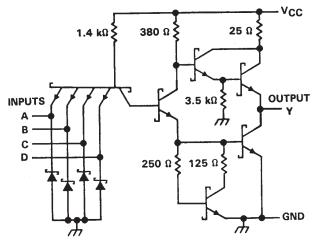
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schematics (each gate)









Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)		
Input voltage: '40, 'S40 'LS40		
Operating free-air temperature range:	SN54'	–55°C to 125°C

NOTE 1: Voltage values are with respect to network ground terminal.



SN5440, SN54LS40, SN54S40 SN7440, SN74LS40, SN74S40 **DUAL 4-INPUT POSITIVE-NAND BUFFERS**

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recommended operating conditions

			SN5440			SN7440			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.8			0.8	V	
юн	High-level output current			- 1.2			- 1.2	mA	
IOL	Low-level output current			48			48	mA	
Τ _A	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]			SN5440			SN7440			
PARAMETER			MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT	
Viк	V _{CC} = MIN,	l _l = – 12 mA				- 1.5			- 1.5	V
VOH	V _{CC} = MIN,	V _{1L} = 0.8 V,	l _{OH} = 1.2 mA	2.4	3.3		2.4	3.3		V
VOL	V _{CC} = MIN,	V _{IH} = 2 V,	IOL = 48 mA		0.2	0.4		0.2	0.4	V
١	V _{CC} = MAX,	V _I = 5.5 V				1			1	mA
Чн	V _{CC} = MAX,	VI = 2.4 V				40			40	μA
ΠL	V _{CC} = MAX,	V _I = 0.4 V				- 1.6			- 1.6	mA
IOS §	V _{CC} = MAX			- 20		- 70	- 18		- 70	mA
ICCH	V _{CC} = MAX,	V1 = 0			4	8		4	8	mA
ICCL	V _{CC} = MAX,	V ₁ = 4.5 V			17	27		17	27	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$. § Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed 100 milliseconds.

switching characteristics, $V_{CC} = 5 V$, $T_A = 25^{\circ}C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONI	MIN TYP	MAX	UNIT	
^t PLH	A 614	~	P. = 122 O	C. = 15 = 5	13	22	ពន
^t PHL	Any	T	R _L = 133 Ω,	C _L = 15 pF	8	15	ns



SN5440, SN54LS40, SN54S40 SN7440, SN74LS40, SN74S40 **DUAL 4-INPUT POSITIVE-NAND BUFFERS**

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recommended operating conditions

		S	SN54LS40			SN74LS40			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
V _{CC} S	upply voltage	4.5	5	5.5	4.75	5	5.25	V	
	ligh-level input voltage	2			2			V	
	ow-level input voltage			0.7			08	V	
	ligh-level output current			- 1.2			- 1.2	mA	
	ow-level output current			12			24	mA	
	perating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			s	10	S	UNIT				
PARAMETER		TEST CONDITIONS T		MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIK	V _{CC} = MIN,	l _l = – 18 mA				- 1.5			- 1.5	V
VOH	V _{CC} = MIN,	VIL = MAX,	I _{OH} = - 1.2 mA	2.5	3.4		2.7	3.4		V
VOL	V _{CC} = MIN,	V _{IH} = 2 V,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	v
	V _{CC} = MIN,	V _{IH} = 2 V,	loL = 24 mA					0.35	0.5	
li I	V _{CC} = MAX,	V _I = 7 V				0.1			0.1	mA
Чн	V _{CC} = MAX,	V _I = 2.7 V				20			20	μA
μ	V _{CC} = MAX,	V _I = 0.4 V	<u> </u>			- 0.4			- 0.4	mA
IOS §	V _{CC} = MAX			- 30		- 130	- 30		- 130	mA
ІССН	V _{CC} = MAX,	V = 0			0.45	1		0.45	1	mA
ICCL	V _{CC} = MAX,	V ₁ = 4.5 V			3	6		3	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$. §Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, $T_A = 25^{\circ}C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS			ТҮР	MAX	UNIT
^t PLH	A.0.4	v	$P_{1} = 667 \Omega$	$C_1 = 45 \text{ pE}$		12	24	ns
^t PHL	Any	1	R _L = 667 Ω,	C _L = 45 pF		12	24	ns



SN5440, SN54LS40, SN54S40 SN7440, SN74LS40, SN74S40 DUAL 4-INPUT POSITIVE-NAND BUFFERS SDLS108A – APRIL 1985 – REVISED OCTOBER 2004

recommended operating conditions

[SN54S40			SN74S40			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.8			0.8	V	
юн	High-level output current			- 3			- 3	mA	
IOL	Low-level output current			60			60	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			SN54S40		SN74S40			UNIT		
	TEST CONDITIONS T			MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIK	V _{CC} = MIN,	l _l = 18 mA				- 1.2			- 1.2	V
VOH	V _{CC} = MIN,	VIL = 0.8 V,	1 _{OH} = - 3 mA	2.5	3.4		2.7	3.4		V
VOL	V _{CC} = MIN,	V _{IH} = 2 V,	I _{OL} = 60 mA			0.5			0.5	V
1	V _{CC} = MAX,	V _I = 5.5 V				1			1	mA
Чн	V _{CC} = MAX,	V ₁ = 2.7 V				0.1			0.1	mA
յլ	V _{CC} = MAX,	V _I = 0.5 V				- 4			- 4	mA
los§	V _{CC} = MAX			- 50		- 225	- 50		- 225	mA
1ссн	V _{CC} = MAX,	V _I = 0			10	18		10	18	mA
ICCL	V _{CC} = MAX,	V ₁ = 4.5 V			25	44		25	44	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$. § Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed 100 milliseconds.

switching characteristics, V_{CC} = 5 V, T_A = 25° C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CON	ΜΙΝ ΤΥΡ	MAX	UNIT	
^t PLH			RL = 93 Ω,	C1 = 50 pF	4	6.5	ns
^t ₽HL	Апу	Y	nL - 93 44,	C[-50pr	4	6.5	ns
^t PLH			R _L = 93 Ω,	C _L = 150 pF	6		ns
^t PHL					6		ns



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN5440J	OBSOLETE	CDIP	J	14	TBD	Call TI	Call TI
SN7440N	OBSOLETE	PDIP	Ν	14	TBD	Call TI	Call TI
SN74LS40N	OBSOLETE	PDIP	Ν	14	TBD	Call TI	Call TI
SN74S40D	OBSOLETE	SOIC	D	14	TBD	Call TI	Call TI
SN74S40N	OBSOLETE	PDIP	Ν	14	TBD	Call TI	Call TI
SNJ5440J	OBSOLETE	CDIP	J	14	TBD	Call TI	Call TI
SNJ5440W	OBSOLETE	CFP	W	14	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AB.



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