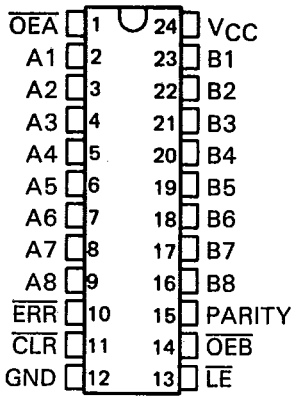
# SN74ALS29853, SN74ALS29854
# 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

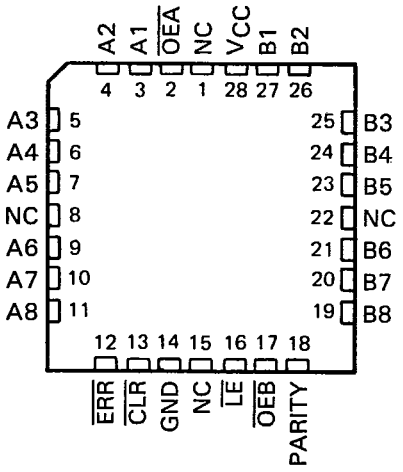
D2990, FEBRUARY 1987

- **Functionally Similar to AMD AM29853 and AM29854**
- **High-Speed Bus Transceivers with Parity Generator/Checker**
- **Parity Error Flag with Open-Collector Outputs**
- **Choice of True ('ALS29853) or Inverting ('ALS29854) Logic**
- **Has a Latch for Storage of the Parity Error Flag**
- **Package Options Include Plastic "Small Outline" Package, Plastic Chip Carriers, and Standard Plastic 300-mil Dips**
- **Dependabale Texas Instruments Quality and Reliability**

**SN74ALS' . . . DW OR NT PACKAGE**
**(TOP VIEW)**




**SN74ALS' . . . FN PACKAGE**
**(TOP VIEW)**




NC—No internal connection

## description

The SN74ALS29853 and SN74ALS29854 are 8-bit to 9-bit parity transceivers designed for two-way communication between data buses. When data is transmitted from the A to B bus a parity bit is generated. When data is transmitted from the B to A bus with its corresponding parity bit, the $\overline{ERR}$ output will indicate whether or not an error in the B data has occurred. The output enable inputs $\overline{OEA}$ and $\overline{OEB}$ can be used to disable the device so that the buses are effectively isolated.

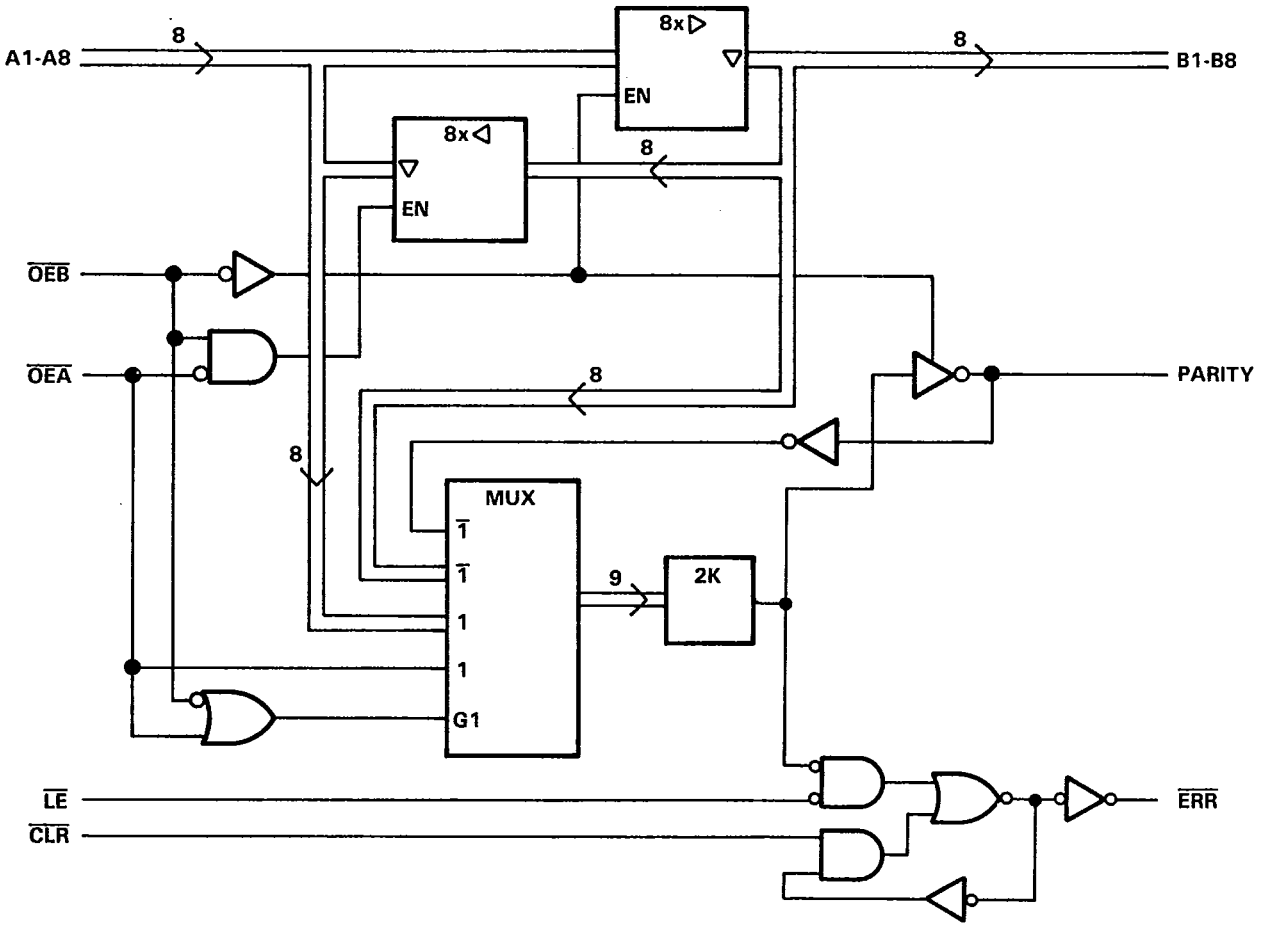
A 9-bit parity generator/checker generates a parity-odd output (PARITY), and monitors the parity of the I/O ports with an open-collector parity error flag ($\overline{ERR}$). $\overline{ERR}$ can be either passed, sampled, stored, or cleared from the latch using the $\overline{EN}$ and $\overline{CLR}$ control inputs. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition which gives the designer more system diagnostic capability.

The SN74ALS29853 and SN74ALS29854 are characterized for operation from 0°C to 70°C.

# SN74ALS29853
# 8-BIT TO 9-BIT PARITY BUS TRANSCEIVER



## logic diagram (positive logic)




## FUNCTION TABLE

| INPUTS | | | | | | OUTPUT & I/O | | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{OEB}$ | $\overline{OEA}$ | $\overline{CLR}$ | $\overline{LE}$ | Ai $\Sigma$ of H's | Bi† $\Sigma$ of H's | A | B | PARITY | $\overline{ERR}$ | |
| L | H | X | X | Odd<br>Even | NA | NA | A | L<br>H | NA | A Data to B Bus and Generate Parity |
| H | L | X | L | NA | Odd<br>Even | B | NA | NA | H<br>L | B Data to A Bus and Check Parity |
| H | L | H | H | NA | X | X | NA | NA | N-1 | Store Error Flag |
| X | X | L | H | X | X | X | NA | NA | H | Clear Error Flag Register |
| H | H | H<br>L<br>X<br>X | H<br>H<br>L<br>L | X<br>X<br>L Odd<br>H Even | X | Z | Z | Z | NC<br>H<br>H<br>L | Isolation‡ (Parity Check) |
| L | L | X | X | Odd<br>Even | NA | NA | A | H<br>L | NA | A Data to B Bus and Generate Inverted Parity |

NA = Not applicable, NC = No change, X = Don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ In this mode the $\overline{ERR}$ output, when enabled, shows inverted parity of the A bus.



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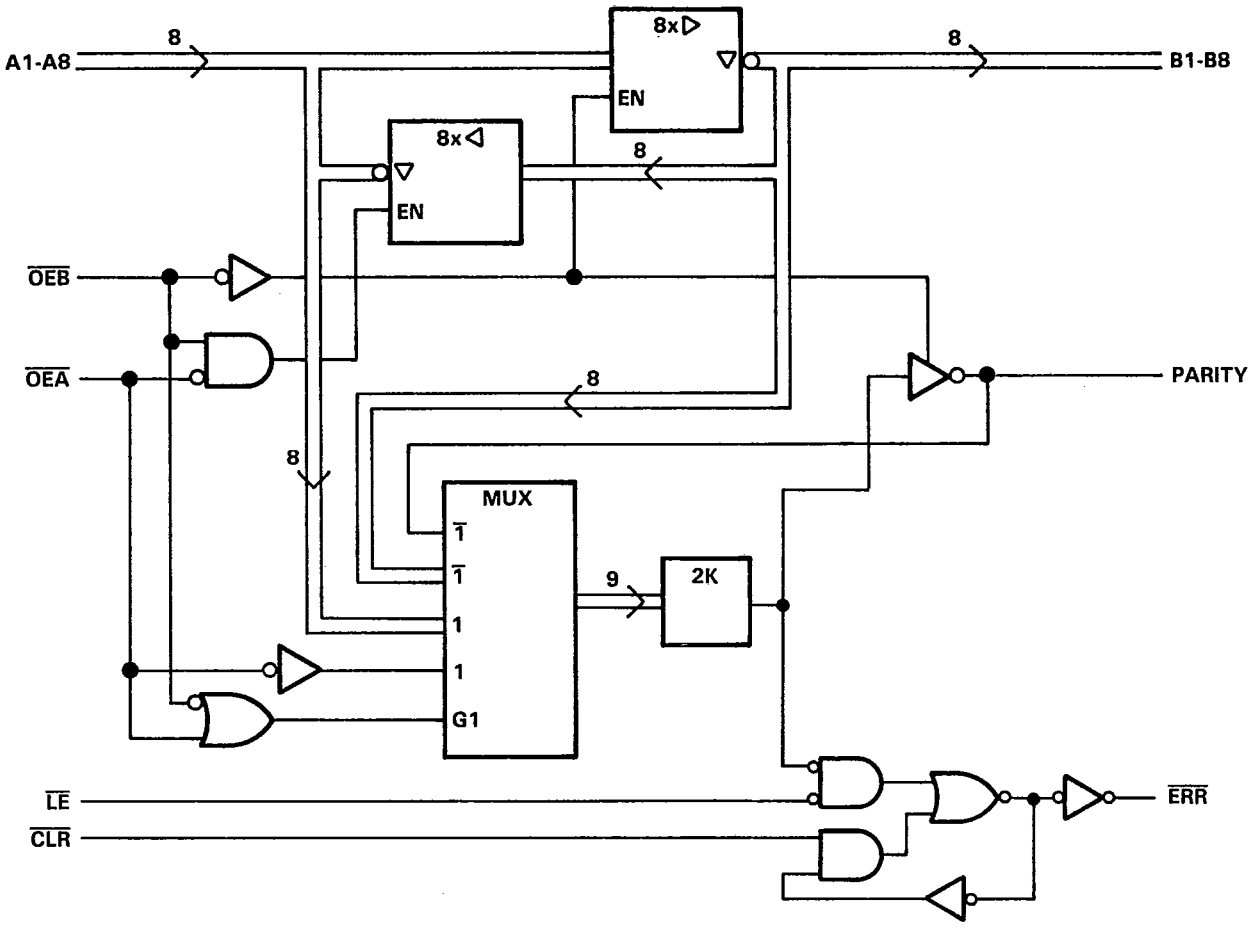
## logic diagram (positive logic)

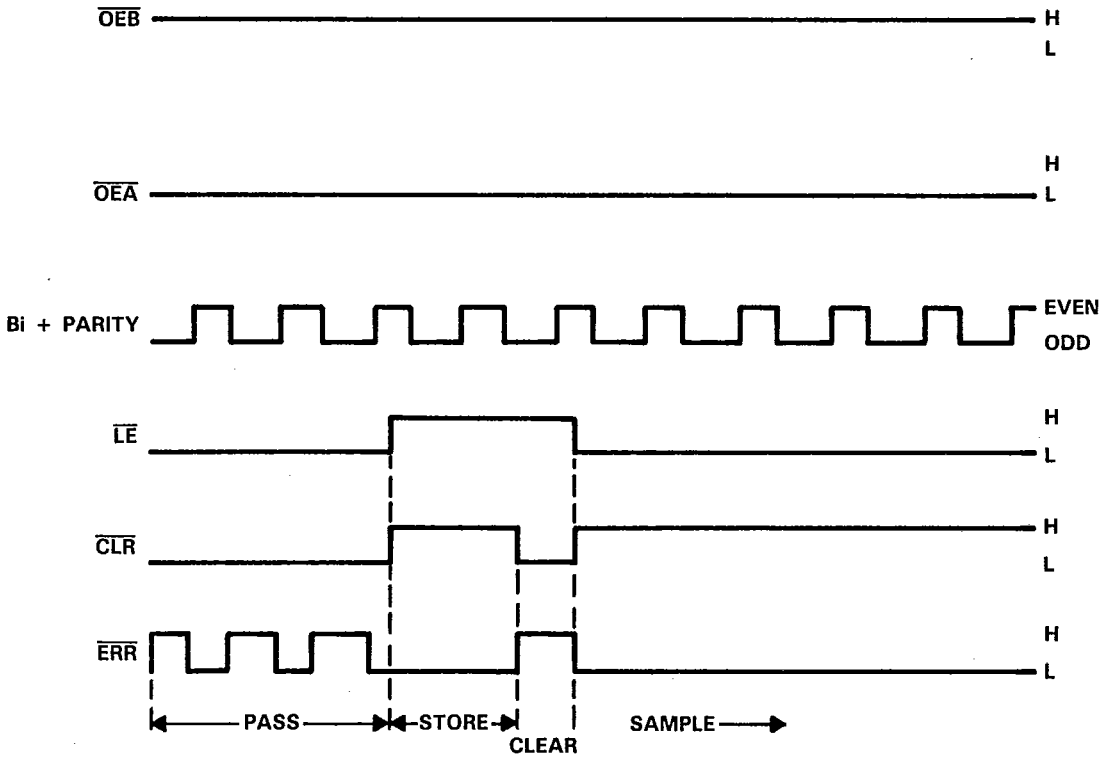



## FUNCTION TABLE

| INPUTS | | | | | | OUTPUT & I/O | | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{OEB}$ | $\overline{OEA}$ | $\overline{CLR}$ | $\overline{LE}$ | Ai<br>$\sum$ of H's | Bi† <br>$\sum$ of L's | A | B | PARITY | $\overline{ERR}$‡ | |
| L | H | X | X | Odd<br>Even | NA | NA | $\overline{A}$ | H<br>L | NA | $\overline{A}$ Data to B Bus and Generate Parity |
| H | L | X | L | NA | Odd<br>Even | $\overline{B}$ | NA | NA | H<br>L | $\overline{B}$ Data to A Bus and Check Parity |
| H | L | H | H | NA | X | X | NA | NA | N-1 | Store Error Flag |
| X | X | L | H | X | X | X | NA | NA | H | Clear Error Flag Register |
| H | H | H<br>L<br>X<br>X | H<br>H<br>L<br>L | X<br>X<br>L Odd<br>H Even | X | Z | Z | Z | NC<br>H<br>L<br>H | Isolation§ |
| L | L | X | X | Odd<br>Even | NA | NA | $\overline{A}$ | L<br>H | NA | $\overline{A}$ Data to B Bus and Generate Inverted Parity |

NA = Not applicable, NC = No change, X = Don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output state assumes a high output pre-state.
§ In this mode the $\overline{ERR}$ output, when enabled, shows noninverted parity of the A bus.

**error flag waveforms**




**ERROR FLAG FUNCTION TABLE**

| INPUTS | | INTERNAL TO DEVICE | OUTPUT PRE-STATE | OUTPUT | FUNCTION |
|---|---|---|---|---|---|
| $\overline{LE}$ | $\overline{CLR}$ | POINT "P" | $\overline{ERR}_{n-1}$† | $\overline{ERR}$ | |
| L | L | L<br>H | X | L<br>H | PASS |
| L | H | L<br>X<br>H | X<br>L<br>H | L<br>L<br>H | SAMPLE |
| H | L | X | X | H | CLEAR |
| H | H | X | L<br>H | L<br>H | STORE |

†ERRn-1 represents the state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, $\overline{LE}$ or point P.



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled I/O port . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

## recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage, $\overline{ERR}$ | | | | 5.5 | V |
| $I_{OH}$ | High-level output current | | | | −24 | mA |
| $I_{OL}$ | Low-level output current | | | | 48 | mA |
| $t_w$ | Pulse duration | $\overline{LE}$ high | 10 | | | ns |
| | | $\overline{LE}$ low | 10 | | | |
| | | $\overline{CLR}$ low | 10 | | | |
| $t_{su}$ | Setup time before $\overline{LE}$↓ | Bi and PARITY | 15 | | | ns |
| | | $\overline{CLR}$ high | 15 | | | |
| $t_h$ | Hold time, Bi and PARITY after $\overline{LE}$↓ | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.75 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | All inputs/outputs except $\overline{ERR}$ | $V_{CC}$ = 4.75 V | $I_{OH}$ = −15 mA | 2.4 | | | V |
| | | | $I_{OH}$ = −24 mA | 2 | | | |
| $I_{OH}$ | $\overline{ERR}$ | $V_{CC}$ = 4.75 V, | $V_{OH}$ = 5.5 V | | | 0.1 | mA |
| $V_{OL}$ | | $V_{CC}$ = 4.75 V, | $I_{OL}$ = 48 mA | | 0.35 | 0.5 | V |
| $I_I$ | | $V_{CC}$ = 5.25 V, | $V_I$ = 5.5 V | | | 0.1 | mA |
| $I_{IH}$‡ | | $V_{CC}$ = 5.25 V, | $V_I$ = 2.7 V | | | 20 | μA |
| $I_{IL}$‡ | Data | $V_{CC}$ = 5.25 V, | $V_I$ = 0.4 V | | | −0.2 | mA |
| | Control | | | | | −0.75 | |
| $I_O$§ | | $V_{CC}$ = 5.25 V, | $V_O$ = 0 | −75 | | −250 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.25 V, | All outputs open | | 70 | 100 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ These parameters include off-state output current for I/O ports only.
§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | $V_{CC}$ = 4.75 V to 5.25 V, $T_A$ = MIN to MAX | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | $C_L$ = 50 pF | | 6 | 8 | | 10 | ns |
| $t_{PHL}$ | | | | | 6 | 8 | | 10 | |
| $t_{PLH}$ | | | $C_L$ = 300 pF | | 10 | 13 | | 17 | |
| $t_{PHL}$ | | | | | 10 | 13 | | 17 | |
| $t_{PLH}$ | A | PARITY | $C_L$ = 50 pF | | 11 | 14 | | 18 | ns |
| $t_{PHL}$ | | | | | 11 | 14 | | 18 | |
| $t_{PLH}$ | | | $C_L$ = 300 pF | | 18 | 22 | | 27 | |
| $t_{PHL}$ | | | | | 18 | 22 | | 27 | |
| $t_{PZH}$ | $\overline{OEA}$ or $\overline{OEB}$ | A or B | $C_L$ = 50 pF | | 11 | 15 | | 19 | ns |
| $t_{PZL}$ | | | | | 11 | 15 | | 19 | |
| $t_{PZH}$ | | | $C_L$ = 300 pF | | 24 | 30 | | 35 | |
| $t_{PZL}$ | | | | | 17 | 23 | | 28 | |
| $t_{PHZ}$ | $\overline{OEA}$ or $\overline{OEB}$ | A or B | $C_L$ = 5 pF | | 5 | 8 | | 10 | ns |
| $t_{PLZ}$ | | | | | 5 | 8 | | 10 | |
| $t_{PHZ}$ | | | $C_L$ = 50 pF | | 9 | 12 | | 15 | |
| $t_{PLZ}$ | | | | | 4 | 8 | | 10 | |
| $t_{PHL}$ | $\overline{LE}$ | $\overline{ERR}$ | $C_L$ = 50 pF | | 5 | 10 | | 12 | ns |
| $t_{PLH}$ | $\overline{CLR}$ | $\overline{ERR}$ | $C_L$ = 50 pF | | 17 | 21 | | 26 | ns |
| $t_{PLH}$ | $\overline{OEA}$ | PARITY | $C_L$ = 50 pF | | 12 | 15 | | 19 | ns |
| $t_{PHL}$ | | | | | 11 | 15 | | 19 | |
| $t_{PLH}$ | | | $C_L$ = 300 pF | | 16 | 22 | | 25 | |
| $t_{PHL}$ | | | | | 16 | 22 | | 25 | |
| $t_{PLH}$ | Bi/PARITY | $\overline{ERR}$ | $C_L$ = 50 pF | | 25 | 34 | | 38 | ns |
| $t_{PHL}$ | | | | | 12 | 18 | | 21 | |



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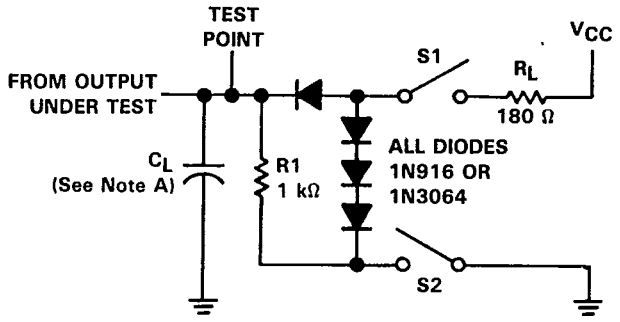
## switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | $V_{CC}$ = 4.75 V to 5.25 V, $T_A$ = MIN to MAX | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | $C_L$ = 50 pF | | 3 | 6 | | 8 | ns |
| $t_{PHL}$ | | | | | 3 | 6 | | 8 | |
| $t_{PLH}$ | | | $C_L$ = 300 pF | | 10 | 13 | | 15 | |
| $t_{PHL}$ | | | | | 7 | 11 | | 13 | |
| $t_{PLH}$ | A | PARITY | $C_L$ = 50 pF | | 12 | 15 | | 19 | ns |
| $t_{PHL}$ | | | | | 10 | 13 | | 15 | |
| $t_{PLH}$ | | | $C_L$ = 300 pF | | 18 | 22 | | 25 | |
| $t_{PHL}$ | | | | | 15 | 19 | | 22 | |
| $t_{PZH}$ | $\overline{OEA}$ or $\overline{OEB}$ | A or B | $C_L$ = 50 pF | | 10 | 13 | | 17 | ns |
| $t_{PZL}$ | | | | | 11 | 15 | | 17 | |
| $t_{PZH}$ | | | $C_L$ = 300 pF | | 25 | 33 | | 35 | |
| $t_{PZL}$ | | | | | 25 | 33 | | 35 | |
| $t_{PHZ}$ | $\overline{OEA}$ or $\overline{OEB}$ | A or B | $C_L$ = 5 pF | | 3 | 7 | | 8 | ns |
| $t_{PLZ}$ | | | | | 3 | 7 | | 8 | |
| $t_{PHZ}$ | | | $C_L$ = 50 pF | | 8 | 12 | | 15 | |
| $t_{PLZ}$ | | | | | 3.5 | 6 | | 8 | |
| $t_{PHL}$ | $\overline{LE}$ | $\overline{ERR}$ | $C_L$ = 50 pF | | 6 | 10 | | 12 | ns |
| $t_{PLH}$ | $\overline{CLR}$ | $\overline{ERR}$ | $C_L$ = 50 pF | | 13 | 17 | | 20 | ns |
| $t_{PLH}$ | $\overline{OEA}$ | PARITY | $C_L$ = 50 pF | | 11 | 14 | | 17 | ns |
| $t_{PHL}$ | | | | | 12 | 15 | | 19 | |
| $t_{PLH}$ | | | $C_L$ = 300 pF | | 15 | 19 | | 22 | |
| $t_{PHL}$ | | | | | 19 | 22 | | 25 | |
| $t_{PLH}$ | Bi/PARITY | $\overline{ERR}$ | $C_L$ = 50 pF | | 22 | 30 | | 35 | ns |
| $t_{PHL}$ | | | | | 12 | 18 | | 21 | |

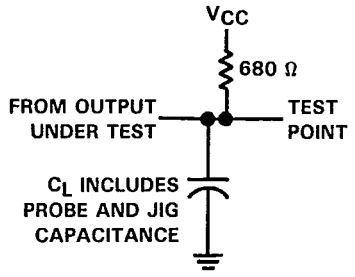
## PARAMETER MEASUREMENT INFORMATION



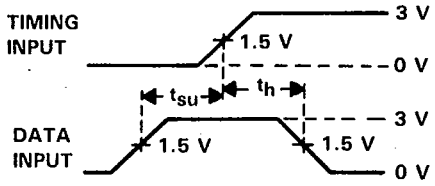

LOAD CIRCUIT 1 ALL OUTPUTS EXCEPT FOR ERROR FLAG

SWITCH POSITION TABLE

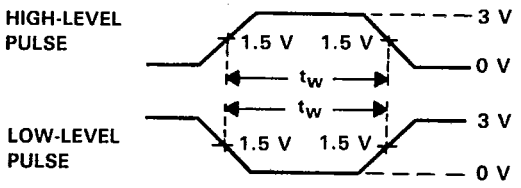
| TEST | S1 | S2 |
|---|---|---|
| $t_{PLH}$ | Closed | Closed |
| $t_{PHL}$ | Closed | Closed |
| $t_{PZH}$ | Open | Closed |
| $t_{PZL}$ | Closed | Open |
| $t_{PHZ}$ | Closed | Closed |
| $t_{PLZ}$ | Closed | Closed |



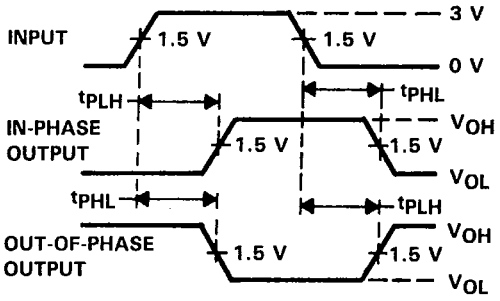

LOAD CIRCUIT 2 ERROR FLAG OUTPUT



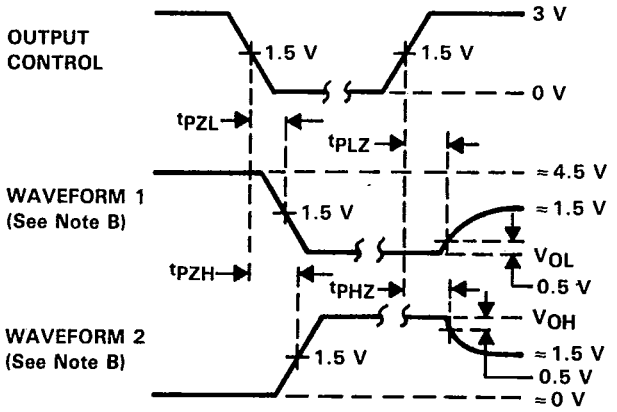

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.