

October 1997

Fast CMOS 16-Bit Registered Transceivers

Features

- Advanced 0.6 micron CMOS Technology
- These Devices Are High-speed, Low Power Devices with High Current Drive
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on All Inputs
- CD74FCT16952T
 - High Output Drive: $I_{OH} = -32mA$; $I_{OL} = 64mA$
 - Power Off Disable Outputs Permit "Live Insertion"
 - Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V, T_A = 25^\circ C$
- CD74FCT162952T
 - Balanced Output Drivers: $\pm 24mA$
 - Reduced System Switching Noise
- Typical V_{OLP} (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V, T_A = 25^\circ C$
- CD74FCT162H952T
 - Bus Hold Retains Last Active Bus State During Three-State
 - Eliminates the Need for External Pull-Up Resistors

Description

These devices are 16-bit registered transceivers organized with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A-to-B, for example, the A-to-B Enable ($\overline{x}CEAB$) input must be LOW in order to enter data from xAX . The data present on the A port will be clocked on the B register when $xCLKAB$ toggles from LOW-to-HIGH. The $\overline{x}OEAB$ control performs the output enable function on the B port. Control of data from B-to-A is similar, but uses the $\overline{x}CEBA$, $xCLKBA$, and $\overline{x}OEBA$ inputs. By connecting the control pins of the two independent transceivers together, a full 16-bit operation can be achieved. The output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT16952T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT162952T has $\pm 24mA$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

The CD74FCT162H952T has "Bus Hold" which retains the input's last state whenever the input goes to high-impedance preventing "floating" inputs and eliminating the need for pull-up/down resistors.

Ordering Information

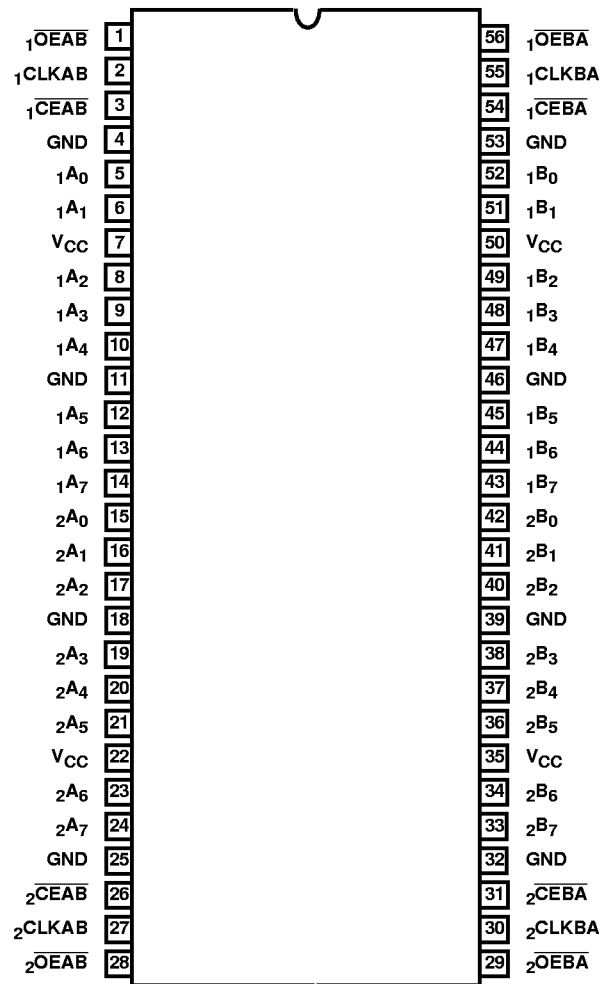
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16952ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16952ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16952CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16952CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16952DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16952DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16952ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16952ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16952TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16952TSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162952ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162952ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162952CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162952CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162952DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162952DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162952ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162952ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FC5162952TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162952TSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H952ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H952ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H952BTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H952BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H952CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H952CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H952DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H952DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H952ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H952ETSM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

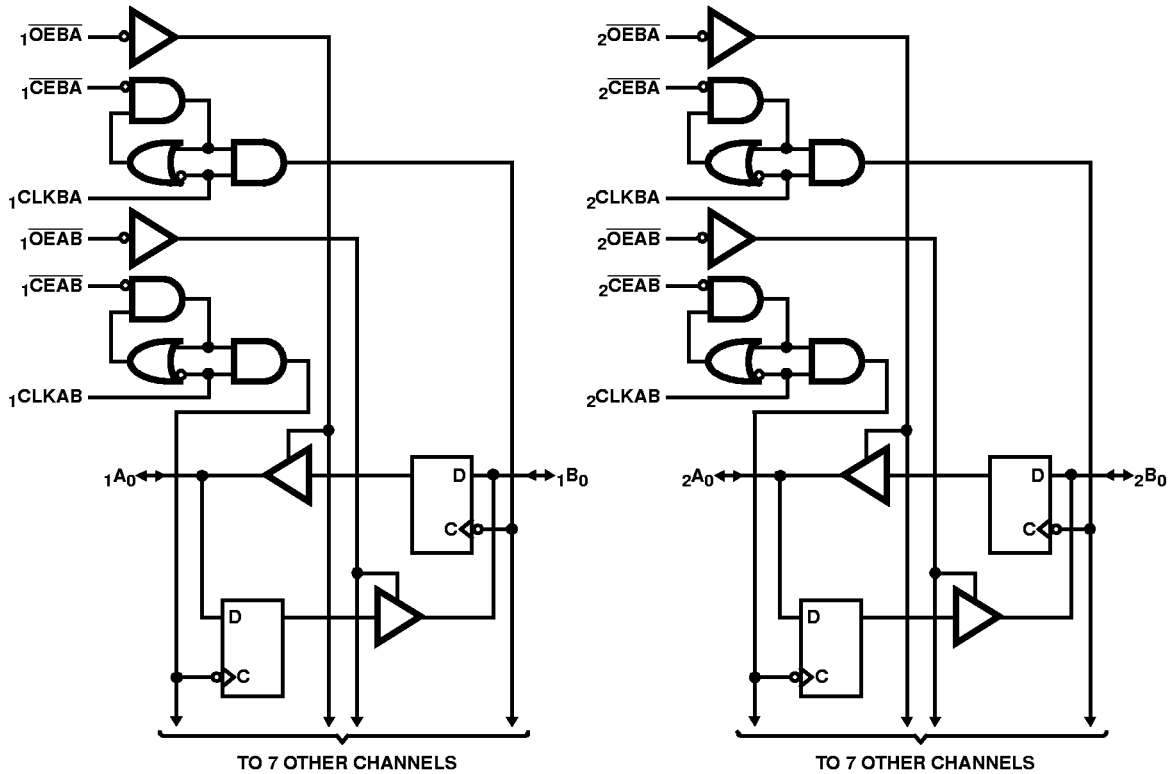
CD74FCT16952T, CD74FCT162952T, CD74FCT162H952T

Pinout

CD74FCT16952T, CD74FCT162952T, CD74FCT162H952T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTES 1, 2)

INPUTS			OUTPUTS	
$\overline{x}CEAB$	$\overline{x}CLKAB$	$\overline{x}OEAB$	xAx	xBx
H	X	L	X	B (Note 3)
X	L	L	X	B (Note 3)
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	High Z

NOTES:

- H = High Voltage Level
L = Low Voltage Level
X = Don't Care or Irrelevant
↑ = LOW-to-HIGH Transition
Z = High Impedance
- A-to-B data flow shown. B-to-A flow control is the same, except using $\overline{x}CEBA$, $\overline{x}CLKBA$, and $\overline{x}OEBA$.
- Level of B before the indicated steady-state input conditions were established.

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{x}OEAB$	A-to-B Output Enable Input (Active LOW)
$\overline{x}OEBA$	B-to-A Output Enable Input (Active LOW)
$\overline{x}CEAB$	A-to-B Clock Enable Input (Active LOW)
$\overline{x}CEBA$	B-to-A Clock Enable Input (Active LOW)
$\overline{x}CLKAB$	A-to-B Clock Input
$\overline{x}CLKBA$	B-to-A Clock Input
xAx	A-to-B Data Inputs or B-to-A Three-State Outputs (Note 4)
xBx	B-to-A Data Inputs or A-to-B Three-State Outputs (Note 4)
GND	Ground
V _{CC}	Power

NOTE:

- For the CD74FCT162H952T, these pins have "Bus Hold". All other pins are standard, outputs, or I/O's.

CD74FCT16952T, CD74FCT162952T, CD74FCT162H952T

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 6) TEST CONDITIONS	MIN	(NOTE 7) TYP	MAX	UNITS	
CD74FCT16952T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V _{OH}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3.0mA	2.5	3.5	-	V
			I _{OH} = -15.0mA	2.4	3.5	-	V
			I _{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I _{OFF}	V _{CC} = 0V, V _{IN} or V _{OUT} ≤ 4.5V	-	-	±100	μA	
CD74FCT162952T, CD74FCT162H952T, OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V _{OH}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I _{ODL}	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V (Note 8)	60	115	150	mA	
Output HIGH Current	I _{ODH}	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V (Note 8)	-60	-115	-150	mA	
CAPACITANCE T _A = 25°C, f = 1MHz							
Input Capacitance (Note 11)	C _{IN}	V _{IN} = 0V	-	4.5	6	pF	
Output Capacitance (Note 11)	C _{OUT}	V _{OUT} = 0V	-	5.5	8	pF	
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I _{CC}	V _{CC} = Max	V _{IN} = GND or V _{CC}	-	0.1	500	μA
Supply Current per Input at TTL HIGH	ΔI _{CC}	V _{CC} = Max	V _{IN} = 3.4V (Note 12)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 13)	I _{CCD}	V _{CC} = Max, Outputs Open x _{OEAB} or x _{OEBA} = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	-	75	120	μA/ MHz
Total Power Supply Current (Note 15)	I _C	V _{CC} = Max, Outputs Open f _{CP} = 10MHz (x _{CLKAB}) 50% Duty Cycle x _{OEAB} = x _{CEAB} = GND x _{CEBA} = V _{CC} One Bit Toggling, f ₁ = 5MHz	V _{IN} = V _{CC} V _{IN} = GND	-	0.8	1.7 (Note 14)	mA
			V _{IN} = 3.4V V _{IN} = GND	-	1.3	3.2 (Note 14)	mA
			V _{IN} = V _{CC} V _{IN} = GND	-	3.8	6.5 (Note 14)	mA
			V _{IN} = 3.4V V _{IN} = GND	-	8.3	20.5 (Note 14)	mA

CD74FCT16952T, CD74FCT162952T, CD74FCT162H952T

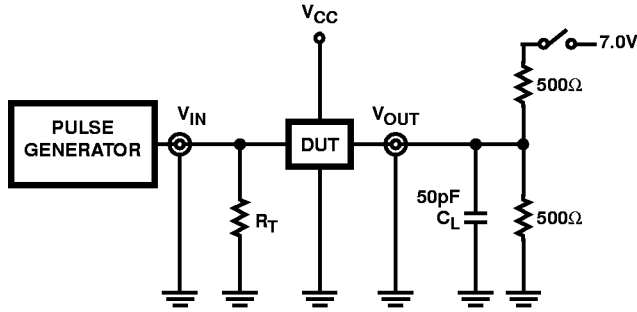
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 16) TEST CONDITIONS	AT		BT		CT		DT		ET		UNITS
			(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	
Propagation Delay $\chi\text{CLKAB}, \chi\text{CLKBA}$ to $\chi\text{Bx}, \chi\text{Ax}$	$t_{\text{PLH}}, t_{\text{PHL}}$	$C_L = 50\text{pF}$ $R_L = 500\Omega$	2.0	10.0	2.0	7.5	2.0	6.3	2.0	4.4	1.5	3.7	ns
Output Enable Time $\chi\overline{\text{OEBA}}, \chi\overline{\text{OEAB}}$ to $\chi\text{Ax}, \chi\text{Bx}$	$t_{\text{PZH}}, t_{\text{PZL}}$		1.5	10.5	1.5	8.0	1.5	7.0	1.5	4.8	1.5	4.4	ns
Output Disable Time (Note 18) $\chi\overline{\text{OEBA}}, \chi\overline{\text{OEAB}}$ to $\chi\text{Ax}, \chi\text{Bx}$	$t_{\text{PHZ}}, t_{\text{PLZ}}$		1.5	10.0	1.5	7.5	1.5	6.5	1.5	4.0	1.5	4.0	ns
Setup Time HIGH or LOW, $\chi\text{Ax}, \chi\text{Bx}$ to $\chi\text{CLKAB}, \chi\text{CLKBA}$	t_{SU}		2.5	-	2.5	-	2.5	-	2.0	-	1.5	-	ns
Hold Time HIGH or LOW, $\chi\text{Ax}, \chi\text{Bx}$ to $\chi\text{CLKAB}, \chi\text{CLKBA}$	t_{H}		2.0	-	2.0	-	1.5	-	1.0	-	0.0	-	ns
Setup Time HIGH or LOW, $\chi\overline{\text{CEAB}}, \chi\overline{\text{CEBA}}$ to $\chi\text{CLKAB}, \chi\text{CLKBA}$	t_{SU}		3.0	-	3.0	-	3.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, $\chi\overline{\text{CEAB}}, \chi\overline{\text{CEBA}}$ to $\chi\text{CLKAB}, \chi\text{CLKBA}$	t_{H}		2.0	-	2.0	-	2.0	-	1.5	-	0.0	-	ns
Pulse Width HIGH (Note 18) or LOW, χCLKAB or χCLKBA	t_{W}		3.0	-	3.0	-	3.0	-	3.0	-	3.0	-	ns
Output Skew (Note 19)	$t_{\text{SK(O)}}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

6. For conditions shown as Max or Min, use appropriate value specified under Electrical Characteristics for the applicable device type.
7. Typical values are at $V_{\text{CC}} = 5.0\text{V}$, 25°C ambient and maximum loading, except as noted.
8. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
9. Pins with Bus Hold are identified in the pin description.
10. This specification does not apply to bi-directional functionalities with Bus Hold.
11. This parameter is determined by device characterization but is not production tested.
12. Per TTL driven input ($V_{\text{IN}} = 3.4\text{V}$); all other inputs at V_{CC} or GND.
13. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
14. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
15. $I_{\text{C}} = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_{\text{C}} = I_{\text{CC}} + \Delta I_{\text{CC}} D_{\text{H}} N_{\text{T}} + I_{\text{CCD}} (f_{\text{CP}}/2 + f_{\text{I}} N_{\text{I}})$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{\text{IN}} = 3.4\text{V}$)
 D_{H} = Duty Cycle for TTL Inputs High
 N_{T} = Number of TTL Inputs at D_{H}
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_{I} = Input Frequency
 N_{I} = Number of Inputs at f_{I}
 All currents are in milliamps and all frequencies are in megahertz.
16. See test circuit and wave forms.
17. Minimum limits are guaranteed but not tested on Propagation Delays.
18. This parameter is guaranteed but not production tested.
19. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION	
TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
$t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.
 R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

20. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_{OUT} \leq 50\Omega$;
 $t_f, t_r \leq 2.5\text{ns}$.

FIGURE 1. TEST CIRCUIT

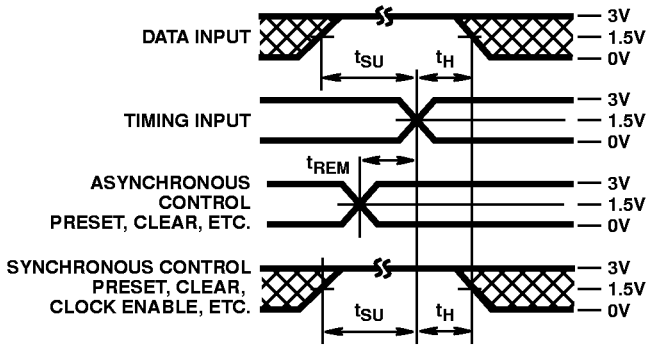


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

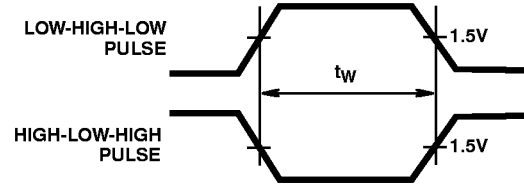


FIGURE 3. PULSE WIDTH

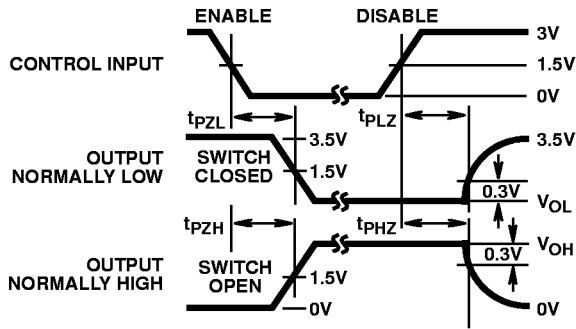


FIGURE 4. ENABLE AND DISABLE TIMING

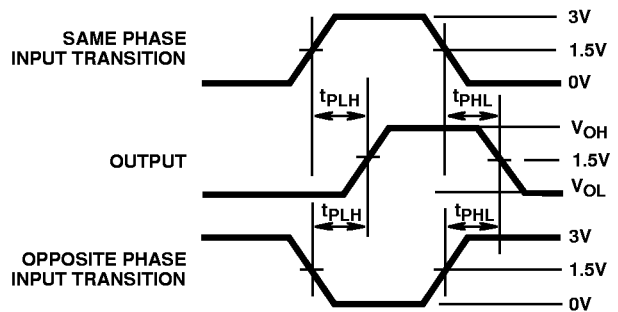


FIGURE 5. PROPAGATION DELAY