

DN74LS73 *DN74LS73*

Dual J-K Flip-Flops (with Reset)

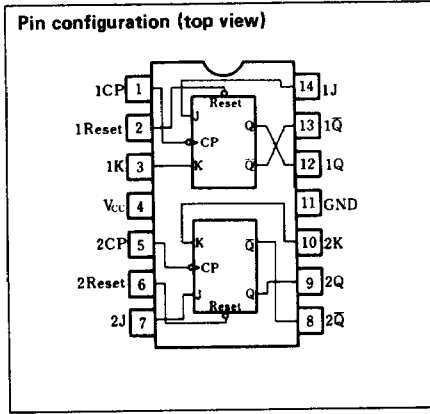
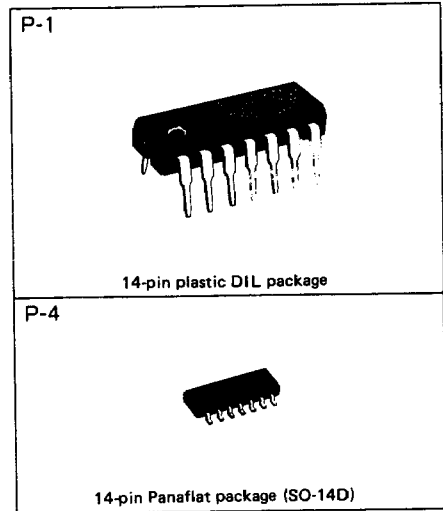
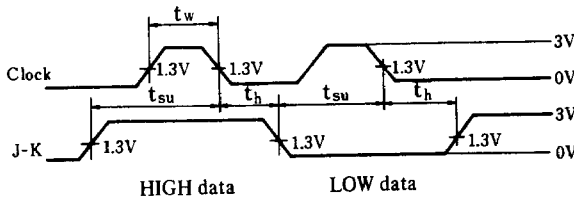
■ Description

DN74LS73 contains two negative-edge triggered J-K flip-flop circuit, each with independent clock CP, J, K, and direct-coupled reset input terminals.

■ Features

- Negative-edge trigger
- Independent input terminals for each flip flop
- Direct-coupled reset input
- Q and \bar{Q} outputs
- Wide operating temperature range ($T_a = -20$ to $+75^\circ\text{C}$)

■ Timing definition



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{cc}	4.75	5.00	5.25	V
Output current	I_{OH}			-400	μA
	I_{OL}			8	mA
Operating temperature range	T_{opr}	-20	25	75	$^\circ\text{C}$
Clock frequency	f_{clock}	0		30	MHz
Pulse width	Clock High		20		ns
	Reset Low	t_w	25		ns
Set-up time	HIGH data	t_{su}	20 ↓		ns
	LOW data	t_{su}	20 ↓		ns
Hold time	t_h	0 ↓			ns

Notes 1. ↓: Indicates fall edge of standard clock pulse.

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■ DC characteristics (Ta = -20 ~ +75 °C)

Parameter		Sym	Test conditions	Min	Typ*	Max	Unit
Input voltage		V _{IH}		2.0			V
		V _{IL}				0.8	V
Output voltage		V _{OH}	V _{CC} =4.75V, V _{IH} =2V V _{IL} =0.8V, I _{OH} =-400 μA	2.7	3.4		V
		V _{OL1}	V _{CC} =4.75V V _{IH} =2V		0.25	0.4	V
		V _{OL2}	V _{IL} =0.8V			0.35	0.5
Input current	J, K	I _{IH}	V _{CC} =5.25V V _I =2.7V			20	μA
	Reset					60	μA
	Clock					80	μA
	J, K	I _{IL}	V _{CC} =5.25V V _I =0.4V			-0.4	mA
	Reset					-0.8	mA
	Clock					-0.8	mA
	J, K	I _I	V _{CC} =5.25V			0.1	mA
	Reset					0.3	mA
	Clock					0.4	mA
Output short circuit current**		I _{OS}	V _{CC} =5.25, V _O =0V	-15		-100	mA
Input clamp voltage		V _{IK}	V _{CC} =4.75V, I _I =-18mA			-1.5	V
Supply current***		I _{CC}	V _{CC} =5.25V		4	8	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

*** Measured with all outputs open, Q and Q̄ outputs alternately HIGH, and clock inputs grounded.

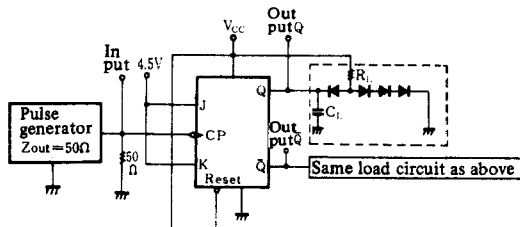
■ Switching characteristics (V_{CC}=5V, Ta=25°C)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit	
Maximum clock frequency	f _{max}			C _L =15pF R _L =2KΩ	30	45		MHz	
Propagation delay time	t _{PLH}	Reset clock	Q, Q̄				11	20	ns
	t _{PHL}						15	30	ns

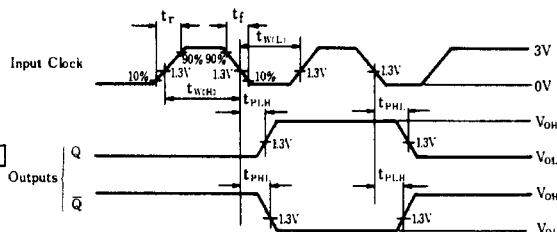
※ Switching parameter measurement information

(1) f_{max}, t_{PLH}, t_{PHL} (Clock → Q, Q̄)

1. Measurement circuit



2. Waveforms

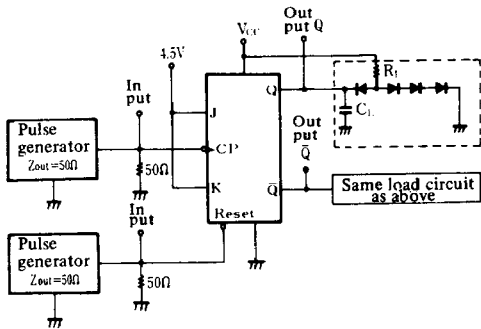


Notes

1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161 or equivalent.
1. Clock input waveform: t_r ≤ 15ns, t_f ≤ 6ns, PRR=1MHz, duty cycle 50%
2. When measuring f_{max}, t_r and t_f ≤ 2.5ns.

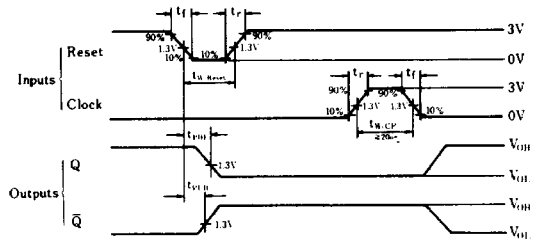
(2) $t_{PHL}(\text{Reset} \rightarrow Q)$, $t_{PLH}(\text{Reset} \rightarrow \bar{Q})$

1. Measurement circuit



1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161 or equivalent.

2. Waveforms



Notes

1. Set and clock waveforms: $t_r \leq 15\text{ns}$, $t_f \leq 6\text{ns}$, $\text{PRR} = 1\text{MHz}$.

■ Truth tables

Inputs				Outputs	
Reset	Clock	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	↓	L	L	Q_0	\bar{Q}_0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_0	\bar{Q}_0

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. ↓: Change from HIGH to LOW.
4. X: Either HIGH or LOW; doesn't matter.
5. Q_0 : Q level prior to determination of input condition shown in table.
6. \bar{Q}_0 : \bar{Q} level prior to determination of input condition shown in table.
7. Toggle: With ↓ change, outputs become compliment of previous condition.

■ Logic diagram (1/2)

