- **Three-State Version of SN54/74LS153, SN54/74S153**

- **Schottky-Diode-Clamped Transistors**

- **Permits Multiplexing from N Lines to 1 Line**

- **Performs Parallel-to-Serial Conversion**

- **Fully Compatible with Most TTL Circuits**

- **Low Power Dissipation**
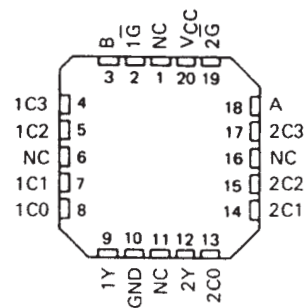   'LS253 . . . 35 mW Typical
    'S253 . . . 225 mW Typical

SN54LS253, SN54S253 . . . J OR W PACKAGE
SN74LS253, SN74S253 . . . D OR N PACKAGE
(TOP VIEW)

$\overline{1G}$	1	16	V_{CC}
B	2	15	$\overline{2G}$
1C3	3	14	A
1C2	4	13	2C3
1C1	5	12	2C2
1C0	6	11	2C1
1Y	7	10	2C0
GND	8	9	2Y
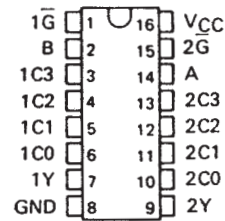
SN54LS253, SN54S253 . . . FK PACKAGE
(TOP VIEW)

NC-No internal connection

description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage: 'LS253 . . . . 7 V
             'S253 . . . . 5.5 V
Off-state output voltage . . . . 5.5 V
Operating free-air temperature range: SN54LS253, SN54S253 . . . . – 55°C to 125°C
                                 SN74LS253, SN74S253 . . . . 0°C to 70°C
Storage temperature range . . . . – 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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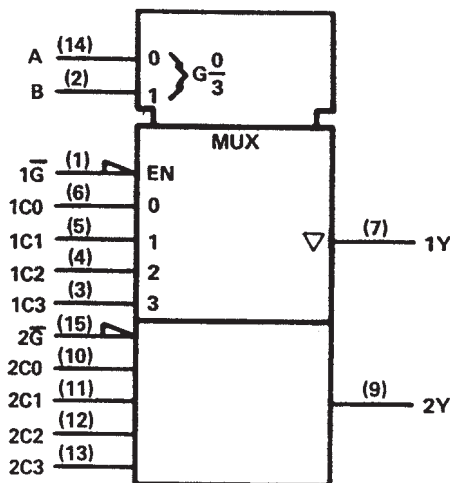
logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)
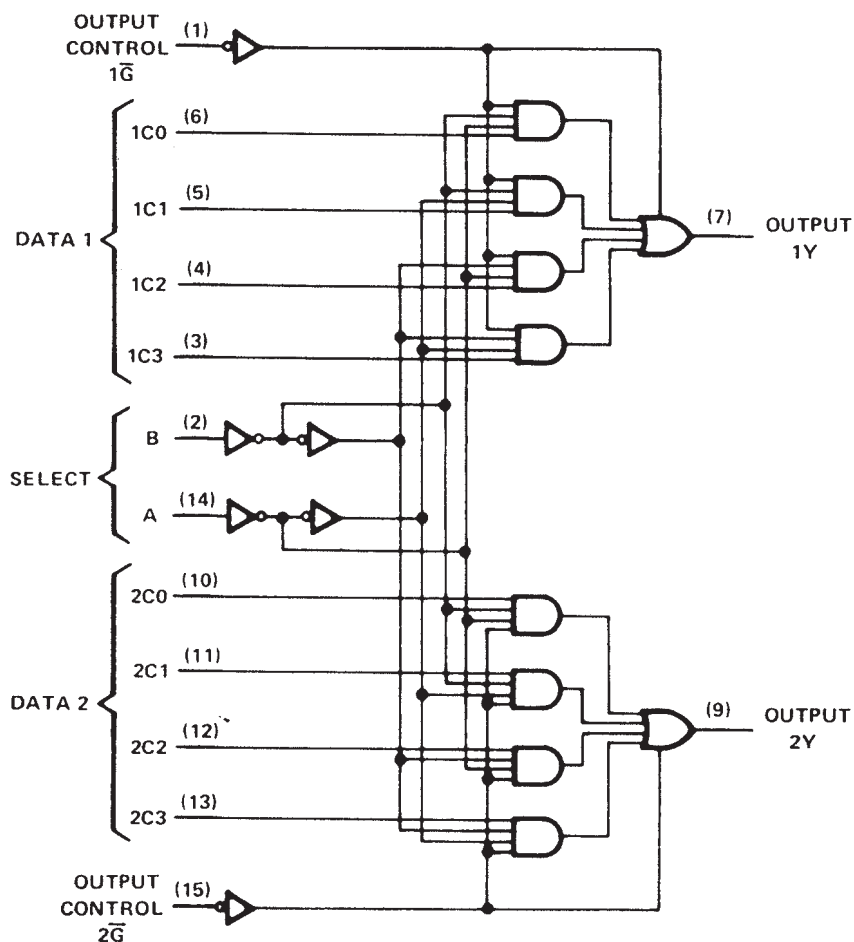
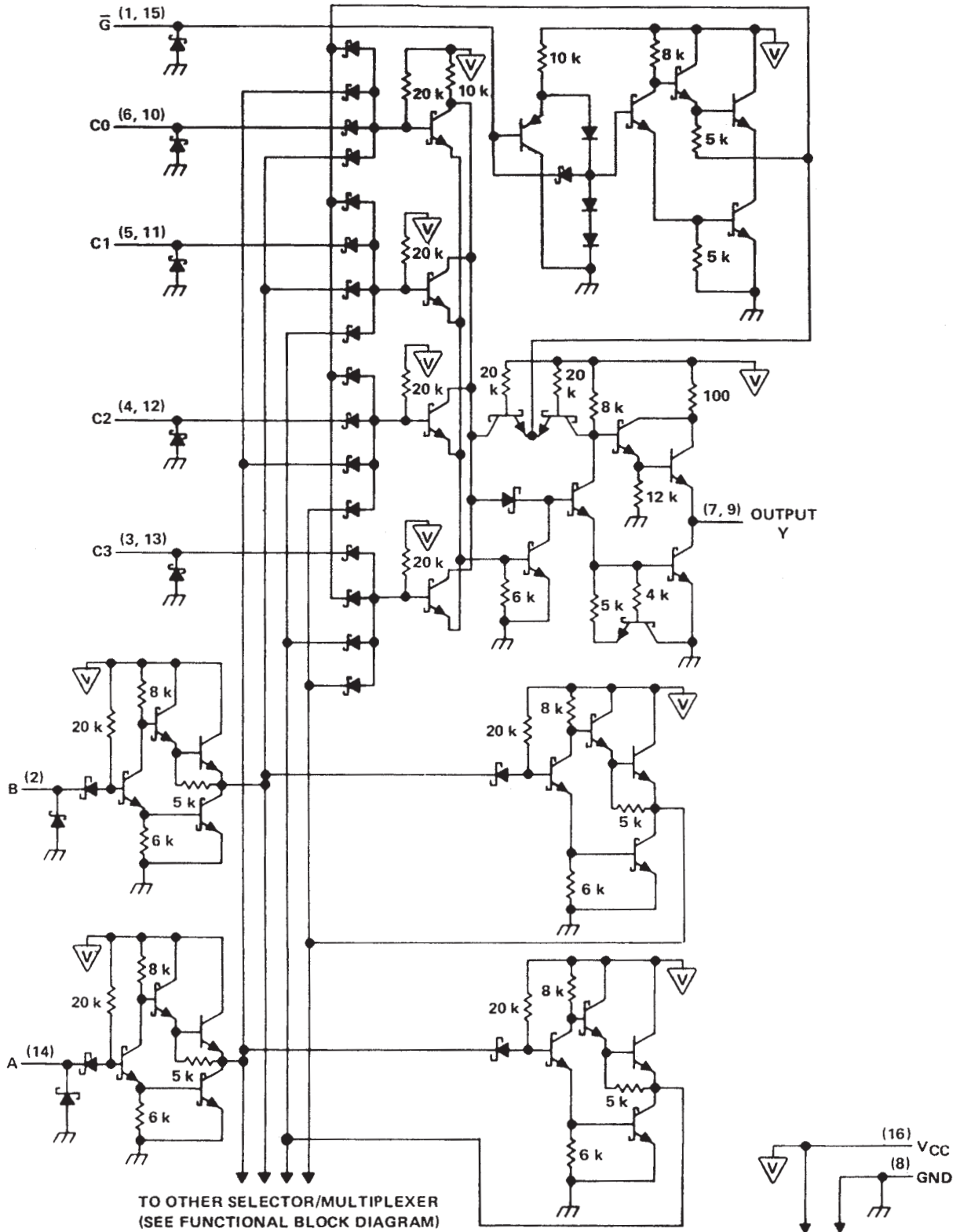Pin numbers shown are for D, J, N, and W packages.

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POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

schematic (each selector/multiplexer, and the common select section)

Pin numbers shown are for D, J, N, and W packages.

recommended operating conditions

		SN54LS253			SN74LS253			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS[†]				SN54LS253			SN74LS253			UNIT
					MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA					−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IH} = 2 V,	V_{IL} = MAX,	I_{OH} = MAX	2.4	3.4		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	V_{IL} = MAX	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.25	0.5	
I_{OZ}	V_{CC} = MAX,	V_{IH} = 2 V		V_O = 2.7 V			20			20	μA
				V_O = 0.4 V			−20			−20	
I_I	V_{CC} = MAX,	V_I = 7 V					0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V					20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V		$\overline{G}$			−0.2			−0.2	mA
				All other			−0.4			−0.4	
I_{OS}[§]	V_{CC} = MAX				−30		−130	−30		−130	mA
I_{CC}	V_{CC} = MAX,	See Note 2		Condition A		7	12		7	12	mA
				Condition B		8.5	14		8.5	14	

† For conditions shown as MIN or MAX, use the appropriate value spcified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration for the short-circuit should exceed one second.
NOTE 2: I_{CC} is measured with the outputs open under the following conditions:
   A. All inputs grounded.
   B. Output control at 4.5 V, all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y				17	25	ns
t_{PHL}						13	20	
t_{PLH}	Select	Y	C_L = 15 pF,	R_L = 2 kΩ,		30	45	ns
t_{PHL}			See Note 3			21	32	
t_{PZH}	Output Control	Y				15	28	ns
t_{PZL}						15	23	
t_{PHZ}	Output Control	Y	C_L = 5 pF,	R_L = 2 kΩ,		27	41	ns
t_{PLZ}			See Note 3			18	27	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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recommended operating conditions

		SN54S253			SN74S253			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-2			-6.5	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†					MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = MIN,	$I_I = -18$ mA						-1.2	V
V_{OH}	V_{CC} = MIN,	V_{IH} = 2 V,	V_{IL} = 0.8 V,	I_{OH} = MAX	Series 54S	2.5	3.4		V
					Series 74S	2.7	3.4		
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	V_{IL} = 0.8 V,	I_{OL} = 20 mA				0.5	V
I_{OZ}	V_{CC} = MAX,	V_{IH} = 2 V			V_O = 2.4 V			50	µA
					V_O = 0.5 V			-50	
I_I	V_{CC} = MAX,	V_I = 5.5 V						1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V						50	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			$\overline{G}$ = 0.8 V			-2	mA
					$\overline{G}$ = 2 V			-0.25	
I_{OS}§	V_{CC} = MAX					-40		-100	mA
I_{CC}	V_{CC} = MAX,	See Note 2			Condition A		45	70	mA
					Condition B		65	85	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
  Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with the outputs open under the following conditions:
      A. All inputs grounded.
      B. Output control at 4.5 V, all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y				6	9	ns
t_{PHL}						6	9	
t_{PLH}	Select	Y	R_L = 280 Ω,	C_L = 15 pF		11.5	18	ns
t_{PHL}			See Note 3			12	18	
t_{PZH}	Output Control	Y				11	16.5	ns
t_{PZL}						12	18	
t_{PHZ}	Output Control	Y	R_L = 280 Ω,	C_L = 5 pF		6.5	9.5	ns
t_{PLZ}			See Note 3			10	15	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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PRODUCT FOLDER | PRODUCT INFO: FEATURES | DESCRIPTION | DATASHEETS | PRICING/AVAILABILITY/PKG | APPLICATION NOTES | RELATED DOCUMENTS

PRODUCT SUPPORT: TRAINING

SN74LS253, Dual 4-Line To 1-Line Data Selectors/Multiplexers With 3-State Outputs
DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54LS253	SN74LS253
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-2.6/8
Output	3S	3S
From	4	4
To	1	1

FEATURES   ▲Back to Top

- Three-State Version of SN54/74LS153, SN54/74S153
- Schottky-Diode-Clamped Transistors
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to Serial Conversion
- Fully Compatible with Most TTL Circuits
- Low Power Dissipation
    - 'LS253 ... 35 mW Typical
    - 'S253 ... 225 mW Typical

DESCRIPTION   ▲Back to Top

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level.

TECHNICAL DOCUMENTS   ▲Back to Top
To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET   ▲Back to Top
Full datasheet in Acrobat PDF: sn74ls253.pdf (220 KB) (Updated: 03/01/1988)

APPLICATION NOTES

View Application Notes for Digital Logic

- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Designing with the SN54/74LS123 (Rev. A) (SDLA006A - Updated: 03/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)

RELATED DOCUMENTS

View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

PRICING/AVAILABILITY/PKG

DEVICE INFORMATION

TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002

REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002

ORDERABLE DEVICE	STATUS	PACKAGE TYPE|PINS	TEMP (ºC)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY|DATE	LEAD TIME	DISTRIBUTOR COMPANY|REGION	IN STOCK	PURCHASE
SN74LS253D	ACTIVE	SOP (D) | 16	0 TO 70	View Contents	1KU | 0.32	40	N/A*	4994 | 03 Oct	4 WKS			
								>10k | 10 Oct				
								>10k | 17 Oct				
								>10k | 24 Oct				
								>10k | 07 Nov				
SN74LS253DR	ACTIVE	SOP (D) | 16	0 TO 70	View Contents	1KU | 0.35	2500	N/A*	779 | 23 Sep	4 WKS			
								1114 | 03 Oct				
								>10k | 10 Oct				
								>10k | 17 Oct				
								>10k | 24 Oct				
SN74LS253J	OBSOLETE	CDIP (J) | 16	0 TO 70	View Contents	1KU |		N/A*		Not Available			
SN74LS253N	ACTIVE	PDIP (N) | 16	0 TO 70	View Contents	1KU | 0.28	25	N/A*	>10k | 02 Oct	4 WKS	Avnet | AMERICA	361	BUY NOW
								6461 | 04 Oct				

								>10k | 09 Oct					
								>10k | 16 Oct					
								>10k | 04 Dec					
SN74LS253N3	OBSOLETE	PDIP (N) | 16	0 TO 70	View Contents	1KU |		N/A*		Not Available			
SN74LS253NSR	ACTIVE	SOP (NS) | 16		View Contents	1KU | 0.28	2000	N/A*	6429 | 04 Oct	4 WKS			
								2302 | 11 Oct					
								>10k | 18 Oct					
								>10k | 08 Nov					
								>10k | 15 Nov					

Table Data Updated on: 9/26/2002