

# 54F/74F564

## Octal D-Type Flip-Flop With 3-State Outputs

### Description

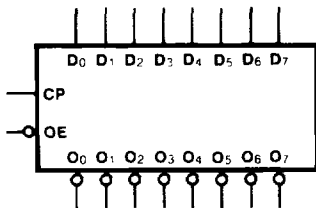
The 'F564 is a high speed low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ( $\overline{OE}$ ). The information presented to the inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

This device is functionally identical to the 'F574, but has inverted outputs.

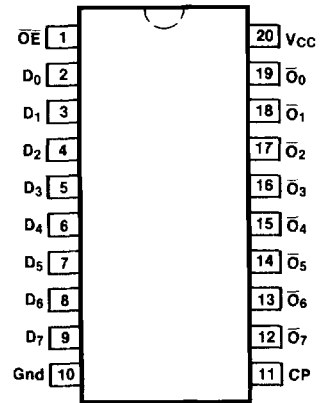
- Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessors
- Functionally Identical to 'F574
- 3-State Outputs for Bus-Oriented Applications

**Ordering Code:** See Section 5

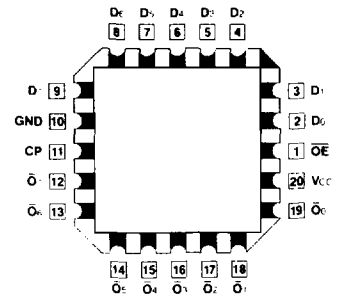
### Logic Symbol



### Connection Diagrams



**Pin Assignment for DIP and SOIC**



**Pin Assignment for LCC and PCC**

**Input Loading/Fan-Out:** See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D <sub>0</sub> -D <sub>7</sub>	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
$\overline{O_0}$ - $\overline{O_7}$	3-State Outputs	75/15 (12.5)

## Functional Description

The 'F564 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times

requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

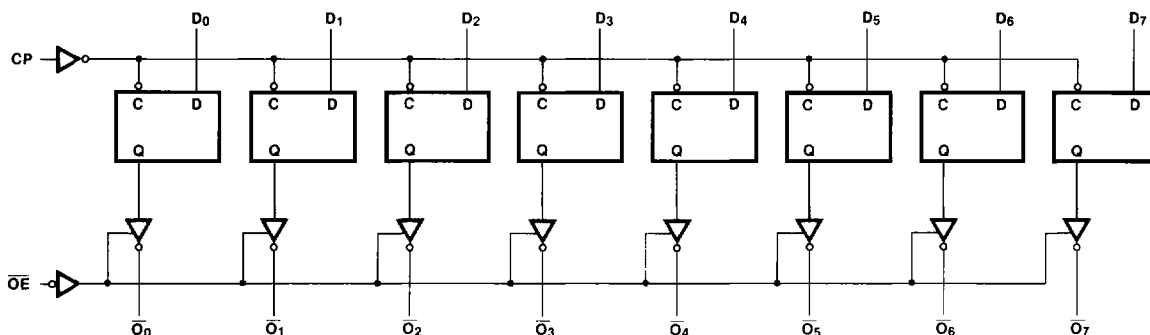
## Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↑	L	H	Z	Load
H	↑	H	L	Z	Load
L	↑	L	H	H	Data Available
L	↑	H	L	L	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 ↑ = LOW-to-HIGH Transition  
 NC = No Change

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## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
$I_{CC}$	Power Supply Current		55	86	mA	$V_{CC} = \text{Max}$ , $D_n = \text{Gnd}$ , $\overline{OE} = \text{HIGH}$

**AC Characteristics:** See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$	$T_A, V_{CC} =$ Mil $C_L = 50\text{ pF}$	$T_A, V_{CC} =$ Com $C_L = 50\text{ pF}$		
		Min Typ Max	Min Max	Min Max		
$f_{\text{max}}$	Maximum Clock Frequency	100			MHz	3-1
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $\bar{O}_n$		7.5 9.5		ns	3-1 3-7
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output Enable Time		11.5 7.5		ns	3-1 3-12
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output Disable Time		7.0 5.5			

**AC Operating Requirements:** See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$	$T_A, V_{CC} =$ Mil	$T_A, V_{CC} =$ Com		
		Min Typ Max	Min Max	Min Max		
$t_{\text{s(H)}}$ $t_{\text{s(L)}}$	Setup Time, HIGH or LOW $D_n$ to CP	2.0 2.0			ns	3-5
$t_{\text{h(H)}}$ $t_{\text{h(L)}}$	Hold Time, HIGH or LOW $D_n$ to CP	2.0 2.0				
$t_{\text{w(H)}}$ $t_{\text{w(L)}}$	CP Pulse Width HIGH or LOW	5.0 5.0			ns	3-7