

**Octal bus transceiver/register; 3-state; inverting**

**74HL33648**

**FEATURES**

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with the JEDEC 3.3 V ±0.3 V supply
- CMOS low power consumption
- Flow-through pin-out architecture
- Low inductance, multiple centre power and ground pins for minimum noise and ground bounce
- 3-state outputs
- Direct interface with TTL levels

**DESCRIPTION**

The 74HL33648 consist of 8 inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the 'A' or 'B' bus will be clocked in the internal registers, as the appropriate clock (CP<sub>AB</sub> or CP<sub>BA</sub>) goes to a HIGH logic level. Output enable ( $\overline{OE}$ ) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the 'A' or 'B' register, or in both. The select source inputs (S<sub>AB</sub> and S<sub>BA</sub>) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when  $\overline{OE}$  is active (LOW). In the isolation mode ( $\overline{OE}$  = HIGH), 'A' data may be stored in the 'B' register and/or 'B' data may be stored in the 'A' register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, 'A' or 'B' may be driven at a time.

The '648' is functionally identical to the '646', but has inverting data paths.

**QUICK REFERENCE DATA**

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay A <sub>n</sub> , B <sub>n</sub> to B <sub>n</sub> , A <sub>n</sub>	C <sub>L</sub> = 50 pF V <sub>CC</sub> = 3.3 V	3.4	ns
f <sub>max</sub>	maximum clock frequency		350	MHz
C <sub>I</sub>	input capacitance		3.5	pF
C <sub>PD</sub>	power dissipation capacitance per latch	notes 1 and 2	50	pF

**Notes to the quick reference data**

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz; C<sub>L</sub> = output load capacity in pF;  
 f<sub>o</sub> = output frequency in MHz; V<sub>CC</sub> = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.
2. The condition is V<sub>i</sub> = GND to V<sub>CC</sub>.

**ORDERING INFORMATION**

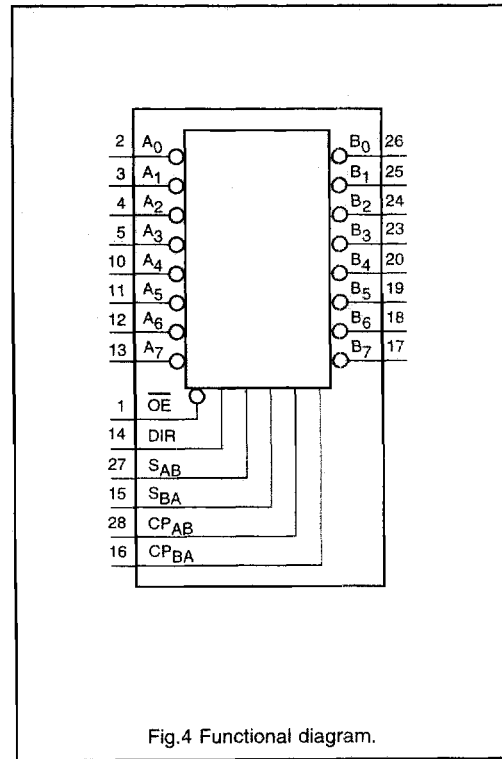
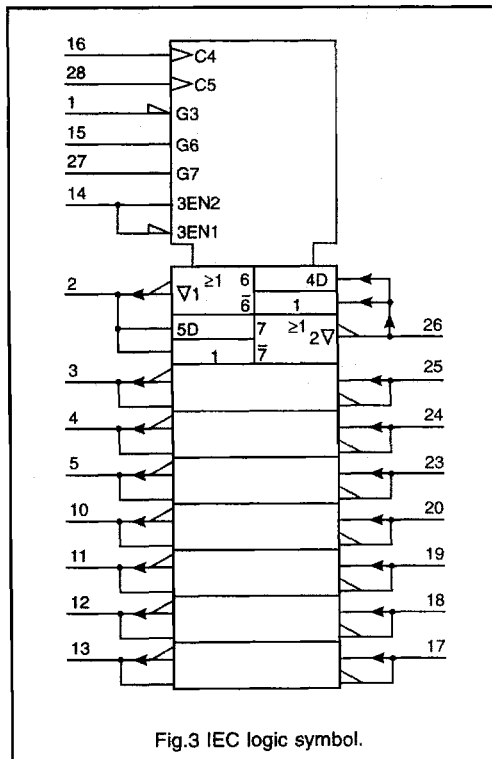
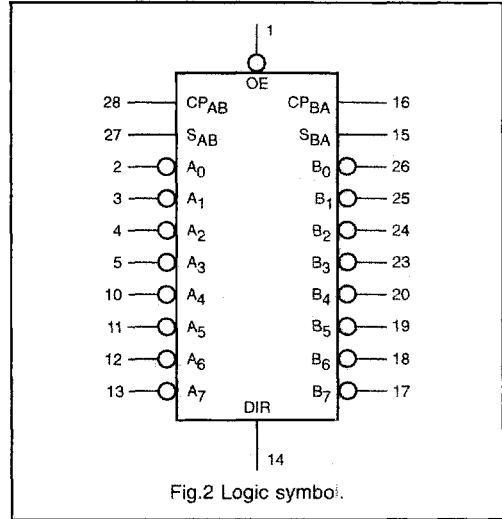
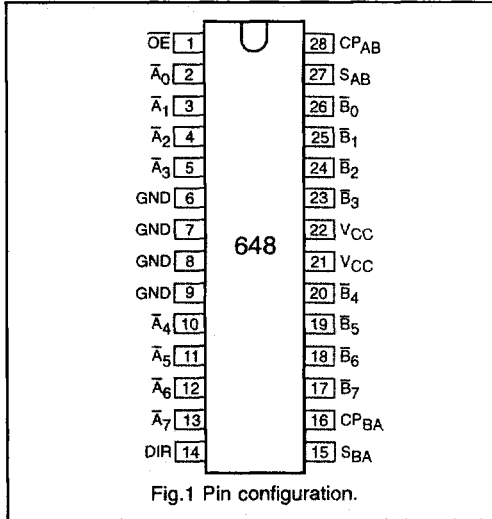
TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HL33648D	28	SO	plastic	SOT136-1
74HL33648DB	28	SSOP	plastic	SOT341-1
74HL33648PW	28	TSSOP	plastic	SOT361-1

**PINNING**

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 3, 4, 5, 10, 11, 12, 13	A <sub>0</sub> to A <sub>7</sub>	'A' data inputs/outputs
6, 7, 8, 9	GND	ground (0 V)
14	DIR	direction control input
15	S <sub>BA</sub>	select 'B' to 'A' source input
16	CP <sub>BA</sub>	'B' to 'A' clock input (Low-to-High, edge-triggered)
26, 25, 24, 23, 20, 19, 18, 17	B <sub>0</sub> to B <sub>7</sub>	'B' data inputs/outputs
21, 22	V <sub>CC</sub>	positive supply voltage
27	S <sub>AB</sub>	select 'A' to 'B' source input
28	CP <sub>AB</sub>	'A' to 'B' clock input (Low-to-High, edge-triggered)

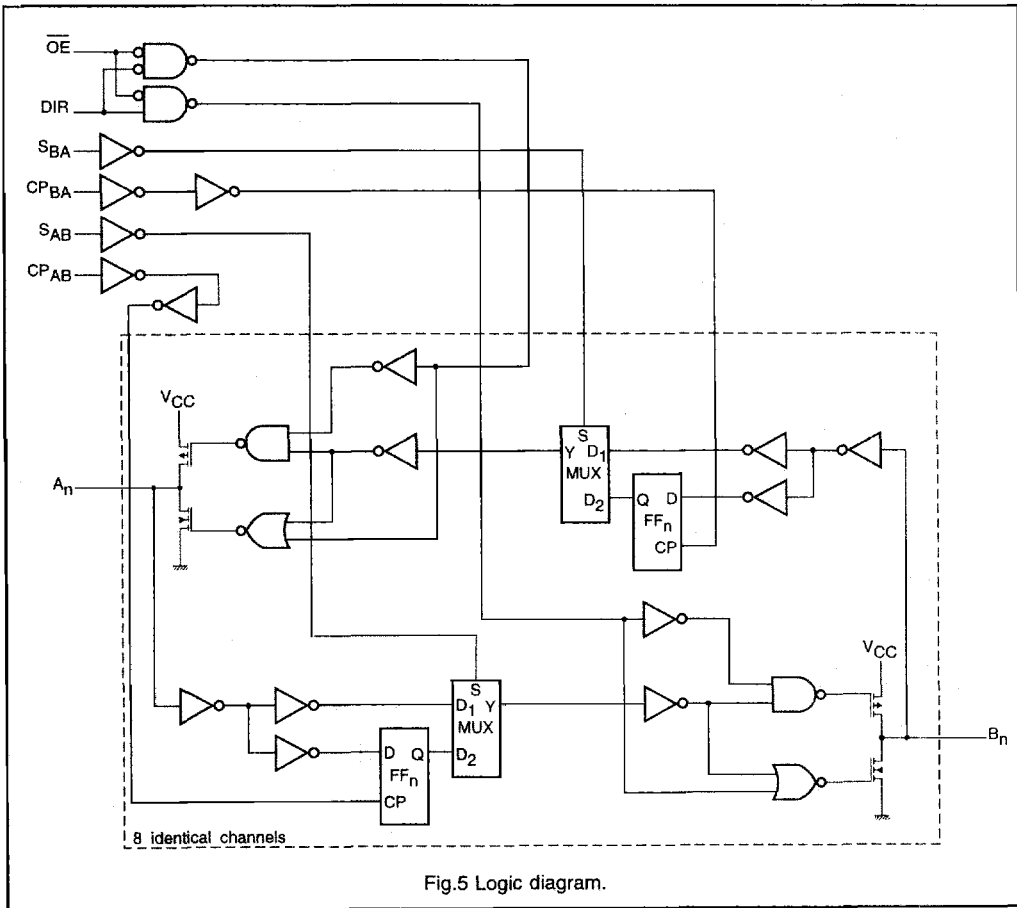
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FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$\overline{OE}$	DIR	$CP_{AB}$	$CP_{BA}$	$S_{AB}$	$S_{BA}$	$\overline{A}_0$ to $\overline{A}_7$	$\overline{B}_0$ to $\overline{B}_7$	
X	X	↑	X	X	X	input	un*	store A, B unspecified*
X	X	X	↑	X	X	un*	input	store B, A unspecified*
H	X	↑	↑	X	X	input	input	store A and B data, isolation hold storage
H	X	H or L	H or L	X	X			
L	L	X	X	X	L	output	input	real-time $\overline{B}$ data to A bus stored $\overline{B}$ data to A bus
L	L	X	H or L	X	H			
L	H	X	X	L	X	input	output	real-time $\overline{A}$ data to B bus stored $\overline{A}$ data to B bus
L	H	H or L	X	H	X			

\* The data output functions may be enabled or disabled by various signals at the  $\overline{OE}$  and DIR inputs. Data input functions are always enabled, i.e., data at

the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified  
 H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 ↑ = LOW-to-HIGH level transition

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## DC CHARACTERISTICS FOR 74HL33648

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

 $I_{CC}$  category: MSI

## AC CHARACTERISTICS FOR 74HL33648

GND = 0 V;  $t_r = t_f = 2.0$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)				UNIT	TEST CONDITIONS	
		+25		-40 to +85			$V_{CC}$ (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
$t_{PHL}/t_{PLH}$	propagation delay $A_n, B_n$ to $\overline{B}_n, \overline{A}_n$	-	19.5	-	22.4	ns	1.2	Fig.6
		-	7.3	-	8.4	2.0		
		-	4.9	-	5.6	3.0		
$t_{PHL}/t_{PLH}$	propagation delay $CP_{AB}, CP_{BA}$ to $\overline{B}_n, \overline{A}_n$	-	23.2	-	26.8	ns	1.2	Fig.7
		-	8.7	-	10.1	2.0		
		-	5.8	-	6.7	3.0		
$t_{PHL}/t_{PLH}$	propagation delay $S_{AB}, S_{BA}$ to $\overline{B}_n, \overline{A}_n$	-	24.4	-	28.0	ns	1.2	Fig.8
		-	9.2	-	10.5	2.0		
		-	6.1	-	7.0	3.0		
$t_{PZH}/t_{PZL}$	3-state output enable time $\overline{OE}$ to $\overline{A}_n, \overline{B}_n$	-	24.4	-	28.0	ns	1.2	Fig.9
		-	9.2	-	10.5	2.0		
		-	6.1	-	7.0	3.0		
$t_{PHZ}/t_{PLZ}$	3-state output disable time $\overline{OE}$ to $\overline{A}_n, \overline{B}_n$	-	19.5	-	22.3	ns	1.2	Fig.9
		-	8.1	-	9.1	2.0		
		-	5.8	-	6.5	3.0		
$t_{PZH}/t_{PZL}$	3-state output enable time DIR to $\overline{A}_n, \overline{B}_n$	-	26.0	-	30.0	ns	1.2	Fig.10
		-	9.8	-	11.3	2.0		
		-	6.5	-	7.5	3.0		
$t_{PHZ}/t_{PLZ}$	3-state output disable time DIR to $\overline{A}_n, \overline{B}_n$	-	20.3	-	23.1	ns	1.2	Fig.10
		-	8.4	-	9.5	2.0		
		-	6.0	-	6.7	3.0		
$t_W$	clock pulse width HIGH or LOW $CP_{AB}$ or $CP_{BA}$	3.0	-	3.7	-	ns	2.0	Figs 6 and 8
		2.0	-	2.5	-	3.0		
$t_{SU}$	set-up time $A_n, B_n$ to $CP_{AB}, CP_{BA}$	-	-	-	-	ns	1.2	Fig.7
		1.0	-	1.0	-	2.0		
$t_H$	hold time $A_n, B_n$ to $CP_{AB}, CP_{BA}$	-	-	-	-	ns	1.2	Fig.7
		1.0	-	1.0	-	2.0		
$f_{max}$	maximum clock pulse frequency	150	-	100	-	ns	2.0	Fig.7
		200	-	150	-	3.0		

AC WAVEFORMS

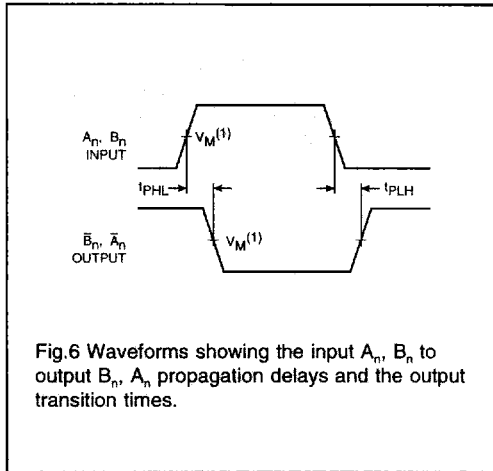


Fig.6 Waveforms showing the input A<sub>n</sub>, B<sub>n</sub> to output B<sub>n</sub>, A<sub>n</sub> propagation delays and the output transition times.

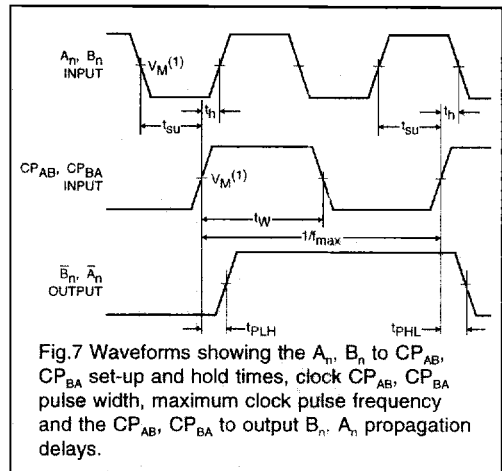


Fig.7 Waveforms showing the A<sub>n</sub>, B<sub>n</sub> to CP<sub>AB</sub>, CP<sub>BA</sub> set-up and hold times, clock CP<sub>AB</sub>, CP<sub>BA</sub> pulse width, maximum clock pulse frequency and the CP<sub>AB</sub>, CP<sub>BA</sub> to output B<sub>n</sub>, A<sub>n</sub> propagation delays.

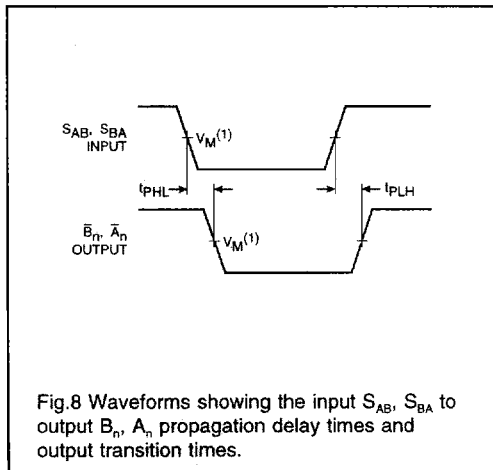


Fig.8 Waveforms showing the input S<sub>AB</sub>, S<sub>BA</sub> to output B<sub>n</sub>, A<sub>n</sub> propagation delay times and output transition times.

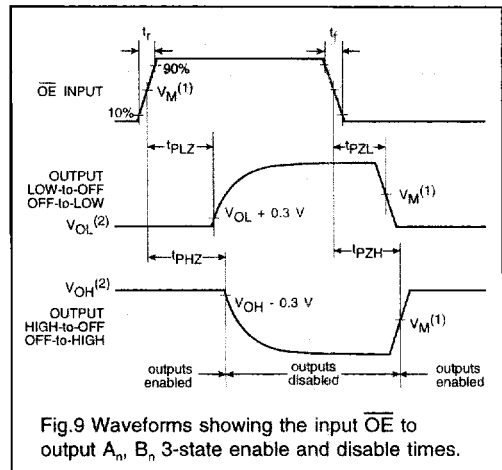


Fig.9 Waveforms showing the input OE to output A<sub>n</sub>, B<sub>n</sub> 3-state enable and disable times.

- Notes:**
- (1) V<sub>M</sub> = 0.6 V at V<sub>CC</sub> = 1.2 V.  
 V<sub>M</sub> = 1.0 V at V<sub>CC</sub> = 2.0 V.  
 V<sub>M</sub> = 1.5 V at V<sub>CC</sub> = 3.0 V.
  - (2) V<sub>OL</sub> and V<sub>OH</sub> are the typical output voltage drop that occur with the 3-state output load.

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## AC WAVEFORMS (Continued)

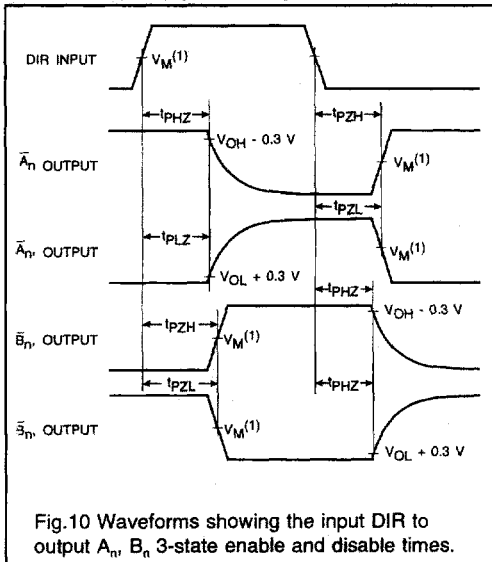


Fig.10 Waveforms showing the input DIR to output  $A_n$ ,  $B_n$  3-state enable and disable times.

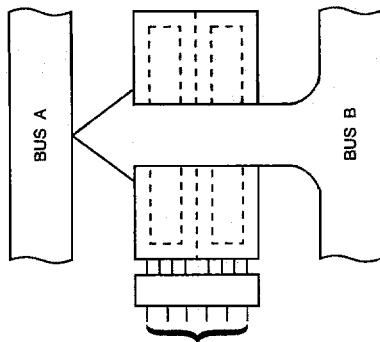
- Notes:**
- (1)  $V_M = 0.6\text{ V}$  at  $V_{CC} = 1.2\text{ V}$ .  
 $V_M = 1.0\text{ V}$  at  $V_{CC} = 2.0\text{ V}$ .  
 $V_M = 1.5\text{ V}$  at  $V_{CC} = 3.0\text{ V}$ .
  - (2)  $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the 3-state output load.

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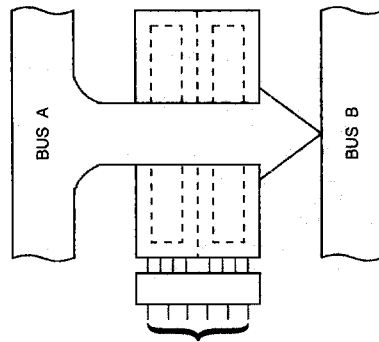
**APPLICATION INFORMATION**

Real-time transfer; bus B to bus A



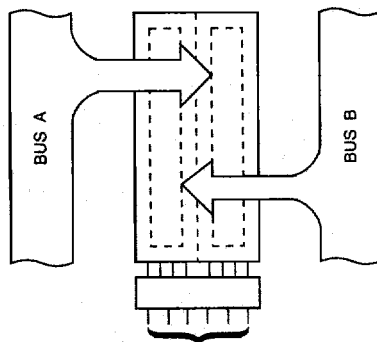
(1)	(14)	(28)	(16)	(27)	(15)
$\overline{OE}$	DIR	CP <sub>AB</sub>	CP <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>
L	L	X	X	X	L

Real-time transfer; bus A to bus B



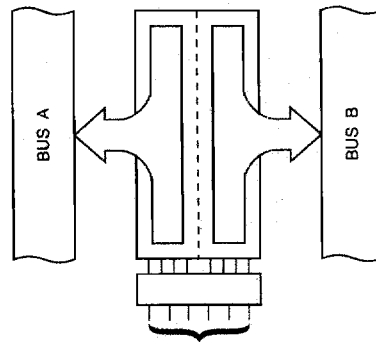
(1)	(14)	(28)	(16)	(27)	(15)
$\overline{OE}$	DIR	CP <sub>AB</sub>	CP <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>
L	H	X	X	L	X

Storage from A, B or A and B



(1)	(14)	(28)	(16)	(27)	(15)
$\overline{OE}$	DIR	CP <sub>AB</sub>	CP <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

Transfer storage data to A or B



(1)	(14)	(28)	(16)	(27)	(15)
$\overline{OE}$	DIR	CP <sub>AB</sub>	CP <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>
L	L	X	H or L	X	H
L	H	H or L	X	H	X