

HEX Inverter

The TC74HC04A is a high speed CMOS INVERTER fabricated with silicon gate C²MOS technology.

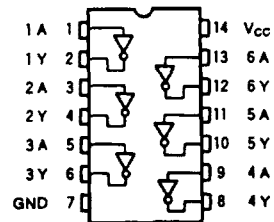
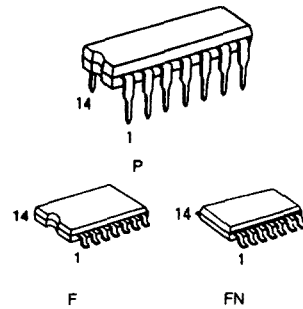
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

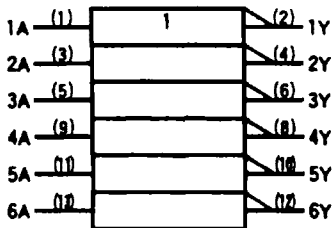
Features

- High Speed: $t_{pd} = 6\text{ns(Typ.)}$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation: $I_{CC} = 1\mu\text{A(Max.)}$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}(\text{Min.})$
- Output Drive Capability: 10 LSTTL Loads
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL} = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays: $t_{PLH} = t_{PHL}$
- Wide Operating Voltage Range: $V_{CC}(\text{opr}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS04



(TOP VIEW)

Pin Assignment



IEC Logic Symbol

Truth Table

A	Y
L	H
H	L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 - V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5 - V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} /Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 - V_{CC}	V
Output Voltage	V_{OUT}	0 - V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 - 1000($V_{CC} = 2.0\text{V}$) 0 - 500($V_{CC} = 4.5\text{V}$) 0 - 400($V_{CC} = 6.0\text{V}$)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		Unit		
			V_{CC}	Min	Typ.	Max.	Min.		Max.	
High-Level Input Voltage	V_{IH}	-	2.0	1.5	-	-	1.5	-	V	
			4.5	3.15	-	-	3.15	-		
			6.0	4.2	-	-	4.2	-		
Low-Level Input Voltage	V_{IL}	-	2.0	-	-	0.5	-	0.5	V	
			4.5	-	-	1.35	-	1.35		
			6.0	-	-	1.8	-	1.8		
High-Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
			$I_{OH} = -4\text{mA}$ $I_{OH} = -5.2\text{mA}$	4.5	4.18	4.31	-	4.13	-	
				6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20\mu\text{A}$	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
			$I_{OL} = 4\text{mA}$ $I_{OL} = 5.2\text{mA}$	4.5	-	0.17	0.26	-	0.33	
				6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0	-	-	±0.1	-	±1.0	μA	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	6.0	-	-	1.0	-	10.0		

AC Electrical Characteristics ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$, Input $t_r = t_f = 6\text{ns}$)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Transition Time	t_{TLH} t_{THL}	–	–	4	8	ns
Propagation Delay Time	t_{PLH} t_{PHL}	–	–	6	12	

AC Electrical Characteristics ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

Parameter	Symbol	Test Condition	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		Unit	
			V_{CC}	Min.	Typ.	Max.	Min.		Max.
Output Transition Time	t_{TLH} t_{THL}	–	2.0	–	25	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{PLH} t_{PHL}	–	2.0	–	27	75	–	95	
			4.5	–	9	15	–	19	
			6.0	–	8	13	–	16	
Input Capacitance	C_{IN}	–	–	5	10	–	10	pF	
Power Dissipation Capacitance	$C_{PD(1)}$	–	–	20	–	–	–		

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$$I_{CC(oper)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6(\text{per Gate})$$

Notes