Quad Register With Two Independently Controlled Three-State Outputs 2919

PRELIMINARY DATA

Features/Benefits

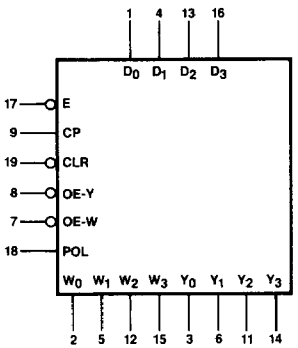
- **Two sets of fully buffered three-state outputs**
- **Four D-type flip-flops**
- **Polarity control on one set of outputs**
- **Buffered common clock enable**
- **Buffered common asynchronous clear**
- **Separate buffered common output enable for each set of outputs**
- **100% product assurance screening to MIL-STD-883 requirements**

Description

The 29LS19 consists of four D-type flip-flops with a buffered common clock enable. Information meeting the set-up and hold time requirements of the D inputs is transferred to the flip-flop outputs on the LOW-to-HIGH transition of the clock. Data on the Q outputs of the flip-flops is enabled at the three-state outputs when the output control ($\overline{OE}$) input is LOW. When the appropriate $\overline{OE}$ input is HIGH, the outputs are in the high impedance state. Two independent sets of outputs—W and Y—are provided such that the register can simultaneously and independently drive two buses. One set of outputs contains a polarity control such that the outputs can either be inverting or non-inverting.

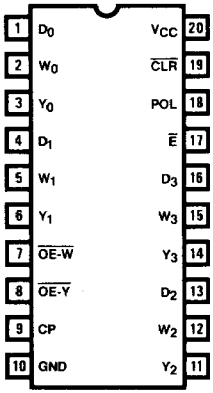
The device also features an active LOW asynchronous clear. When the clear input is LOW, the Q output of the internal flip-flops are forced LOW independent of the other inputs. The 29LS19 is packaged in a space saving (0.3-inch row spacing) 20-pin package.

Logic Symbol

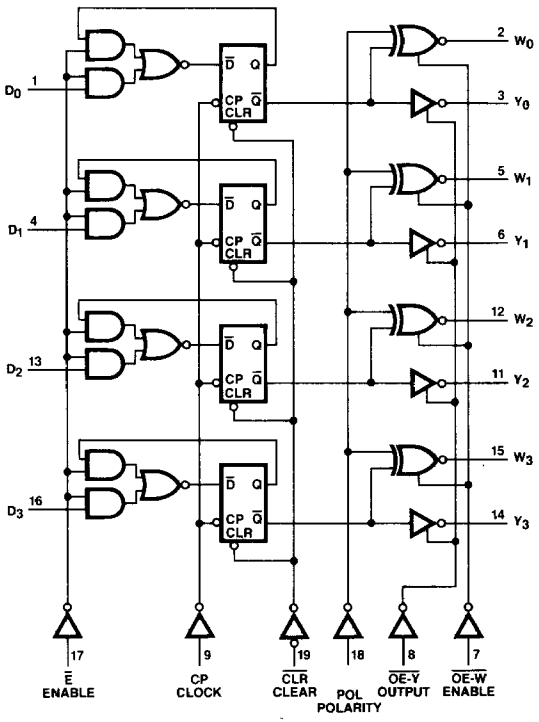


V_{CC} = Pin 20
GND = Pin 10

Pin Configuration



Logic Diagram



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Absolute Maximum Ratings

Storage temperature ..... −65°C to +150°C
Temperature (ambient) under bias ..... −55°C to +125°C
Supply voltage to ground potential continuous ..... −0.5 V to +7.0 V
DC voltage applied to outputs for high output state ..... −0.5 V to + V_{CC} max.
DC input voltage ..... −0.5 V to +7.0 V
DC output current, into outputs 30mA
DC input current ..... −30mA to +5.0mA

Electrical Characteristics

Over Recommended Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MILITARY T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% MIN = 4.50V, MAX = 5.50V MIN	TYP[2]	MAX	COMMERCIAL T_A = 0°C to +70% V_{CC} = 5.0V ± 5% MIN = 4.75V, MAX = 5.25V MIN	TYP[2]	MAX	UNIT
V_{OH}	Output HIGH voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.0mA	2.4	3.4					V
			I_{OH} = −2.6mA				2.4	3.4		
V_{OL}	Output LOW voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4			0.4	V
			I_{OL} = 8.0mA			0.45			0.45	
			I_{OL} = 12mA			0.5			0.5	
V_{IH}	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs		2.0			2.0			V
V_{IL}	Input LOW level	Guaranteed input logical LOW voltage for all inputs				0.7			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5			−1.5	V
I_{IL}	Input LOW current	V_{CC} = MAX, V_{IN} = 0.4V				−0.36			−0.36	mA
I_{IH}	Input HIGH current	V_{CC} = MAX, V_{IN} = 2.7V				20			20	μA
I_I	Input HIGH current	V_{CC} = MAX, V_{IN} = 7.0V				0.1			0.1	mA
I_{OZ}	Off-state (high-impedance) output current	V_{CC} = MAX	V_O = 0.4V			−20			−20	μA
			V_O = 2.4V			20			20	
I_{SC}	Output short circuit current[3]	V_{CC} MAX		−15		−85	−15		−85	mA
I_{CC}	Power supply current[4]	V_{CC} = MAX			24	36		24	39	mA

NOTES: 1. For conditions shown as MIN, or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics

T_A +25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Clock to Y_i		C_L = 15pF R_L = 2.0kΩ		22	33	ns
t_{PHL}					20	30	
t_{PHL}	Clock to W_i (either polarity)				24	36	ns
t_{PHL}					24	36	
t_{PHL}	Clear to Y_i				29	43	ns
t_{PLH}	Clear to W_i				25	37	ns
t_{PHL}				30	45		
t_{PLH}	Polarity to W_i			23	34		ns
t_{PHL}					25	37	
t_{pw}	Clear			18			ns
t_{pw}	Clock pulse width	LOW		15			ns
		HIGH		18			
t_s	Data			15			ns
t_h	Data			5			ns
t_s	Data enable			20			ns
t_h	Data enable			0			ns
t_s	Set-up time, clear recovery (inactive) to clock			20	15		ns
t_{ZH}	Output enable to W or Y				11	17	ns
t_{ZL}					13	20	
t_{HZ}	Output enable to W or Y		C_L = 5.0pF R_L = 2.0kΩ		13	20	ns
t_{LZ}					11	17	
f_{max}	Maximum clock frequency[1]		C_L = 15pF R_L = 2.0kΩ	35	45		MHz

NOTES: 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle. 2.4AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Switching Characteristics

Over Operating Range[2]

SYMBOL	PARAMETER		TEST CONDITIONS	COMMERCIAL T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% MIN	COMMERCIAL MAX	MILITARY T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% MIN	MILITARY MAX	UNIT
t_{PLH}	Clock to Y_i		C_L = 50pF, R_L = 2.0kΩ		39		42	ns
t_{PHL}					39		45	
t_{PLH}	Clock to W_i (Either polarity)				41		43	ns
t_{PHL}					44		48	
t_{PHL}	Clear to Y_i				52		58	ns
t_{PLH}	Clear to W_i				42		43	ns
t_{PHL}					51		53	
t_{PLH}	Polarity to W_i				41		45	ns
t_{PHL}					42		44	
t_{pw}	Clear			20		20		ns
t_{pw}	Clock	LOW		20		20		ns
		HIGH		20		20		
t_s	Data			15		15		ns
t_h	Data			10		10		ns
t_s	Data enable			25		25		ns
t_h	Data enable			0		0		ns
t_s	Set-up time, clear recovery (inactive) to clock			23		24		ns
t_{ZH}	Output enable to W_i or Y_i				24		27	ns
t_{ZL}					29		35	
t_{HZ}	Output enable to W_i or Y_i		C_L = 5.0pF, R_L = 2.0kΩ		33		45	ns
t_{LZ}					22		26	
f_{max}	Maximum clock frequency[1]		C_L = 50pF, R_L = 2.0kΩ	30		25		MHz

NOTES: 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.
2. AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Function Table

FUNCTION	INPUTS							INTERNAL	OUTPUTS	
	CP	D_i	$\overline{E}$	$\overline{CLR}$	POL	$\overline{OE\text{-}W}$	$\overline{OE\text{-}Y}$	Q	W_i	Y_i
Output Three-State Control	X	X	X	X	X	H	L	NC	Z	Enabled
	X	X	X	X	X	L	H	NC	Enabled	Z
	X	X	X	X	X	H	H	NC	Z	Z
	X	X	X	X	X	L	L	NC	Enabled	Enabled
W_i Polarity	X	X	X	X	L	L	L	NC	Non-Inverting	Non-Inverting
	X	X	X	X	H	L	L	NC	Inverting	Non-Inverting
Asynchronous Clear	X	X	X	L	L	L	L	L	L	L
	X	X	X	L	H	L	L	L	H	L
Clock Enabled	↑	X	H	H	X	X	X	NC	NC	NC
	↑	L	L	H	L	L	L	L	L	L
	↑	L	L	H	H	L	L	L	H	L
	↑	H	L	H	L	L	L	H	H	H
	↑	H	L	H	H	L	L	H	L	H

L LOW
H = HIGH
Z = High Impedance
X = Don't Care
NC = No Change
↑ = LOW to HIGH Transition

Definition of Functional Terms

Data lines, D_i
Any of the four D flip-flops data lines.

Clock enable $\overline{E}$
When LOW, the data is entered into the register on the next clock LOW-to-HIGH transition. When HIGH, the data in the register remains unchanged, regardless of the data in.

Clock pulse, CP
Data is entered into the register on the LOW-to-HIGH transition.

Output enable, $\overline{OE\text{-}W}$, $\overline{OE\text{-}Y}$
When $\overline{OE}$ is LOW, the register is enable to the output. When HIGH, the output is in the high-impedance state. The $\overline{OE\text{-}W}$ controls the W set of outputs, and $\overline{OE\text{-}Y}$ controls the Y set.

Output lines, Y_i
Any of the four non-inverting three-state output lines.

Outputs with polarity control, W_i
Any of the four three-state outputs with polarity control.

Polarity Control, POL
The W_i outputs will be non-inverting when POL is LOW, and when it is HIGH, the outputs are inverting.

Asynchronous clear, $\overline{CLR}$
When $\overline{CLR}$ is LOW, the internal Q flip-flops are reset to LOW.