National Semiconductor

March 1993

54ACTQ/74ACTQ16543 16-Bit Registered Transceiver with TRI-STATE® Outputs

General Description

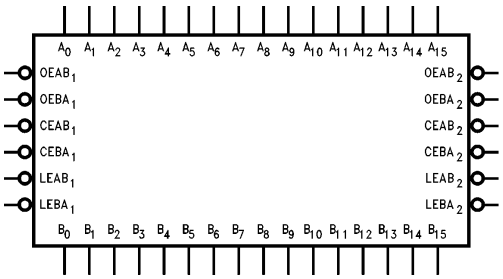
The 'ACTQ16543 contains sixteen non-inverting transceivers containing two sets of D-type registers for temporary storage of data flowing in either direction. Each byte has separate control inputs which can be shorted together for full 16-bit operation. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent input and output control in either direction of data flow.

The ACTQ16543 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector for superior performance.

Features

- Utilizes NSC FACT Quiet Series technology
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin output skew
- Independent registers for A and B buses
- Separate controls for data flow in each direction
- Back-to-back registers for storage
  Multiplexed real-time and stored data transfers
- Separate control logic for each byte
- 16-bit version of the 'ACTQ543
- Outputs source/sink 24 mA
- Additional specs for Multiple Output Switching
- Output loading specs for both 50 pF and 250 pF loads

Logic Symbol

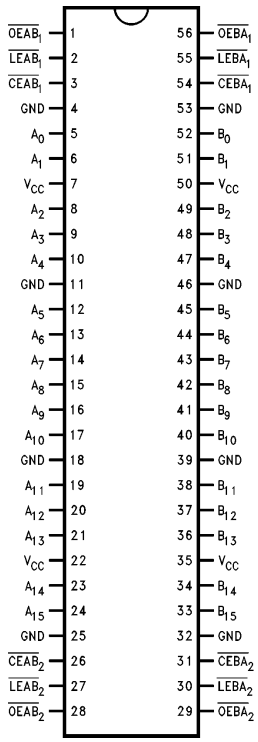


TL/F/10967–1

Pin Names	Description
$\overline{OEAB}_n$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}_n$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}_n$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}_n$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}_n$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}_n$	B-to-A Latch Enable Input (Active LOW)
A_0–A_{15}	A-to-B Data Inputs or B-to-A TRI-STATE Outputs
B_0–B_{15}	B-to-A Data Inputs or A-to-B TRI-STATE Outputs

Connection Diagram

Pin Assignment for SSOP and CERPAK



TL/F/10967–2

TRI-STATE® is a registered trademark of National Semiconductor Corporation.
FACT™, FACT Quiet Series™ and GTO™ are trademarks of National Semiconductor Corporation.

Functional Description

The 'ACTQ16543 contains sixteen non-inverting transceivers with TRI-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The following description applies to each byte. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}_n$) input must be LOW in order to enter data from A_0–A_{15} or take data from B_0–B_{15}, as indicated in the Data I/O Control Table. With $\overline{CEAB}_n$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}_n$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}_n$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}_n$ and $\overline{OEAB}_n$ both LOW, the TRI-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}_n$, $\overline{LEBA}_n$ and $\overline{OEBA}_n$ inputs.

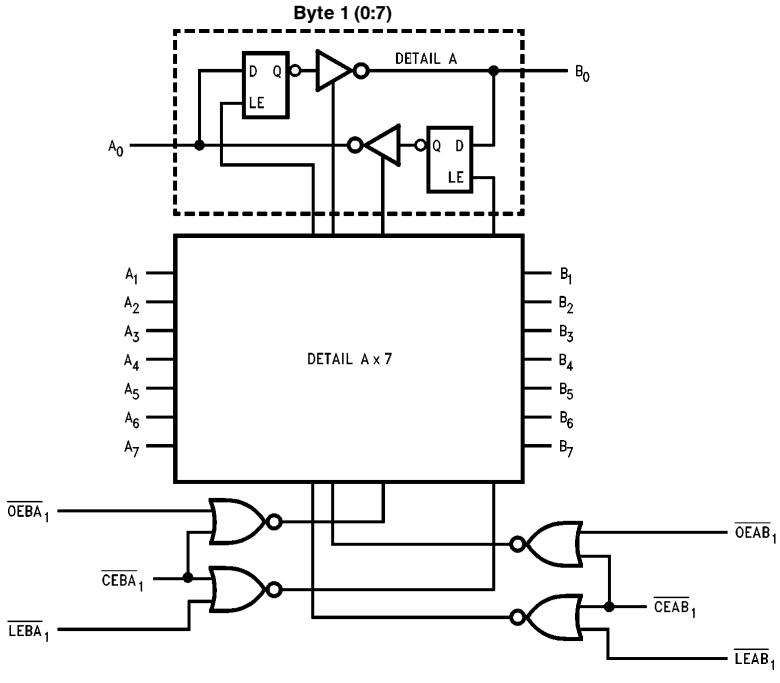
Data I/O Control Table

Inputs			Latch Status (Byte n)	Output Buffers (Byte n)
$\overline{CEAB}_n$	$\overline{LEAB}_n$	$\overline{OEAB}_n$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}_n$, $\overline{LEBA}_n$ and $\overline{OEBA}_n$

Logic Diagrams

Byte 1 (0:7)

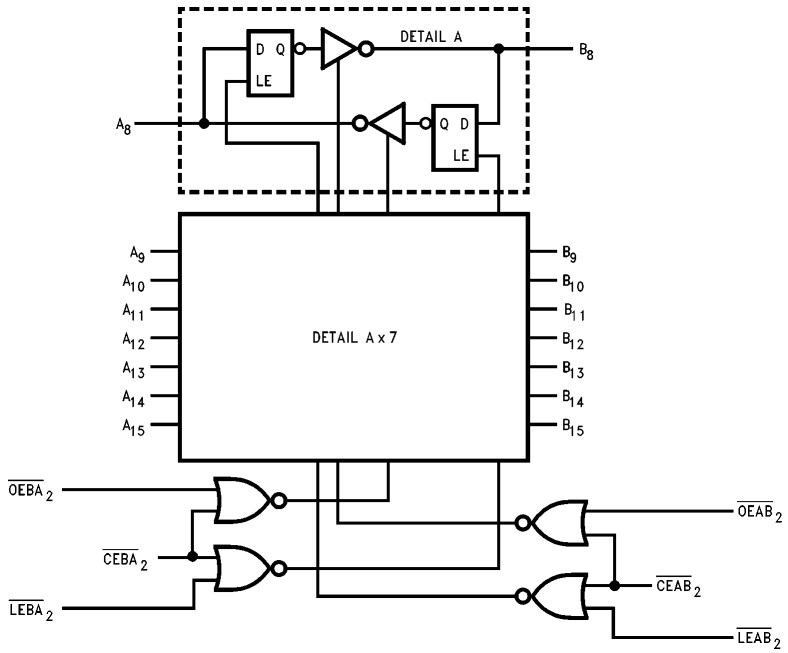


TL/F/10967–3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagrams (Continued)

Byte 2 (8:15)



TL/F/10967–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source/Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin	±50 mA
Junction Temperature	
CDIP	+175°C
PDIP/SOIC	+140°C
Storage Temperature	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Note 2: For qualification information please refer to the NSC SSOP Qualification Handbook.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACTQ	−40°C to +85°C
54ACTQ	−55°C to +125°C
Minimum Input Edge Rate (dV/dt)	
'ACTQ Devices	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ		54ACTQ	74ACTQ	Units	Conditions
			T_A = +25°C		T_A = −55°C to +125°C	T_A = −40°C to +85°C		
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	V_{IN}* = V_{IL} or V_{IH}; I_{OH} −24 mA
		5.5		4.86	4.70	4.76		
V_{OL}	Maximum Low Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	V_{IN}* = V_{IL} or V_{IH}; I_{OL} 24 mA
		5.5		0.36	0.50	0.44		
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH}; V_O = V_{CC}, GND
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V

*All outputs loaded; thresholds associated with output under test.

DC Electrical Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$ Typ	74ACTQ $T_A = +25°C$ Guaranteed Limits	54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{CC}	Max Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 5)
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}					50	−75	mA	$V_{OHD} = 3.85V$ Min
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	0.5	0.8			V	*Figures 2-12, 13* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.5	−0.8			V	*Figures 2-12, 13* (Notes 2, 3)
V_{OHP}	Maximum Overshoot	5.0	$V_{OH} + 1.0$	$V_{OH} + 1.5$			V	*Figures 2-12, 13* (Notes 1, 3)
V_{OHV}	Minimum V_{CC} Droop	5.0	$V_{OH} - 1.0$	$V_{OH} - 1.8$			V	*Figures 2-12, 13* (Notes 1, 3)
V_{IHD}	Minimum High Dynamic Input Voltage Level	5.0	1.7	2.0			V	(Notes 1, 4)
V_{ILD}	Maximum Low Dynamic Input Voltage Level	5.0	1.2	0.8			V	(Notes 1, 4)

†Maximum test duration 2.0 ms; one output loaded at a time.

Note 1: Worst case package.

Note 2: Maximum number of outputs that can switch simultaneously is n. (n − 1) outputs are switched LOW and one output held LOW.

Note 3: Maximum number of outputs that can switch simultaneously is n. (n − 1) outputs are switched HIGH and one output held HIGH.

Note 4: Maximum number of data inputs (n) switching. (n − 1) inputs switching 0V to 3V ('ACTQ). Input under test switching 3V to threshold (V_{ILD}).

Note 5: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF Min	Max	74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_n to B_n or B_n to A_n	5.0	3.8 3.5	5.9 5.5	8.3 7.9			3.0 2.6	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}_n$, $\overline{LEAB}_n$ to A_n, B_n	5.0	4.7 3.9	6.9 6.3	9.8 9.0			3.4 3.1	10.8 9.8	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}_n$ or $\overline{OEAB}_n$ to A_n or B_n $\overline{CEBA}_n$ or $\overline{CEAB}_n$ to A_n or B_n	5.0	4.2 4.9	6.3 7.3	9.2 10.3			3.0 3.6	9.9 10.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}_n$ or $\overline{OEAB}_n$ to A_n or B_n $\overline{CEBA}_n$ or $\overline{CEAB}_n$ to A_n or B_n	5.0	2.8 2.6	5.2 5.0	8.0 7.6			2.1 2.0	8.3 8.1	ns

*Voltage Range 5.0 is 5.0V ±0.5V.

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF		54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum			
t_S	Setup Time, HIGH or LOW A_n or B_n to $\overline{LEBA}_n$ or $\overline{LEAB}_n$	5.0		3.0		3.0	ns
t_H	Hold Time, HIGH or LOW A_n or B_n to $\overline{LEBA}_n$ or $\overline{LEAB}_n$	5.0		1.5		1.5	ns
t_W	Latch Enable, B to A Pulse Width, LOW	5.0		4.0		4.0	ns

*Voltage Range 5.0 is 5.0V ±0.5V

Extended AC Electrical Characteristics

Symbol	Parameter	74ACTQ $T_A = -40$ to $+85°C$, V_{CC} = Com, $C_L = 50$ pF, 16 Outputs Switching (Note 1)			54ACTQ T_A = Mil, V_{CC} = Mil, $C_L = 50$ pF, 16 Outputs Switching (Note 1)		74ACTQ $T_A = -40$ to $+85°C$, V_{CC} = Com, $C_L = 250$ pF (Note 2)		54ACTQ T_A = Mil, V_{CC} = Mil, $C_L = 250$ pF (Note 2)		Units
		Min	Typ	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_n to B_n or B_n to A_n	4.5 3.7		11.1 9.6			5.8 5.1	14.3 13.4			ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}_n$, $\overline{LEAB}_n$ to A_n, B_n	4.3 3.7		11.3 9.7			6.2 5.8	16.3 14.9			ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}_n$ or $\overline{OEAB}_n$ to A_n or B_n $\overline{CEBA}_n$ or $\overline{CEAB}_n$ to A_n or B_n	4.0 4.3		10.7 11.3			(Note 3)		(Note 3)		ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}_n$ or $\overline{OEAB}_n$ to A_n or B_n $\overline{CEBA}_n$ or $\overline{CEAB}_n$ to A_n or B_n	3.0 2.8		8.0 7.6			(Note 4)		(Note 4)		ns
t_{OSHL} (Note 5)	Pin to Pin Skew HL Data to Output			1.1							ns
t_{OSLH} (Note 5)	Pin to Pin Skew LH Data to Output			1.4							ns
t_{OSHL} (Note 5)	Pin to Pin Skew Latch to Output			2.6							ns
t_{OSLH} (Note 5)	Pin to Pin Skew Latch to Output			1.0							ns
t_{OST} (Note 5)	Pin to Pin Skew Data to Output			1.0							ns
t_{OST} (Note 5)	Pin to Pin Skew Latch to Output			2.2							ns

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 3: TRI-STATE delays are load dominated and have been excluded from the datasheet.

Note 4: The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Note 5: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}).

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	95.0	pF	V_{CC} = 5.0V

FACT Noise Characteristics

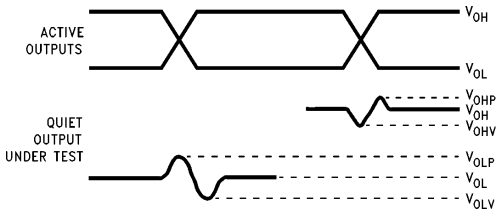
The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator
PC-163A Test Fixture
Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set V_{CC} to 5.0V



TL/F/10967–5

FIGURE 1. Quiet Output Noise Voltage Waveforms

Note A. V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B. Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

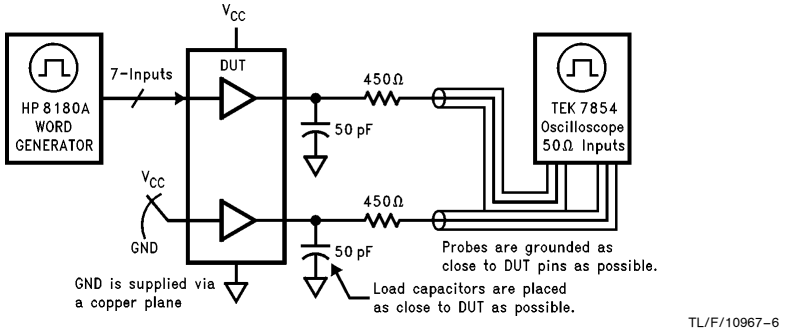
5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.
6. Set the word generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with a digital volt meter.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the HL transition. Measure V_{OHP} and V_{OHV} on the quiet output during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

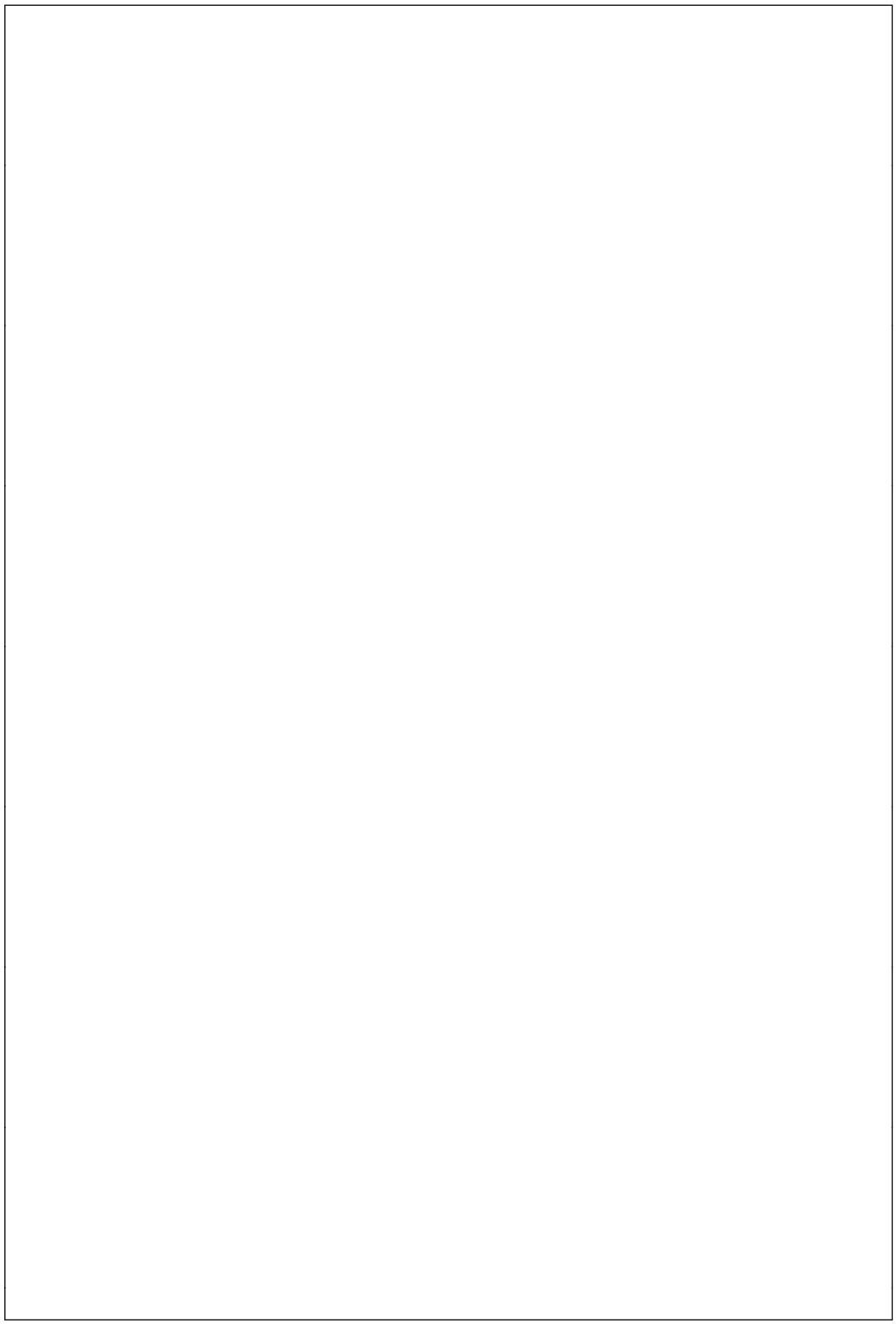
V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next increase the input HIGH voltage level on the word generator, V_{IH} until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability on the measurements.



TL/F/10967–6

FIGURE 2. Simultaneous Switching Test Circuit



Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74ACTQ 16543 SS C X

Temperature Range Family
74ACTQ = Commercial—TTL Compatible
54ACTQ = Military—TTL Compatible

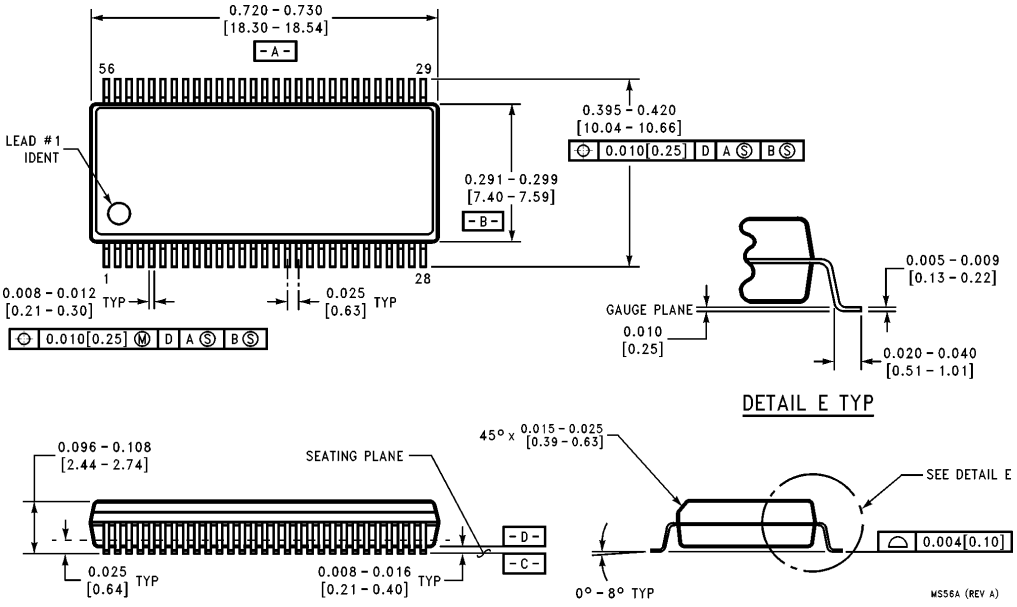
Device Type

Package Code
SS = Small Outline (SSOP)
F = CERPAK

Temperature Range
C = Commercial (−40°C to +85°C)
M = Military (−55°C to +125°C)

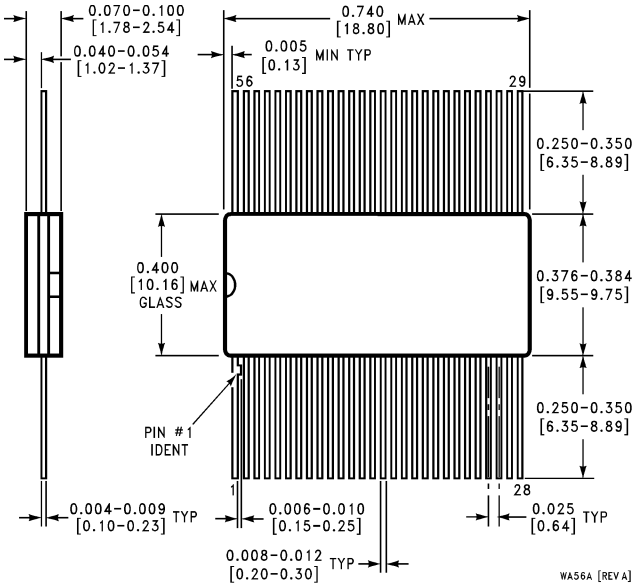
Special Variations
X = Devices shipped in 13″ reels
QB = 883 Processing

Physical Dimensions inches (millimeters)



56-Lead SSOP (0.300″ Wide) (SS)
NS Package Number MS56A

Physical Dimensions inches (millimeters) (Continued)



56-Lead CERPAK (F)
NS Package Number WA56A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998