MOTOROLA

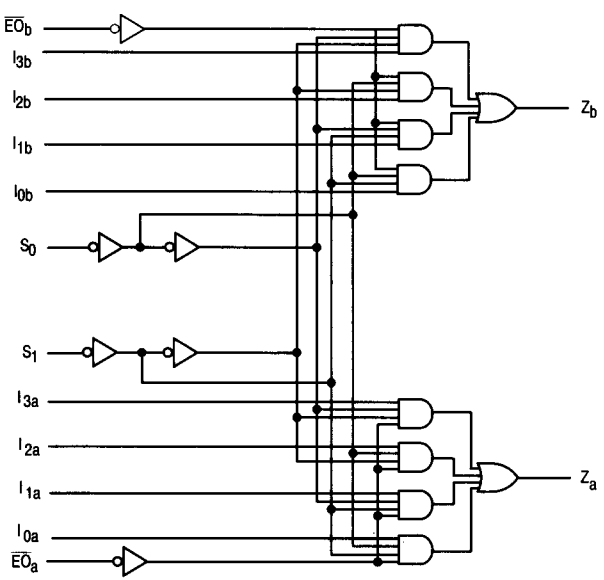
Dual 4-Input Data Selector/Multiplexer (3-State Output With Enable)

ELECTRICALLY TESTED PER:
MIL-M-38510/30908

The 54LS253 is a Dual 4-input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{EO}$) input, allowing the outputs to interface directly with bus oriented systems. The 'LS253 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Multifunction Capability
- Non-Inverting 3-State Outputs
- Schottky Process For High-Speed
- Input Clamp Diodes Limit High-Speed Termination Effects

LOGIC DIAGRAM



Military 54LS253

AVAILABLE AS:

1) JAN: JM38510/30908BXA
2) SMD: 7601701
3) 883: 54LS253/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
$\overline{EO}_a$	1	1	2	V_{CC}
S_1	2	2	3	V_{CC}
I_{3a}	3	3	4	V_{CC}
I_{2a}	4	4	5	V_{CC}
I_{1a}	5	5	7	V_{CC}
I_{0a}	6	6	8	V_{CC}
Z_a	7	7	9	V_{CC}
GND	8	8	10	GND
Z_b	9	9	12	V_{CC}
I_{0b}	10	10	13	V_{CC}
I_{1b}	11	11	14	V_{CC}
I_{2b}	12	12	15	V_{CC}
I_{3b}	13	13	17	V_{CC}
S_0	14	14	18	V_{CC}
$\overline{EO}_b$	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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FUNCTIONAL DESCRIPTION

The 'LS253 contains two identical 4-input Multiplexers with 3-state outputs. They select two bits of data from four sources selected by common select inputs (S_0, S_1). The 4-input multiplexers have identical Output Enable ($\overline{EO}_a$, $\overline{EO}_b$) inputs which when HIGH, forces the outputs to a high impedance (high Z) state.

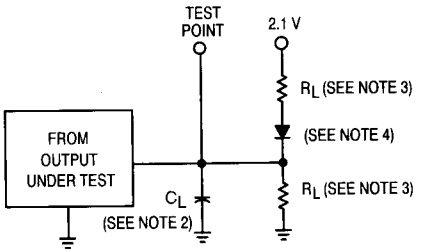
The 'LS253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{EO}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$Z_b = \overline{EO}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{0b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

LOAD CIRCUIT FOR 3-STATE OUTPUT



NOTES:

1. Input pulse characteristics: PRR ≤ 1.0 MHz, t_r = 15 ns, t_f ≤6.0 ns.
2. C_L = 50 pF ± 10% for t_{PLH}, t_{PHL}, t_{PZL} and t_{PZH} tests, C_L = 15 pF minimum for t_{PHZ} and t_{PLZ} tests. C_L includes scope probe, wiring and stray capacitance.
3. R_L = 2.0 kΩ ± 5.0%.
4. All diodes are 1N3064 or 1N916.
5. The limits specified for C_L = 15 pF and C_L = 5.0 pF are guaranteed but not tested.

TRUTH TABLE

Select Inputs		Output Enable	Data Inputs				Output
S_0	S_1	$\overline{EO}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	(Z)
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z) = High Impedance (Off)
Address inputs S_0 and S_1 are common to both sections

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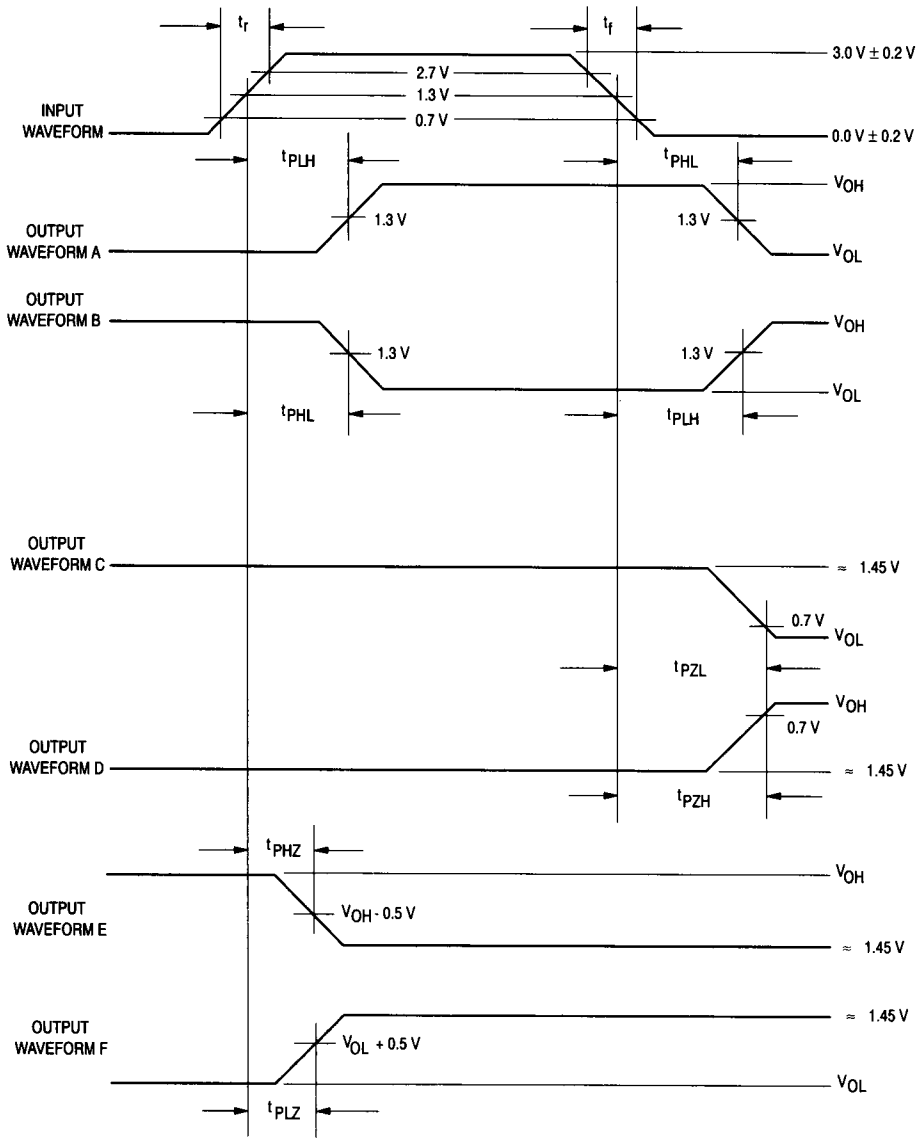
WAVEFORMS



SWITCH POSITIONS

Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = – 1.0 mA, V_{IH} = 2.0 V, other inputs are open, S = 0.7 V, $\overline{EO}$ = 0.7 V.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IL} = 0.7 V, S = 2.0 V, $\overline{EO}$ = 2.0 V, all other inputs are open.
V_{IC}	Input Clamping Voltage		– 1.5					V	V_{CC} = 4.5 V, I_{IN} = – 18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open, S = 2.7 V, 5.5 V or GND.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open, S = 5.5 V or GND.
$I_{IL(E)}$	Logical "0" Input Current	– 0.16	– 0.4	– 0.16	– 0.4	– 0.16	– 0.4	mA	V_{CC} = 5.5 V, $\overline{EO}$ = 0.4 V, other inputs are open.
$I_{IL(S)}$	Logical "0" Input Current	– 0.12	– 0.36	– 0.12	– 0.36	– 0.12	– 0.36	mA	V_{CC} = 5.5 V, S = 0.4 V, other inputs are open.
I_{IL}	Logical "0" Input Current	– 0.16	– 0.4	– 0.16	– 0.4	– 0.16	– 0.4	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open, $\overline{EO}$ = GND, S = 5.5 V or GND.
I_{OS}	Output Short Circuit Current	– 15	– 100	– 15	– 100	– 15	– 100	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, all other inputs are GND, V_{OUT} = GND.
I_{OZH}	Output Off Current High		20		20		20	µA	V_{CC} = 5.5 V, V_{IN} = 0.7 V, all other inputs are open, V_{OUT} = 2.7 V, $\overline{EO}$ = 2.0 V, S = 0.7 V.
I_{OZL}	Output Off Current Low		– 20		– 20		– 20	µA	V_{CC} = 5.5 V, V_{IN} = 2.0 V, all other inputs are open, V_{OUT} = 0.4 V, $\overline{EO}$ & S = 2.0 V.
I_{CCH}	Power Supply Current		14		14		14	mA	V_{CC} = 5.5 V, $\overline{EO}$ = 5.5 V, all other inputs are GND.
I_{CCL}	Power Supply Current		12		12		12	mA	V_{CC} = 5.5 V, all inputs are GND.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.4 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output Output High-Low	3.0 —	25 20	3.0 —	38 33	3.0 —	38 33	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output Output Low-High	3.0	30 25	3.0 —	45 40	3.0 —	45 40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PHL5} t_{PHL5}	Propagation Delay /Data-Output Output High-Low	3.0	37 32	3.0 —	56 51	3.0 —	56 51	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PLH5} t_{PLH5}	Propagation Delay /Data-Output Output Low-High	3.0	50 45	3.0 —	75 70	3.0 —	75 70	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PZH3} t_{PZH3}	Propagation Delay /Data-Output Output High-Low	3.0	46 28	3.0 —	69 64	3.0 —	69 64	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PZL3} t_{PZL3}	Propagation Delay /Data-Output Output Low-High	3.0	28 23	3.0 —	42 47	3.0 —	42 47	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PHZ3} t_{PHZ3}	Propagation Delay /Data-Output Output High-Low	3.0	46 41	3.0 —	69 64	3.0 —	69 64	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 5.0 pF, R_L = 667Ω.
t_{PLZ3} t_{PLZ3}	Propagation Delay /Data-Output Output Low-High	3.0	32 27	3.0 —	48 43	3.0 —	48 43	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 5.0 pF, R_L = 667 Ω.

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