Data Sheet June 2004 FN6089

# Low-Voltage, Single and Dual Supply, Quad SPST, High Performance Analog Switch

The Intersil ISL43144R5172 device is a CMOS, precision, bidirectional, quad SPST analog switch designed to operate from a single +2V to +12V supply or from a dual ±2V to ±6V supplies.

Targeted applications include equipment / systems that require an operating temperature up to 105°C. At 105°C using a single 5V supply, Ron is at most 55Ω and leakage currents are only 9nA max. The part has fast switching speeds at 105°C, $t_{ON}$ = 110ns and $t_{OFF}$ = 65ns.

The ISL43144R5172 is a quad single-pole/single-throw (SPST) device. It has four normally open (NO) switches, each with a separate logic control pin.

The ISL43144R5172 is specified for an operating temperature range of -40°C to 105°C. Users requiring a temperature range of -40°C to 85°C should consider using the ISL43144 device.

Table 1 summarizes the performance of this family. Specifications shown in the table are typical values at 25°C.

**TABLE 1. FEATURES AT A GLANCE**

| | ISL43144 |
|---|---|
| Number of Switches | 4 |
| Configuration | SPST (All NO) |
| ±4.5V $R_{ON}$ | 18Ω |
| ±4.5V $t_{ON}/t_{OFF}$ | 52ns/40ns |
| 10.8V $R_{ON}$ | 14Ω |
| 10.8V $t_{ON}/t_{OFF}$ | 40ns/27ns |
| 4.5V $R_{ON}$ | 30Ω |
| 4.5V $t_{ON}/t_{OFF}$ | 64ns/29ns |
| 3V $R_{ON}$ | 51Ω |
| 3V $t_{ON}/t_{OFF}$ | 120ns/50ns |
| Package | 16 Ld TSSOP |

## Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- AN557 “Recommended Test Procedures for Analog Switches”

## Features

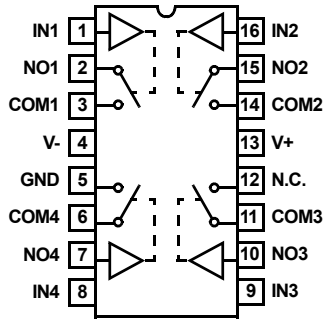
- Temperature Range -40°C to 105°C
- Fully Specified for 10% Tolerances for Single 5V and Dual ±5V Supplies
- Four Separately Controlled SPST Switches
- ON Resistance ($R_{ON}$ Max at 105°C)
  - Single 5V Supply . . . . . 55Ω
  - Dual ±5V Supplies . . . . . 35Ω
- $R_{ON}$ Matching Between Channels (Max at 105°C) . . . . . 4Ω
- Low Off Leakage Current (Max at 105°C) . . . . . 8nA
- Fast Switching Action (Single 5V Supply at 105°C)
  - $t_{ON}$ . . . . . 110ns
  - $t_{OFF}$ . . . . . 65ns
- Minimum 2000V ESD Protection per Method 3015.7
- TTL, CMOS Compatible
- Pin Compatible with DG412

## Applications

- Battery Powered, Handheld, and Portable Equipment
  - Barcode Scanners
  - Laptops, Notebooks, Palmtops
- Communications Systems
  - Radios
  - XDSL and PBX / PABX
  - RF “Tee” Switches
  - Base Stations
- Test Equipment
  - Medical Ultrasound
  - Electrocardiograph
  - ATE
- Audio and Video Switching
- General Purpose Circuits
  - +3V/+5V DACs and ADCs
  - Digital Filters
  - Operational Amplifier Gain Switching Networks
  - High Frequency Analog Switching
  - High Speed Multiplexing

## Pinout (Note 1)

**ISL43144R5172 (TSSOP)**
TOP VIEW




NOTE:

1. Switches Shown for Logic “0” Input.

## Truth Table

| LOGIC | ISL43144R5172 |
|---|---|
| | SW 1, 2, 3, 4 |
| 0 | OFF |
| 1 | ON |

NOTE: Logic “0” ≤ 0.8V. Logic “1” ≥ 2.4V.

## Pin Descriptions

| PIN | FUNCTION |
|---|---|
| V+ | Positive Power Supply Input |
| V- | Negative Power Supply Input. Connect to GND for Single Supply Configurations. |
| GND | Ground Connection |
| IN | Digital Control Input |
| COM | Analog Switch Common Pin |
| NO | Analog Switch Normally Open Pin |
| N.C. | No Internal Connection |

## Ordering Information

| PART NO. | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|---|---|---|---|
| ISL43144IVR5172 | -40 to 85 | 16 Ld TSSOP | M16.173 |
| ISL43144IV-TR5172 | -40 to 85 | 16 Ld TSSOP Tape & Reel | M16.173 |

## Absolute Maximum Ratings

V+ to V- . . . . . -0.3 to15V
V+ to GND . . . . . -0.3 to15V
V- to GND. . . . . -15 to 0.3V
All Other Pins (Note 2). . . . . ((V-) - 0.3V) to ((V+) + 0.3V)
Continuous Current (Any Terminal) . . . . . 30mA
Peak Current, IN, NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . 100mA
ESD Rating (Per MIL-STD-883 Method 3015). . . . . .>2kV

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) |
|---|---|
| 16 Ld TSSOP Package (Note 3) . . . . . | 150 |

Maximum Junction Temperature (Plastic Package). . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

## Operating Conditions

Temperature Range . . . . . -40°C to 105°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

2. Signals on NC, NO, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. $\theta_{JA}$ is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

**Electrical Specifications: 5V Supply** Test Conditions: $V_{SUPPLY}$ = +4.5V to +5.5V, V- = GND = 0V, $V_{INH}$ = 2.4V, $V_{INL}$ = 0.8V (Note 4), Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | TEMP (°C) | (NOTE 5) MIN | TYP | (NOTE 5) MAX | UNITS |
|---|---|---|---|---|---|---|
| **ANALOG SWITCH CHARACTERISTICS** | | | | | | |
| Analog Signal Range, $V_{ANALOG}$ | | Full | 0 | - | V+ | V |
| ON Resistance, $R_{ON}$ | V+ = 4.5V, $I_{COM}$ = 1.0mA, $V_{NO}$ or $V_{NC}$ = 3.5V (See Figure 4, Note 9) | 25 | - | 30 | 40 | Ω |
| | | Full | - | - | 55 | Ω |
| $R_{ON}$ Matching Between Channels, $\Delta R_{ON}$ | V+ = 4.5V, $I_{COM}$ = 1.0mA, $V_{NO}$ or $V_{NC}$ = 3V (Note 9) | 25 | - | 0.5 | 3 | Ω |
| | | Full | - | - | 4 | Ω |
| $R_{ON}$ Flatness, $R_{FLAT(ON)}$ | V+ = 5.5V, $I_{COM}$ = 1.0mA, $V_{NO}$ or $V_{NC}$ = 1V, 2V, 3V (Notes 7, 9) | 25 | - | 4.4 | 6 | Ω |
| | | Full | - | - | 9 | Ω |
| NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$ | V+ = 5.5V, $V_{COM}$ = 1V, 4.5V, $V_{NO}$ or $V_{NC}$ = 4.5V, 1V (Note 6) | 25 | -0.1 | - | 0.1 | nA |
| | | Full | -8 | - | 8 | nA |
| COM OFF Leakage Current, $I_{COM(OFF)}$ | V+ = 5.5V, $V_{COM}$ = 1V, 4.5V, $V_{NO}$ or $V_{NC}$ = 4.5V, 1V (Note 6) | 25 | -0.1 | - | 0.1 | nA |
| | | Full | -8 | - | 8 | nA |
| COM ON Leakage Current, $I_{COM(ON)}$ | V+ = 5.5V, $V_{COM}$ = $V_{NO}$ or $V_{NC}$ = 1V, 4.5V (Note 6) | 25 | -0.2 | - | 0.2 | nA |
| | | Full | -9 | - | 9 | nA |
| **DIGITAL INPUT CHARACTERISTICS** | | | | | | |
| Input Voltage High, $V_{INH}$ | (Note 9) | Full | 2.4 | - | - | V |
| Input Voltage Low, $V_{INL}$ | (Note 9) | Full | - | - | 0.8 | V |
| Input Current, $I_{INH}$, $I_{INL}$ | $V_S$ = 5.5V, $V_{IN}$ = 0V or V+ (Note 9) | Full | -1 | - | 1 | µA |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Turn-ON Time, $t_{ON}$ | V+ = 4.5V, $V_{NO}$ or $V_{NC}$ = 3V, $R_L$ = 300Ω, $C_L$ = 35pF, $V_{IN}$ = 0 to 3V (See Figure 1, Note 10) | 25 | - | 64 | 80 | ns |
| | | Full | - | - | 110 | ns |
| Turn-OFF Time, $t_{OFF}$ | V+ = 4.5V, $V_{NO}$ or $V_{NC}$ = 3V, $R_L$ = 300Ω, $C_L$ = 35pF, $V_{IN}$ = 0 to 3V (See Figure 1, Note 10) | 25 | - | 29 | 40 | ns |
| | | Full | - | - | 65 | ns |
| Charge Injection, Q | $C_L$ = 1.0nF, $V_G$ = 0V, $R_G$ = 0Ω (See Figure 2) | 25 | - | 1.2 | - | pC |
| NO or NC OFF Capacitance, $C_{OFF}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (See Figure 6) | 25 | - | 10 | - | pF |
| COM OFF Capacitance, $C_{COM(OFF)}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (See Figure 6) | 25 | - | 26 | - | pF |
| COM ON Capacitance, $C_{COM(ON)}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (See Figure 6) | 25 | - | 34 | - | pF |
| OFF Isolation | $R_L$ = 50Ω, $C_L$ = 15pF, f = 1MHz, $V_{NO}$ or $V_{NC}$ = $1V_{RMS}$ (See Figures 3, 5) | 25 | - | 71 | - | dB |
| Crosstalk, Note 9 | | 25 | - | -89 | - | dB |
| Power Supply Rejection Ratio | $R_L$ = 50Ω, $C_L$ = 5pF, f = 1MHz | 25 | - | 58 | - | dB |

**Electrical Specifications: 5V Supply** Test Conditions: $V_{SUPPLY}$ = +4.5V to +5.5V, V- = GND = 0V, $V_{INH}$ = 2.4V, $V_{INL}$ = 0.8V (Note 4), Unless Otherwise Specified **(Continued)**

| PARAMETER | TEST CONDITIONS | TEMP (°C) | (NOTE 5) MIN | TYP | (NOTE 5) MAX | UNITS |
|---|---|---|---|---|---|---|
| **POWER SUPPLY CHARACTERISTICS** | | | | | | |
| Power Supply Range | (Note 10) | Full | 2 | - | 12 | V |
| Positive Supply Current, I+ | V+ = 5.5V, $V_{IN}$ = 0V or V+, Switch On or Off (Note 9) | 25 | -1 | 0.01 | 1 | µA |
| | | Full | -1.5 | - | 1.5 | µA |
| Negative Supply Current, I- | | 25 | -1 | 0.01 | 1 | µA |
| | | Full | -1.5 | - | 1.5 | µA |

NOTES:

4. $V_{IN}$ = Input voltage to perform proper function.
5. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Leakage parameter is 100% tested at 85°C, and guaranteed by correlation at 105°C and 25°C.
7. Flatness is defined as the delta between the maximum and minimum $R_{ON}$ values over the specified voltage range.
8. Between any two switches.
9. Tested at 25°C and 85°C and guaranteed by design across the full temperature range.
10. Guaranteed by design.

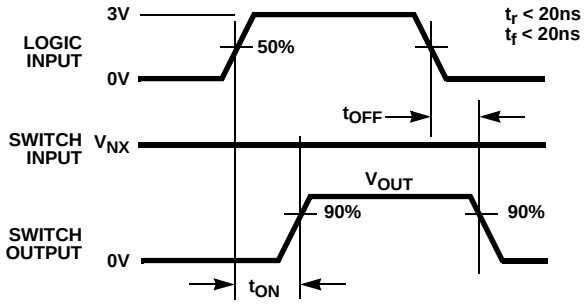
**Electrical Specifications: ±5V Supply** Test Conditions: $V_{SUPPLY}$ = ±4.5V to ±5.5V, GND = 0V, $V_{INH}$ = 2.4V, $V_{INL}$ = 0.8V (Note 4), Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (NOTE 5) | TYP | MAX (NOTE 5) | UNITS |
|---|---|---|---|---|---|---|
| **ANALOG SWITCH CHARACTERISTICS** | | | | | | |
| Analog Signal Range, $V_{ANALOG}$ | | Full | V- | - | V+ | V |
| ON Resistance, $R_{ON}$ | $V_S$ = ±4.5V, $I_{COM}$ = 10mA, $V_{NO}$ or $V_{NC}$ = ±3.5V (See Figure 4, Note 9) | 25 | - | 18 | 25 | Ω |
| | | Full | - | - | 35 | Ω |
| $R_{ON}$ Matching Between Channels, $\Delta R_{ON}$ | $V_S$ = ±4.5V, $I_{COM}$ = 10mA, $V_{NO}$ or $V_{NC}$ = ±3V (Note 9) | 25 | - | 0.5 | 2 | Ω |
| | | Full | - | - | 4 | Ω |
| $R_{ON}$ Flatness, $R_{FLAT(ON)}$ | $V_S$ = ±4.5V, $I_{COM}$ = 10mA, $V_{NO}$ or $V_{NC}$ = 0V, ±3V, (Notes 7, 9) | 25 | - | - | 5 | Ω |
| | | Full | - | - | 6 | Ω |
| NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$ | $V_S$ = ±5.5V, $V_{COM}$ = ±4.5V, $V_{NO}$ or $V_{NC}$ = $\overline{+}$4.5V, (Note 6) | 25 | -0.1 | - | 0.1 | nA |
| | | Full | -15 | - | 15 | nA |
| COM OFF Leakage Current, $I_{COM(OFF)}$ | $V_S$ = ±5.5V, $V_{COM}$ = ±4.5V, $V_{NO}$ or $V_{NC}$ = $\overline{+}$4.5V, (Note 6) | 25 | -0.1 | - | 0.1 | nA |
| | | Full | -15 | - | 15 | nA |
| COM ON Leakage Current, $I_{COM(ON)}$ | $V_S$ = ±5.5V, $V_{COM}$ = $V_{NO}$ or $V_{NC}$ = ±4.5V (Note 6) | 25 | -0.2 | - | 0.2 | nA |
| | | Full | -20 | - | 20 | nA |
| **DIGITAL INPUT CHARACTERISTICS** | | | | | | |
| Input Voltage High, $V_{INH}$ | (Note 9) | Full | 2.4 | - | - | V |
| Input Voltage Low, $V_{INL}$ | (Note 9) | Full | - | - | 0.8 | V |
| Input Current, $I_{INH}$, $I_{INL}$ | $V_S$ = ±5.5V, $V_{IN}$ = 0V or V+ (Note 9) | Full | -1 | - | 1 | µA |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Turn-ON Time, $t_{ON}$ | $V_S$ = ±4.5V, $V_{NO}$ or $V_{NC}$ = ±3V, $R_L$ = 300Ω, $C_L$ = 35pF, $V_{IN}$ = 0 to 3V (See Figure 1, Note 10) | 25 | - | 52 | 65 | ns |
| | | Full | - | - | 95 | ns |
| Turn-OFF Time, $t_{OFF}$ | $V_S$ = ±4.5V, $V_{NO}$ or $V_{NC}$ = ±3V, $R_L$ = 300Ω, $C_L$ = 35pF, $V_{IN}$ = 0 to 3V (See Figure 1, Note 10) | 25 | - | 40 | 50 | ns |
| | | Full | - | - | 75 | ns |
| Charge Injection, Q | $C_L$ = 1.0nF, $V_G$ = 0V, $R_G$ = 0Ω (See Figure 2) | 25 | - | 4 | - | pC |
| NO or NC OFF Capacitance, $C_{OFF}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (See Figure 6) | 25 | - | 10 | - | pF |
| COM OFF Capacitance, $C_{COM(OFF)}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (See Figure 6) | 25 | - | 26 | - | pF |

**Electrical Specifications: ±5V Supply** Test Conditions: $V_{SUPPLY}$ = ±4.5V to ±5.5V, GND = 0V, $V_{INH}$ = 2.4V, $V_{INL}$ = 0.8V (Note 4), Unless Otherwise Specified **(Continued)**

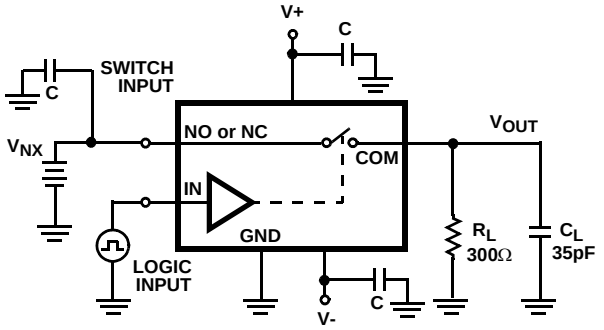
| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (NOTE 5) | TYP | MAX (NOTE 5) | UNITS |
|---|---|---|---|---|---|---|
| COM ON Capacitance, $C_{COM(ON)}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (See Figure 6) | 25 | - | 34 | - | pF |
| OFF Isolation | $R_L$ = 50Ω, $C_L$ = 15pF, f = 1MHz, $V_{NO}$ or $V_{NC}$ = $1V_{RMS}$ (See Figures 3 and 5) | 25 | - | 71 | - | dB |
| Crosstalk (Note 9) | | 25 | - | -89 | - | dB |
| Power Supply Rejection Ratio | $R_L$ = 50Ω, $C_L$ = 5pF, f = 1MHz | 25 | - | 58 | - | dB |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | |
| Power Supply Range | Note 10 | Full | ±2 | - | ±6 | V |
| Positive Supply Current, I+ | $V_S$ = ±5.5V, $V_{IN}$ = 0V or V+, Switch On or Off (Note 9) | 25 | -1 | 0.01 | 1 | µA |
| | | Full | -1.5 | - | 1.5 | µA |
| Negative Supply Current, I- | | 25 | -1 | 0.01 | 1 | µA |
| | | Full | -1.5 | - | 1.5 | µA |

## *Test Circuits and Waveforms*




Logic input waveform is inverted for switches that have the opposite logic sense.

**FIGURE 1A. MEASUREMENT POINTS**

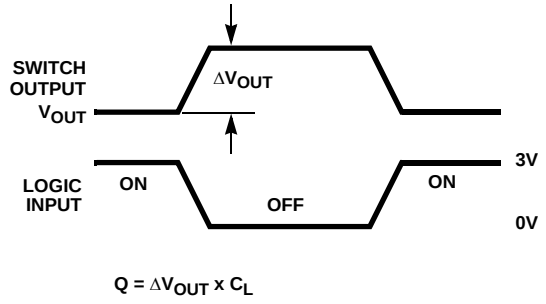



Repeat test for all switches. $C_L$ includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

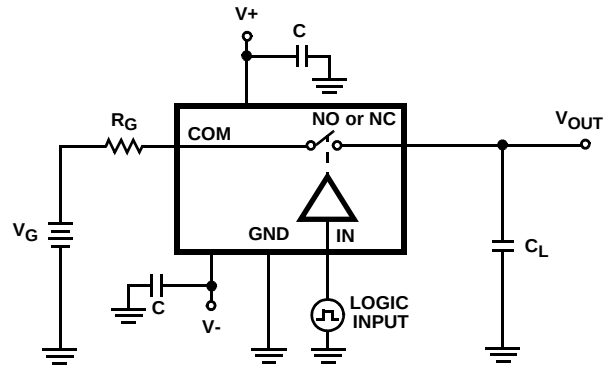
**FIGURE 1B. TEST CIRCUIT**

**FIGURE 1. SWITCHING TIMES**




Logic input waveform is inverted for switches that have the opposite logic sense.

**FIGURE 2A. MEASUREMENT POINTS**

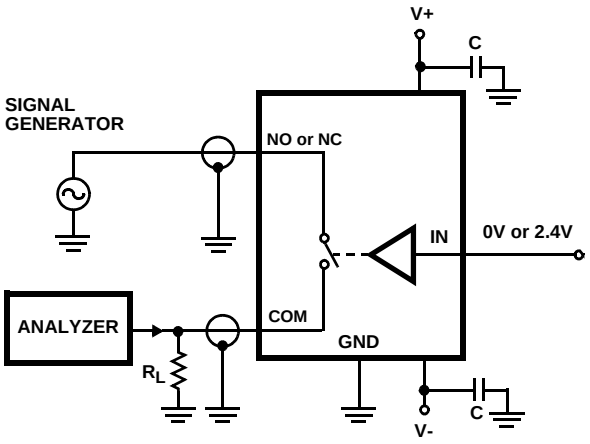



Repeat test for all switches. $C_L$ includes fixture and stray capacitance.

**FIGURE 2B. TEST CIRCUIT**

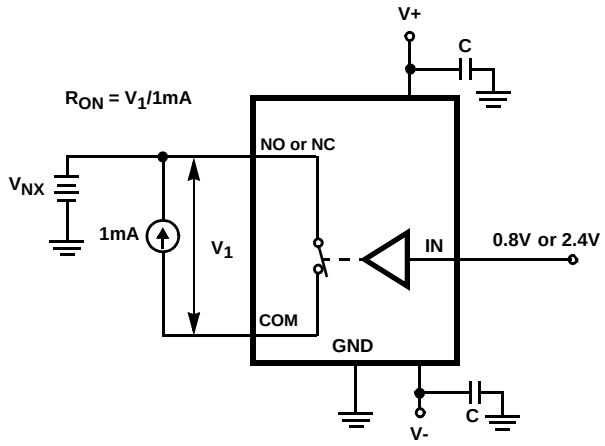
**FIGURE 2. CHARGE INJECTION**

## Test Circuits and Waveforms (Continued)




Repeat test for all switches.

FIGURE 3. OFF ISOLATION TEST CIRCUIT




Repeat test for all switches.

FIGURE 4. $R_{ON}$ TEST CIRCUIT

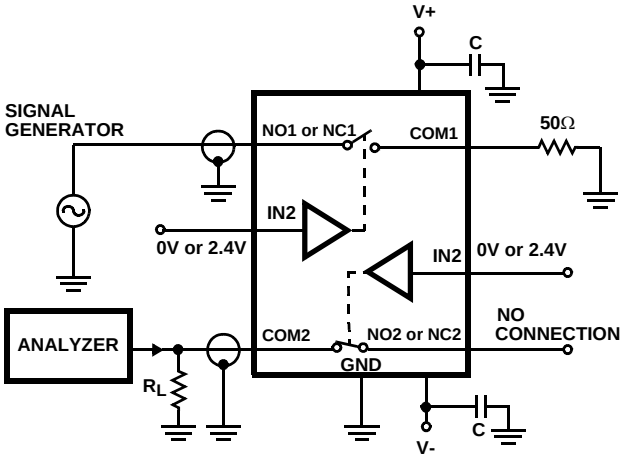



FIGURE 5. CROSSTALK TEST CIRCUIT

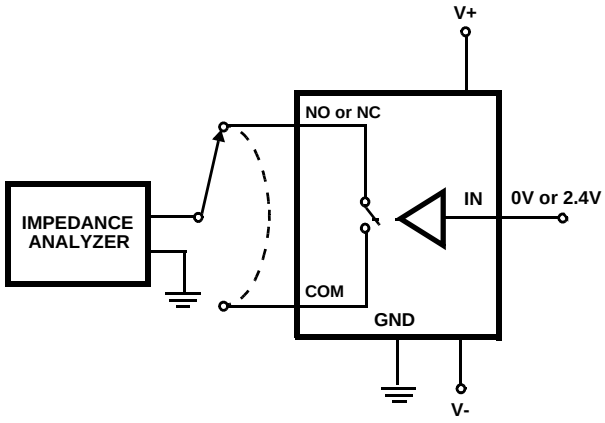



FIGURE 6. CAPACITANCE TEST CIRCUIT

## Detailed Description

The ISL43144R5172 quad SPST analog switch offers precise switching capability from a bipolar ±2V to ±6V or a single 2V to 12V supply. The device offers low on-resistance (30Ω) and high speed switching ($t_{ON}$ = 64ns, $t_{OFF}$ = 29ns) when using a single +5V supply. The device is especially well suited for portable battery powered equipment thanks to the low operating supply voltage (2V), low power consumption (1μW), and low leakage currents (9nA max). High frequency applications also benefit from the wide bandwidth, and the very high OFF isolation and crosstalk rejection.

### Supply Sequencing and Overvoltage Protection

As with any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to V- (see Figure 7). To prevent forward biasing these diodes, V+ and V- must be applied before any input signals, and input signal voltages must remain between V+ and V-. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed:

1. Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 7). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.
2. Adding a series resistor to the switch input defeats the purpose of using a low $R_{ON}$ switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 7). These additional diodes limit the analog signal from 1V below V+ to 1V above V-. The low leakage current

performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

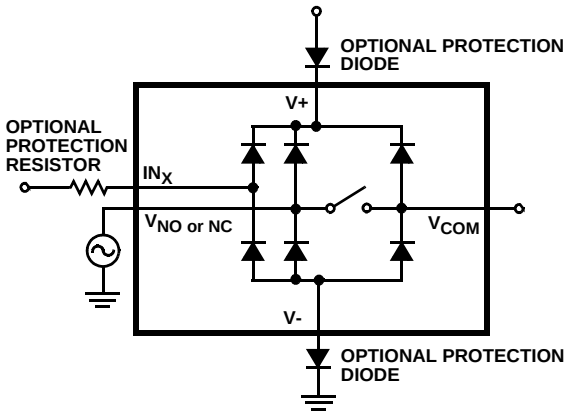



**FIGURE 7. OVERVOLTAGE PROTECTION**

### *Power-Supply Considerations*

The ISL43144R5172 construction is typical of most CMOS analog switches, in that it has three supply pins: V+, V-, and GND. V+ and V- drive the internal CMOS switches and set their analog voltage limits, so there are no connections between the analog signal path and GND. Unlike switches with a 13V maximum supply voltage, the ISL43144R5172 15V maximum supply voltage provides plenty of room for the 10% tolerance of 12V supplies (±6V or 12V single supply), as well as room for overshoot and noise spikes.

This family of switches performs equally well when operated with bipolar or single voltage supplies, and bipolar supplies need not be symmetrical. The minimum recommended supply voltage is 2V or ±2V. It is important to note that the input signal range, switching times, and ON-resistance degrade at lower supply voltages. Refer to the electrical specification tables and *Typical Performance Curves* for details.

V+ and GND power the internal logic (thus setting the digital switching point) and level shifters. The level shifters convert the logic levels to switched V+ and V- signals to drive the analog switch gate terminals, so switch parameters, especially $R_{ON}$, are strong functions of both supplies.

### *Logic-Level Thresholds*

V+ and GND power the internal logic stages, so V- has no affect on logic thresholds. This switch family is TTL compatible (0.8V and 2.4V) over a V+ supply range of 2.5V to 10V (see Figure 16). At 12V the $V_{IH}$ level is about 2.8V, so for best results use a logic family that provides a $V_{OH}$ greater than 3V.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails (see Figure 17). Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation. The ISL43144R5172 switch had been designed to minimize the supply current whenever the digital input voltage is not driven to the supply rails (0V to V+). For example, driving the device with 3V logic while operating with dual or single 5V supplies the device draws only 10µA of current (see Figure 17 for $V_{IN}$ = 3V). Similar devices of competitors can draw 8 times this amount of current.

### *High-Frequency Performance*

In 50Ω systems, signal response is reasonably flat even past 200MHz (see Figure 18). Figure 18 also illustrates that the frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An off switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch's input to its output. OFF Isolation is the resistance to this feedthrough, while Crosstalk indicates the amount of feedthrough from one switch to another. Figure 19 details the high OFF Isolation and Crosstalk rejection provided by this family. At 10MHz, OFF isolation is about 50dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease OFF Isolation and Crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

### *Leakage Considerations*

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and V-. One of these diodes conducts if any analog signal exceeds V+ or V-.

Virtually all the analog leakage current comes from the ESD diodes to V+ or V-. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and GND.

## Typical Performance Curves $T_A$ = 25°C, Unless Otherwise Specified

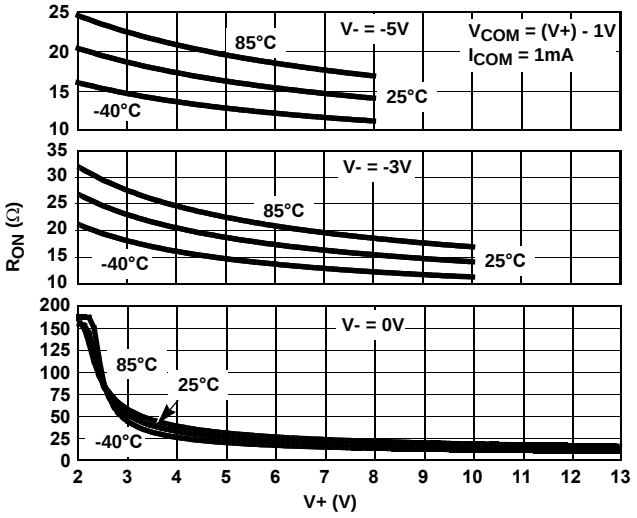



FIGURE 8. ON RESISTANCE vs POSITIVE SUPPLY VOLTAGE

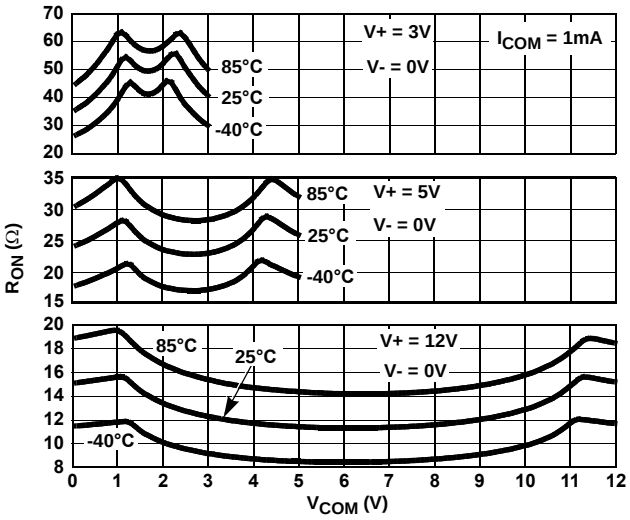



FIGURE 9. ON RESISTANCE vs SWITCH VOLTAGE

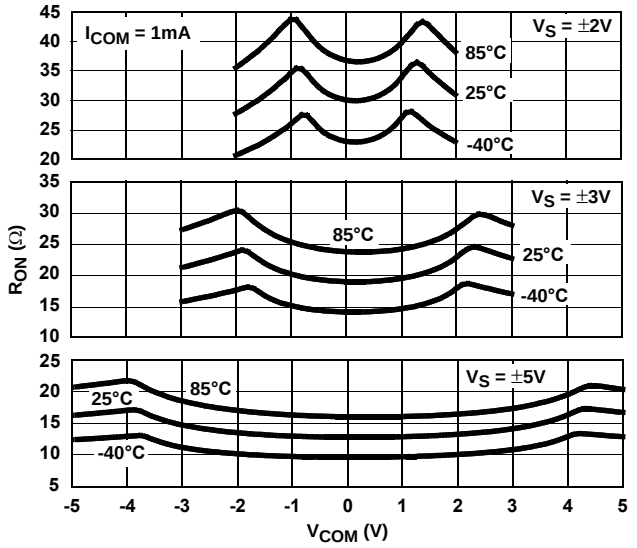



FIGURE 10. ON RESISTANCE vs SWITCH VOLTAGE

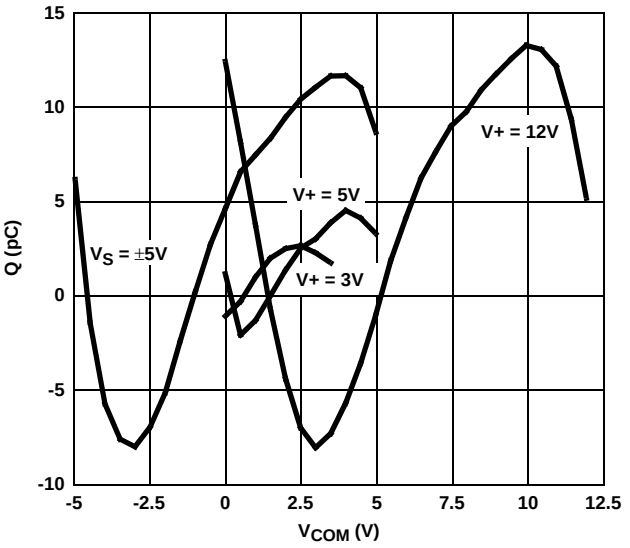



FIGURE 11. CHARGE INJECTION vs SWITCH VOLTAGE

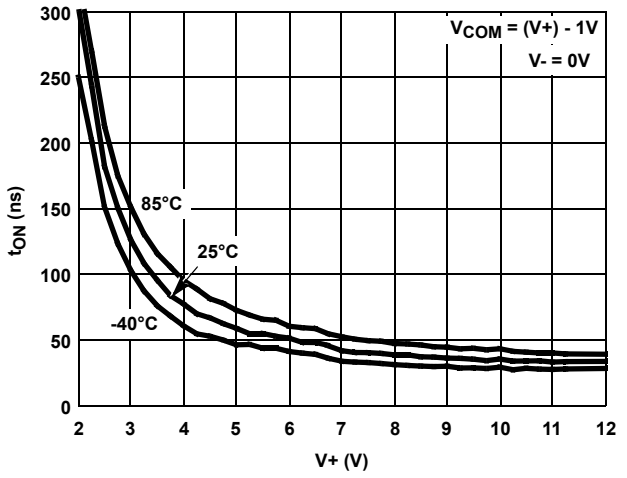



FIGURE 12. TURN - ON TIME vs POSITIVE SUPPLY VOLTAGE

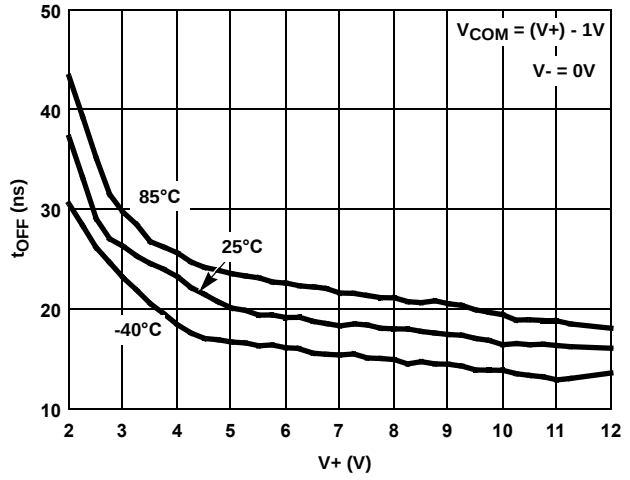



FIGURE 13. TURN - OFF TIME vs POSITIVE SUPPLY VOLTAGE

## Typical Performance Curves $T_A$ = 25°C, Unless Otherwise Specified **(Continued)**

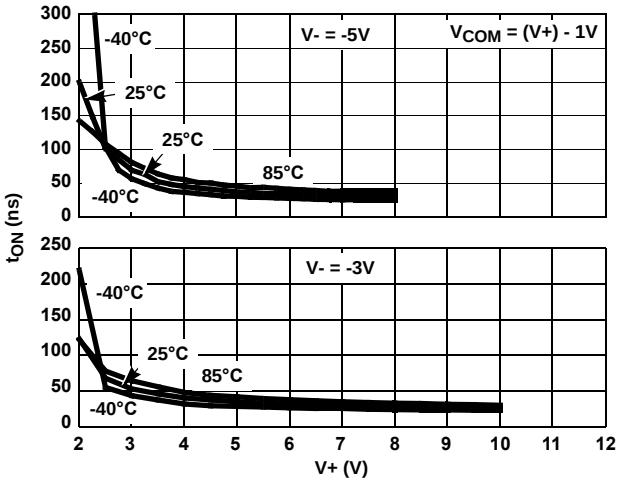



FIGURE 14. TURN - ON TIME vs POSITIVE SUPPLY VOLTAGE

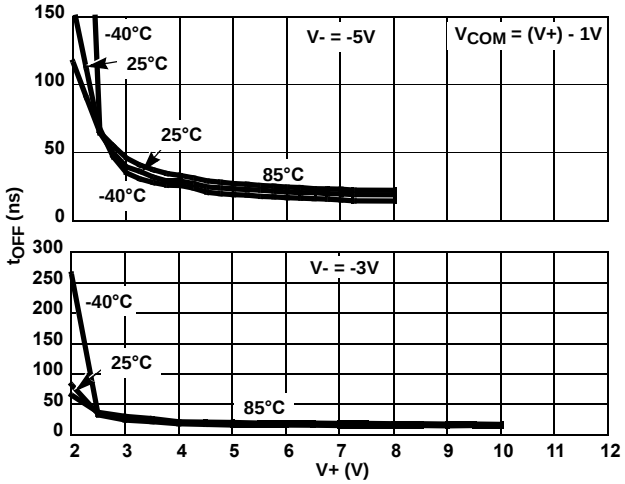



FIGURE 15. TURN - OFF TIME vs POSITIVE SUPPLY VOLTAGE

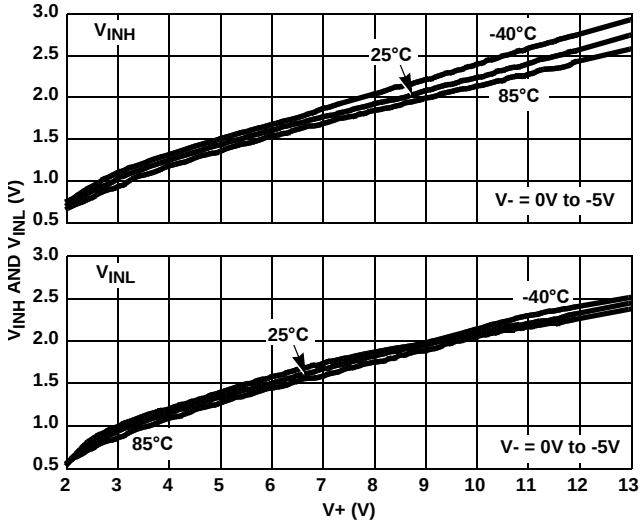



FIGURE 16. DIGITAL SWITCHING POINT vs POSITIVE SUPPLY VOLTAGE

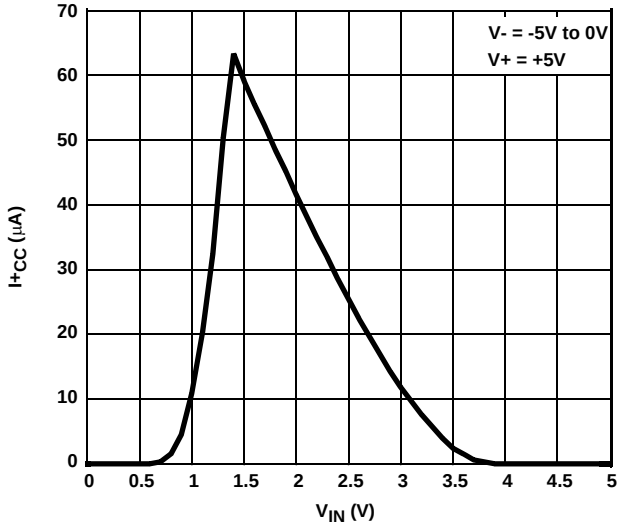



FIGURE 17. POSITIVE SUPPLY CURRENT vs DIGITAL INPUT VOLTAGE

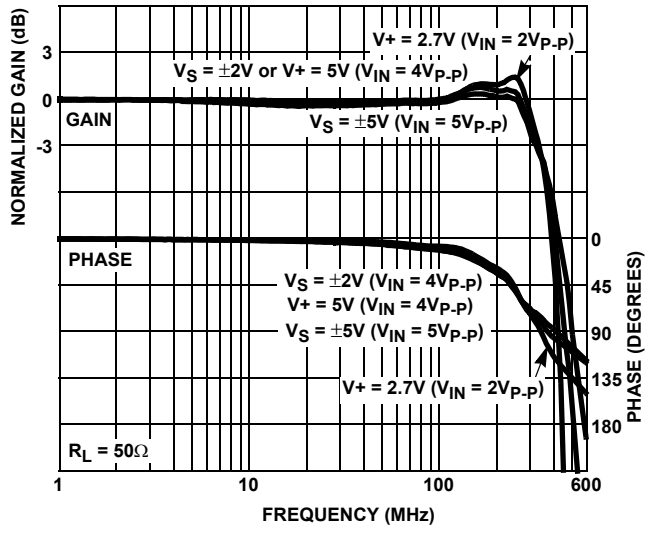



FIGURE 18. FREQUENCY RESPONSE

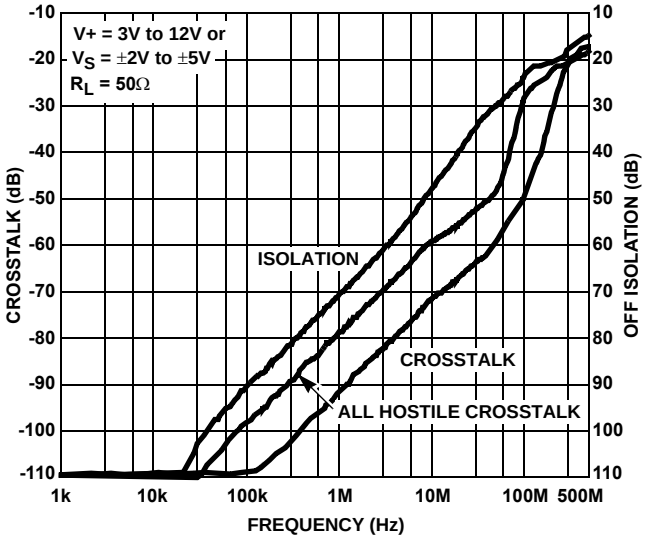



FIGURE 19. CROSSTALK AND OFF ISOLATION

## Typical Performance Curves $T_A$ = 25°C, Unless Otherwise Specified **(Continued)**

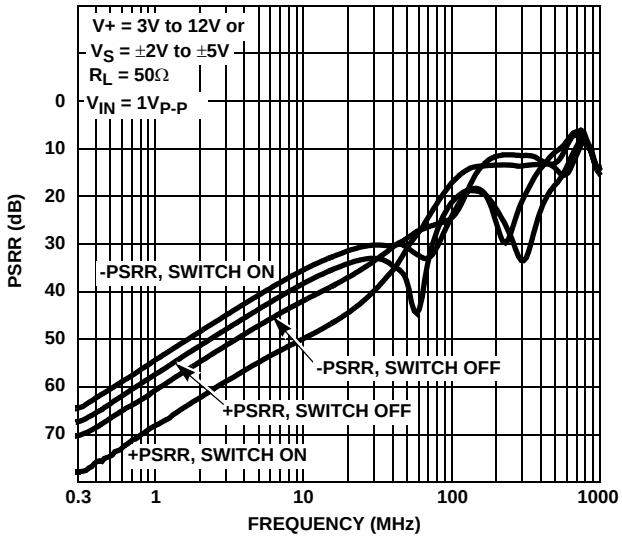



**FIGURE 20. ±PSRR vs FREQUENCY**

## Die Characteristics

**SUBSTRATE POTENTIAL (POWERED UP):**

V-

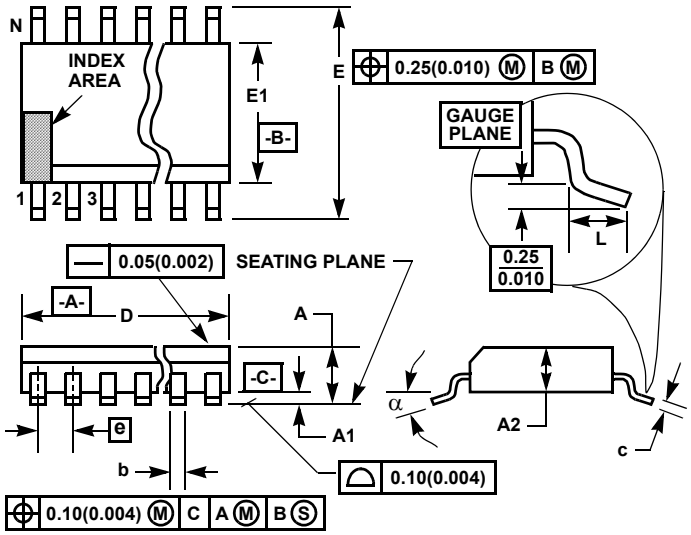
**TRANSISTOR COUNT:**

209

**PROCESS:**

Si Gate CMOS

## Thin Shrink Small Outline Plastic Packages (TSSOP)




NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AB, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

### M16.173

**16 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.043 | - | 1.10 | - |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 | - |
| A2 | 0.033 | 0.037 | 0.85 | 0.95 | - |
| b | 0.0075 | 0.012 | 0.19 | 0.30 | 9 |
| c | 0.0035 | 0.008 | 0.09 | 0.20 | - |
| D | 0.193 | 0.201 | 4.90 | 5.10 | 3 |
| E1 | 0.169 | 0.177 | 4.30 | 4.50 | 4 |
| e | 0.026 BSC | | 0.65 BSC | | - |
| E | 0.246 | 0.256 | 6.25 | 6.50 | - |
| L | 0.020 | 0.028 | 0.50 | 0.70 | 6 |
| N | 16 | | 16 | | 7 |
| α | 0° | 8° | 0° | 8° | - |

Rev. 1 2/02