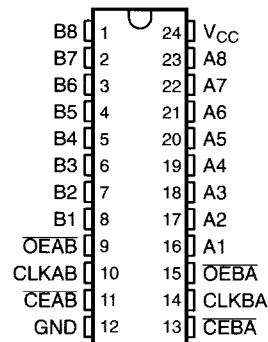


SN74LVC2952 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

JANUARY 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC2952 consists of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (\overline{CEAB} or \overline{CEBA}) input is low. Taking the output-enable (\overline{OEAB} or \overline{OEBA}) input low accesses the data on either port.

The SN74LVC2952 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC2952 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†

INPUTS				OUTPUT
\overline{CEAB}	CLKAB	\overline{OEAB}	A	B
H	X	L	X	B_0^\ddagger
X	L	L	X	B_0^\ddagger
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses \overline{CEBA} , CLKBA, and \overline{OEBA} .

‡ Level of B before the indicated steady-state input conditions were established.

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PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



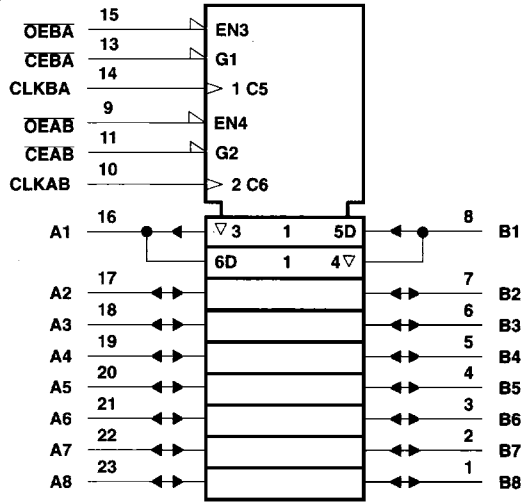
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OCTAL BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

JANUARY 1993

logic symbol†

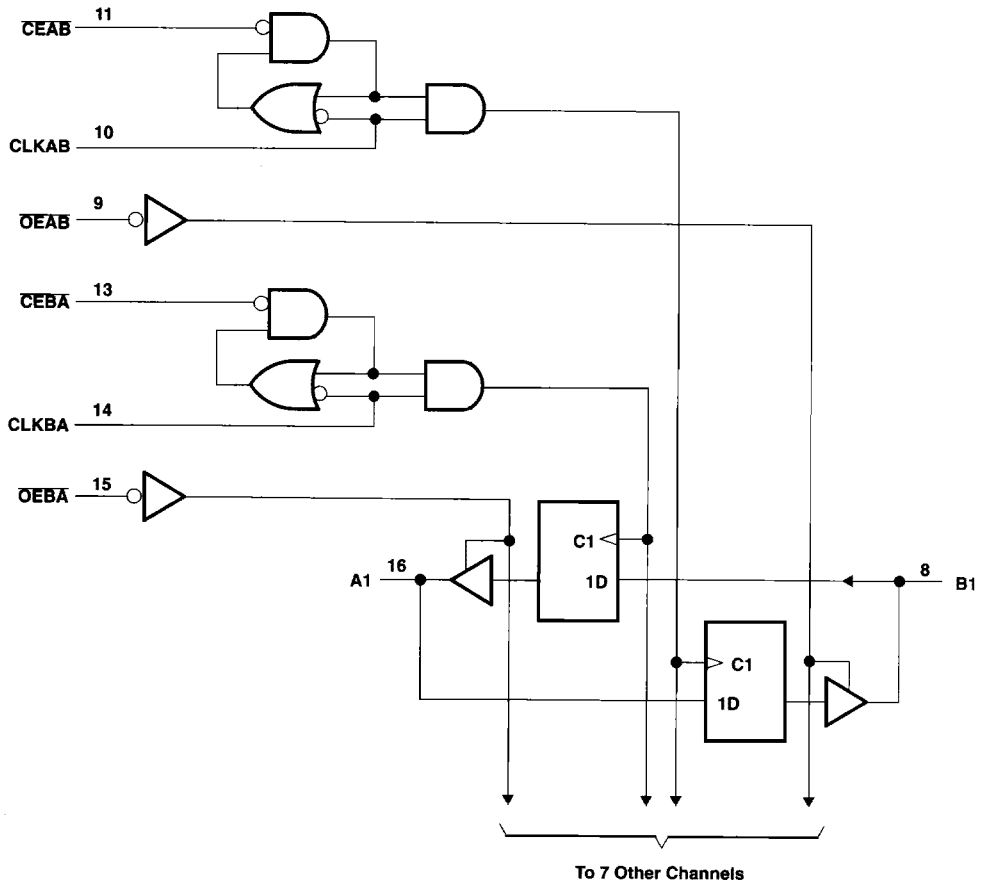


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

SN74LVC2952
OCTAL BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS
 JANUARY 1993

logic diagram (positive logic)



PRODUCT PREVIEW

SN74LVC2952
OCTAL BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

JANUARY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.5 W
..... DW package	0.85 W
..... PW package	0.5 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		-12
		$V_{CC} = 3$ V		-24‡
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12
		$V_{CC} = 3$ V		24‡
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	$^\circ\text{C}$

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

‡ Current duty cycle $\leq 50\%$, $f \geq 1$ kHz

PRODUCT PREVIEW



SN74LVC2952
OCTAL BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS
 JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}^\dagger	MIN	TYP	MAX	UNIT
V_{IK}		$I_i = -18 \text{ mA}$	2.7 V			-1.2	V
V_{OH}		$I_{OH} = -100 \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
		$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
		$I_{OH} = -24 \text{ mA}$	3 V	2.4			
V_{OL}		$I_{OL} = 100 \mu\text{A}$	MIN to MAX			0.2	V
		$I_{OL} = 12 \text{ mA}$	2.7 V			0.4	
		$I_{OL} = 24 \text{ mA}$	3 V			0.55	
I_i		$V_i = V_{CC}$ or GND	3.6 V			± 5	μA
I_{OZ}^\ddagger		$V_O = V_{CC}$ or GND	3.6 V			± 10	μA
I_{CC}		$V_i = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μA
ΔI_{CC}		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND				500	μA
C_i	Control inputs	$V_i = V_{CC}$ or GND	3.3 V	TBD			pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V	TBD			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW



