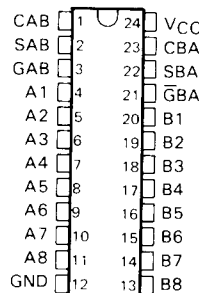


SN74ALS614, SN74ALS615 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

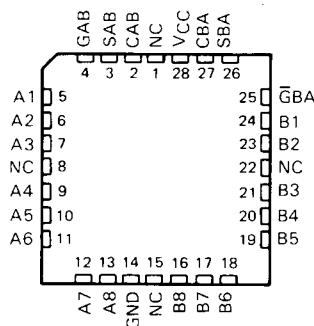
D2915, JANUARY 1986

- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True and Inverting Data Paths
'ALS614 . . . Inverting logic
'ALS615 . . . True logic
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

DW OR NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and \bar{G} BA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and \bar{G} BA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The -1 versions of the SN74ALS614 and SN74ALS615 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes.

The SN74ALS614 and SN74ALS615 are characterized for operation from 0°C to 70°C.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

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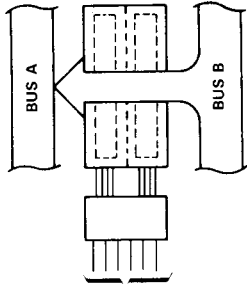
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2
ALS and AS Circuits

SN74ALS614, SN74ALS615
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH OPEN-COLLECTOR OUTPUTS

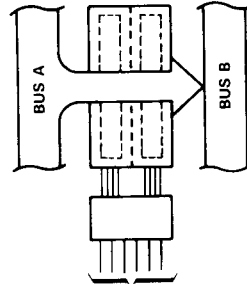
2

ALS and AS Circuits



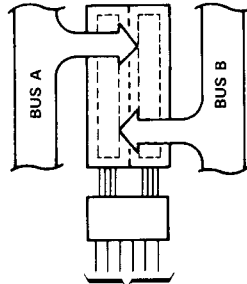
GAB	$\bar{G}BA$	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
 BUS B TO BUS A



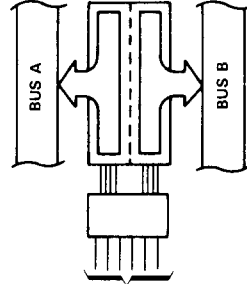
GAB	$\bar{G}BA$	CAB	CBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
 BUS A TO BUS B



GAB	$\bar{G}BA$	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
 A AND/OR B



GAB	$\bar{G}BA$	CAB	CBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER
 STORED DATA
 TO A AND/OR B

SN74ALS614, SN74ALS615

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
GAB	$\bar{G}BA$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	SN74ALS614	SN74ALS615
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	\uparrow	\uparrow	X	X	Input	Input	Store A and B Data	Store A and B Data
X	H	\cdot	H or L	X	X	Input	Unspecified [†]	Store A, Hold B	Store A, Hold B
H	H	\cdot	\uparrow	X [‡]	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	\uparrow	X	X	Unspecified [†]	Input	Hold A, Store B	Hold A, Store B
L	L	\cdot	\uparrow	X	X [‡]	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time \bar{B} Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored \bar{B} Data to A Bus	Stored B data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time \bar{A} Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored \bar{A} Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored \bar{A} Data to B Bus and Stored \bar{B} Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

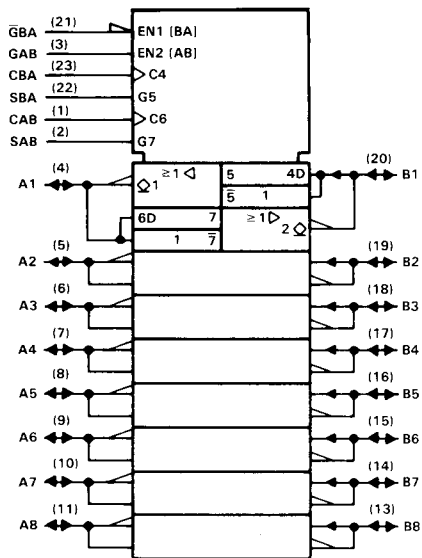
[†]The data output functions may be enabled or disabled by various signals at the GAB or $\bar{G}BA$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

[‡]Select control = L: clocks can occur simultaneously.

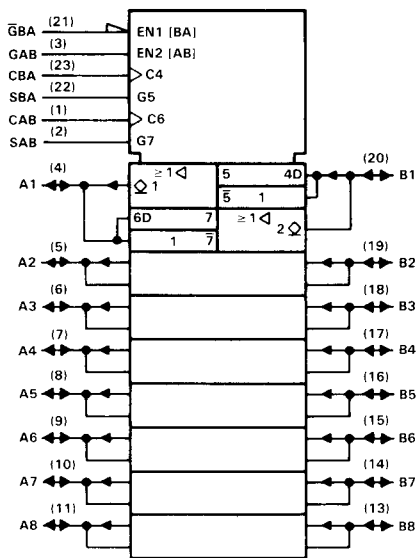
Select control = H: clocks must be staggered in order to load both registers.

logic symbols[†]

SN74ALS614



SN74ALS615



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW and NT packages.

2

ALS and AS Circuits

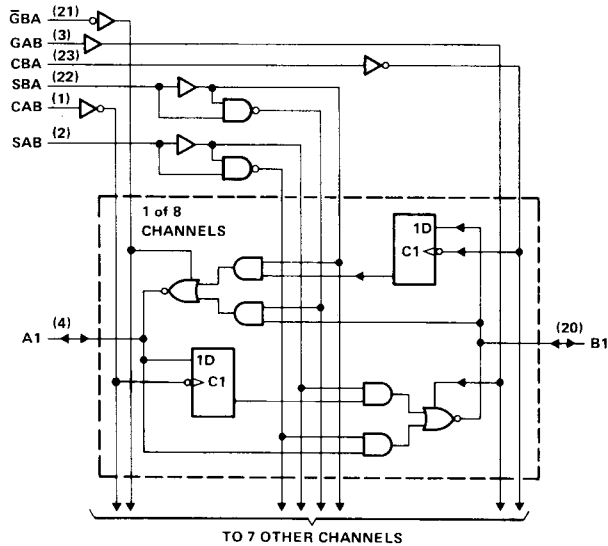
SN74ALS614, SN74ALS615 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

logic diagrams (positive logic)

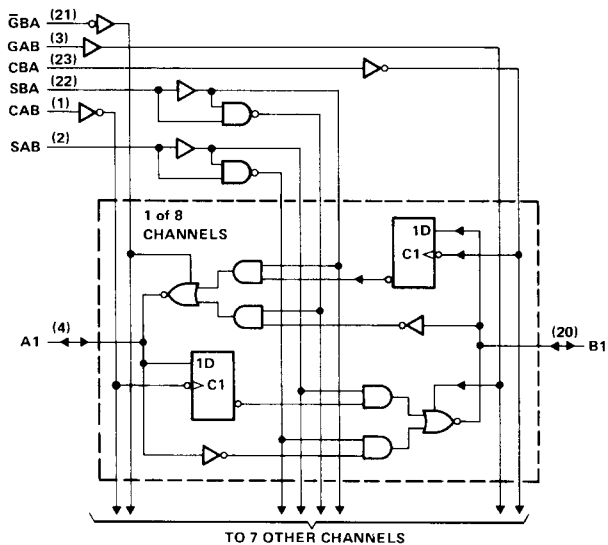
2

ALS and AS Circuits

SN74ALS614



SN74ALS615



Pin numbers shown are for DW and NT packages.

SN74ALS614, SN74ALS615

OCTAL BUS TRANSCIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: All inputs	7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage				0.8
V_{OH}	High-level output voltage				5.5
I_{OL}	Low-level output current				24
					48 ¹
t_w	Pulse duration	CBA or CAB high		16.5	ns
		CBA or CAB low		16.5	
t_{su}	Setup time before CAB [†] or CBA [†]	A or B		10	ns
t_h	Hold time after CAB [†] or CBA [†]	A or B		0	ns
T_A	Operating free-air temperature	0	70		$^{\circ}\text{C}$

¹The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V. The 48-mA limit applies for the SN74ALS614-1 and SN74ALS615-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [‡]	MAX	UNIT
V_{IK}		$V_{CC} = 4.5\text{ V}, I_I = -18\text{ mA}$				-1.2	V
I_{OH}		$V_{CC} = 4.5\text{ V}, V_{OH} = 5.5\text{ V}$				0.1	mA
V_{OL}		$V_{CC} = 4.5\text{ V}, I_{OL} = 12\text{ mA}$			0.25	0.4	V
		$V_{CC} = 4.75\text{ V}, I_{OL} = 24\text{ mA}$ ($I_{OL} = 48\text{ mA}$ for -1 versions)			0.35	0.5	
I_I	Control inputs	$V_{CC} = 5.5\text{ V}, V_I = 7\text{ V}$				0.1	mA
	A or B ports	$V_{CC} = 5.5\text{ V}, V_I = 5.5\text{ V}$				0.1	
I_{IH}	Control inputs	$V_{CC} = 5.5\text{ V}, V_I = 2.7\text{ V}$			20		μA
	A or B ports [§]				20		
I_{IL}	Control inputs	$V_{CC} = 5.5\text{ V}, V_I = 0.4\text{ V}$				-0.2	mA
	A or B ports [§]					-0.2	
I_{CC}	'ALS614	$V_{CC} = 5.5\text{ V}$		Outputs high	52	60	mA
				Outputs low	57	70	
	'ALS615			Output high	40	60	mA
				Output low	48	72	

[‡]All typical values are at $V_{CC} = 5\text{ V}, T_A = 25^{\circ}\text{C}$.

[§]For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

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ALS and AS Circuits

SN74ALS614, SN74ALS615
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH OPEN-COLLECTOR OUTPUTS

SN74ALS614 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R _L = 680 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 680 Ω, T _A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	CBA or CAB	A or B		37	52	20	64	ns
t _{PHL}				14	19	6	20	
t _{PLH}	A or B	B or A		31	42	14	51	ns
t _{PHL}				6	10	2	12	
t _{PLH}	SBA or SAB† (with A or B high)	A or B		35	47	19	58	ns
t _{PHL}				12	20	5	22	
t _{PLH}	SBA or SAB† (with A or B low)	A or B		35	47	19	58	ns
t _{PHL}				12	20	5	22	
t _{PLH}	G̅BA or GAB	A or B		16	22	9	27	ns
t _{PHL}				12	18	6	22	

SN74ALS615 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R _L = 680 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 680 Ω, T _A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	CBA or CAB	A or B		33	50	19	64	ns
t _{PHL}				14	20	6	22	
t _{PLH}	A or B	B or A		28	44	12	56	ns
t _{PHL}				11	17	4	20	
t _{PLH}	SBA or SAB† (with A or B high)	A or B		35	50	19	62	ns
t _{PHL}				15	22	5	25	
t _{PLH}	SBA or SAB† (with A or B low)	A or B		35	50	19	62	ns
t _{PHL}				15	22	5	25	
t _{PLH}	G̅BA or GAB	A or B		17	23	6	27	ns
t _{PHL}				14	20	6	24	

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
 NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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