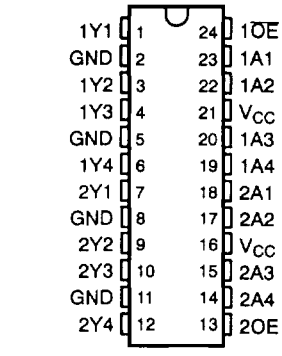
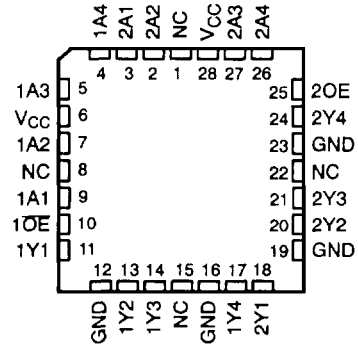
- **State-of-the-Art *EPIC*-IIB ™ BICMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 25 Ω or Greater**
- **Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs**
- **Bus-Hold Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54ABT25241 . . . JT PACKAGE
SN74ABT25241 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ABT25241 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'ABT25241 is a 25-Ω octal buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers.

The 'ABT25241 contains complementary output-enable (1$\overline{OE}$ and 2OE) inputs. When 1$\overline{OE}$ is low and 2OE is high, the device transmits data from the A inputs to the Y outputs. When 1$\overline{OE}$ and 2OE are high, the outputs are in the high-impedance state. Output-enable 1$\overline{OE}$ affects only the 1Y outputs; output-enable 2OE affects only the 2Y outputs.

This buffer/driver is capable of sinking 188 mA of I_{OL} current, which facilitates switching 25-Ω transmission lines on the incident wave. The distributed V_{CC} and GND pins minimize switching noise for more reliable system operation.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN54ABT25241 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT25241 is characterized for operation from −40°C to 85°C.

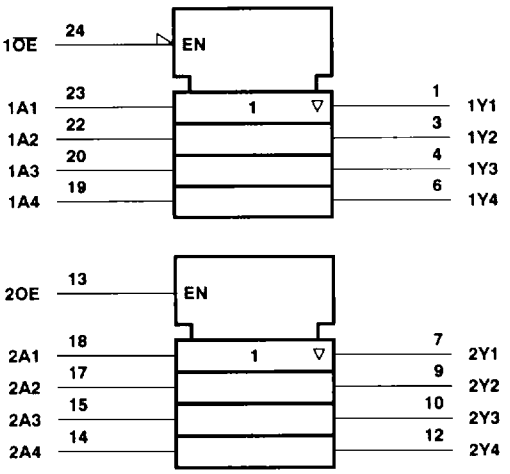
EPIC-IIB is a trademark of Texas Instruments Incorporated.

FUNCTION TABLES

INPUTS		OUTPUT
$1\overline{OE}$	1A	1Y
L	H	H
L	L	L
H	X	Z

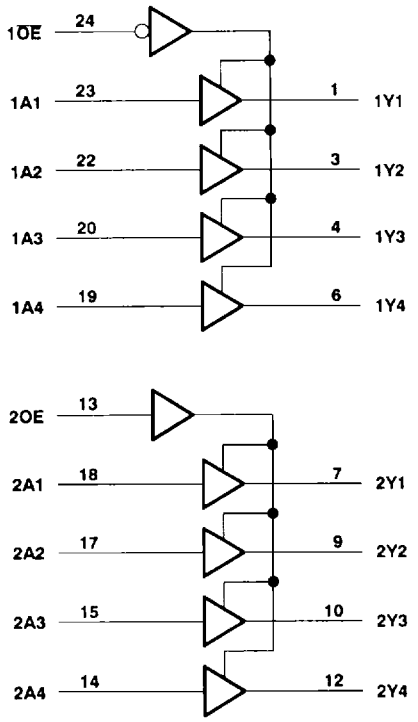
INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O ..... −0.5 V to V_{CC}
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Current into any output in the low state, I_O: SN54ABT25241 ..... 250 mA
SN74ABT25241 ..... 376 mA
Operating free-air temperature range: SN54ABT25241 ..... −55°C to 125°C
SN74ABT25241 ..... −40°C to 85°C
Maximum power dissipation at T_A = 55°C (in still air): DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			SN54ABT25241		SN74ABT25241		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{IK}	Input clamp current			−18		−18	mA
I_{OH}	High-level output current			−53		−80	mA
I_{OL}	Low-level output current			125		188	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

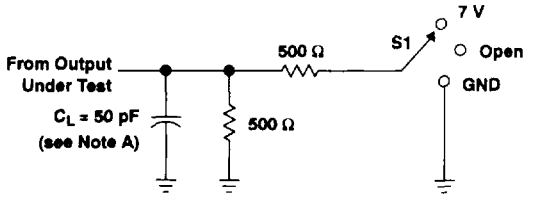
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54ABT25241			SN74ABT25241			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −3 mA					2.7			V
	V_{CC} = 4.5 V,	I_{OH} = −53 mA		2						
	V_{CC} = 4.5 V,	I_{OH} = −80 mA					2.4			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 94 mA				0.55			0.55	V
	V_{CC} = 4.5 V,	I_{OL} = 125 mA				0.8				
	V_{CC} = 4.5 V,	I_{OL} = 188 mA							0.7	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1			±1	µA
I_{hold}	V_{CC} = 4.5 V,	V_I = 0.8 V	A pins			100			100	µA
	V_{CC} = 4.5 V,	V_I = 2 V				−100			−100	
I_{OZH}‡	V_{CC} = 5.5 V,	V_O = 2.7 V				50			50	µA
I_{OZL}‡	V_{CC} = 5.5 V,	V_O = 0.5 V				−50			−50	µA
I_{OFF}	V_{CC} = 0 V,	V_I or V_O ≤ 4.5 V				±500			±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50			50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		−50		180	−50		180	mA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} or GND	Outputs open,	Outputs high			500			500	µA
			Outputs low			30			30	mA
			Outputs disabled			500			500	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				1			1	mA
C_i	V_{CC} = 5 V,	V_I = V_{CC} or GND								pF
C_o	V_{CC} = 5 V,	V_O = V_{CC} or GND								pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

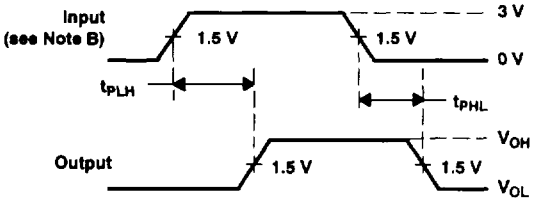
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

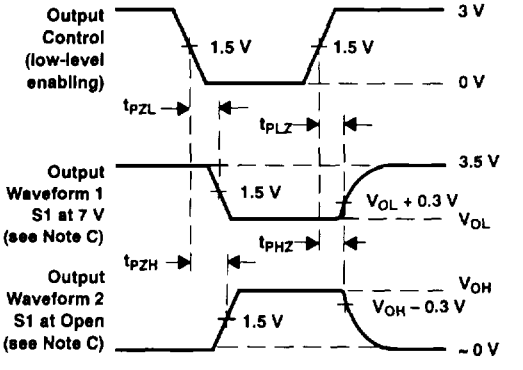


LOAD CIRCUIT FOR OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms