

- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 12 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Low Power . . . 500 μA Max**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage**
950 μV Max at T_A = 25°C (TLV226xA)
- **Wide Supply Voltage Range**
2.7 V to 8 V
- **Macromodel Included**
- **Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control / Print Support Qualification to Automotive Standards**

description

The TLV2262 and TLV2264 are dual and quad low voltage operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single or split supply applications. The TLV226x family offers a compromise between the micro-power TLV225x and the ac performance of the TLC227x. It has low supply current for battery-powered applications, while still having adequate ac performance for applications that demand it. This family is fully characterized at 3 V and 5 V and is optimized for low-voltage applications. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. Figure 1 depicts the low level of noise voltage for this CMOS amplifier, which has only 200 μA (typ) of supply current per amplifier.

The TLV226x, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micro-power dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV226xA family is available and has a maximum input offset voltage of 950 μV.

The TLV2262/4 also makes great upgrades to the TLV2332/4 in standard designs. They offer increased output dynamic range, lower noise voltage and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442 devices. If your design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption make them ideal for high density, battery-powered equipment.

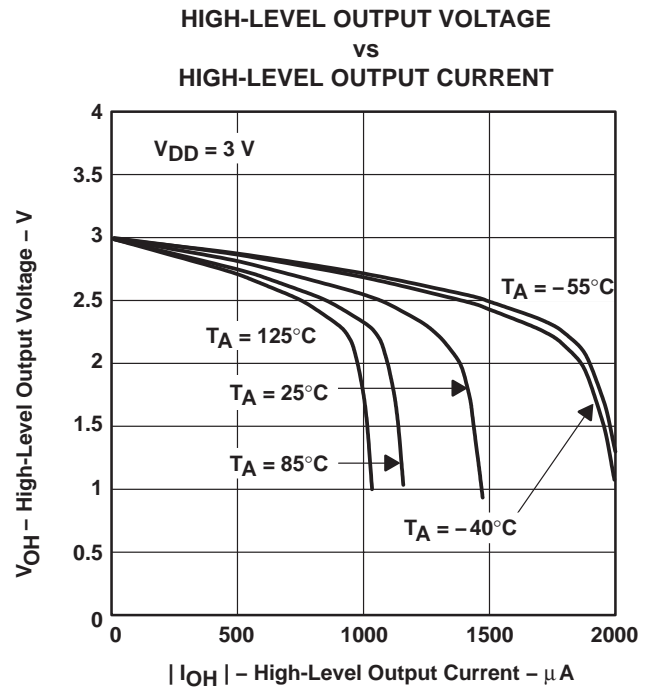


Figure 1



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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TLV2262 AVAILABLE OPTIONS

| T _A | V _{IO} max AT 25°C | PACKAGED DEVICES | | | | | |
|----------------|--------------------------------|-------------------------|---------------------------|---------------------------|-------------------------|--------------------|----------------------------|
| | | SMALL OUTLINE (D) | CHIP CARRIER (FK) | CERAMIC DIP (JG) | PLASTIC DIP (P) | TSSOP (PW) | CERAMIC FLATPACK (U) |
| 0°C to 70°C | 2.5 mV | TLV2262CD | — | — | TLV2262CP | TLV2262CPWLE | — |
| –40°C to 125°C | 950 μV 2.5 mV | TLV2262AID TLV2262ID | — — | — — | TLV2262AIP TLV2262IP | TLV2262AIPWLE — | — — |
| –40°C to 125°C | 950 μV 2.5 mV | TLV2262AQD TLV2262QD | — — | — — | — — | — — | — — |
| –55°C to 125°C | 950 μV 2.5 mV | — — | TLV2262AMFK TLV2262MFK | TLV2262AMJG TLV2262MJG | — — | — — | TLV2262AMU TLV2262MU |

† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2262CDR).

‡ The PW package is available only left-end taped and reeled.

§ Chips are tested at 25°C.

¶ For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

TLV2264 AVAILABLE OPTIONS

| T _A | V _{IO} max AT 25°C | PACKAGED DEVICES | | | | | |
|-------------------|--------------------------------|-------------------------|---------------------------|-------------------------|-------------------------|--------------------|----------------------------|
| | | SMALL OUTLINE (D) | CHIP CARRIER (FK) | CERAMIC DIP (J) | PLASTIC DIP (N) | TSSOP (PW) | CERAMIC FLATPACK (W) |
| –40°C to 125°C | 950 μV 2.5 mV | TLV2264AID TLV2264ID | — — | — — | TLV2264AIN TLV2264IN | TLV2264AIPWLE — | — — |
| –40°C to 125°C | 950 μV 2.5 mV | TLV2264AQD TLV2264QD | — — | — — | — — | — — | — — |
| –55°C to 125°C | 950 μV 2.5 mV | — — | TLV2264AMFK TLV2264MFK | TLV2264AMJ TLV2264MJ | — — | — — | TLV2264AMW TLV2264MW |

† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2262IDR).

‡ The PW package is available only left-end taped and reeled.

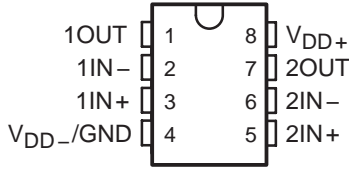
§ Chips are tested at 25°C.

¶ For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

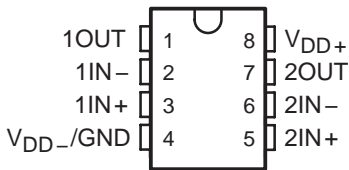
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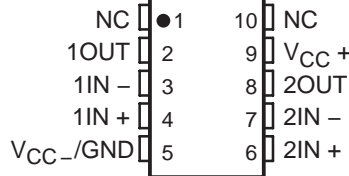
**TLV2262C, TLV2262AC
TLV2262I, TLV2262AI
TLV2262Q, TLV2262AQ
D, P, OR PW PACKAGE
(TOP VIEW)**



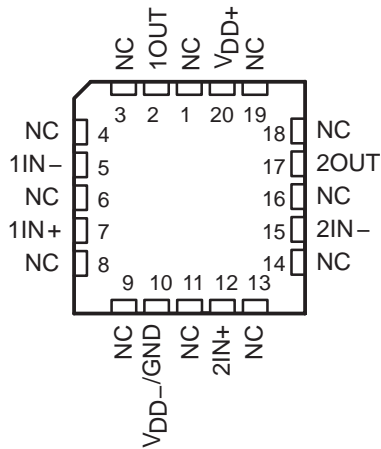
**TLV2262M, TLV2262AM
JG PACKAGE
(TOP VIEW)**



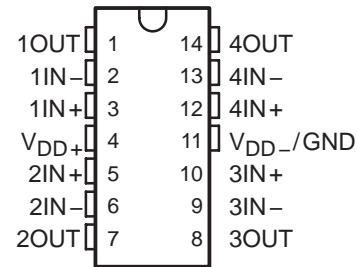
**TLV2662M, TLV2262AM
U PACKAGE
(TOP VIEW)**



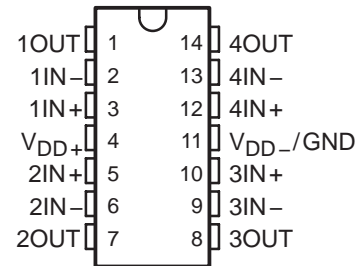
**TLV2262M, TLV2262AM
FK PACKAGE
(TOP VIEW)**



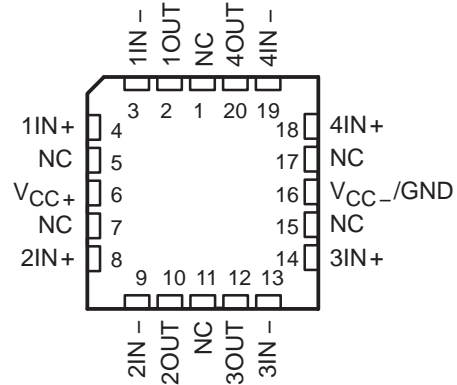
**TLV2264I, TLV2264AI
TLV2264Q, TLV2264AQ
D, N, OR PW PACKAGE
(TOP VIEW)**



**TLV2264M, TLV2264AM
J OR W PACKAGE
(TOP VIEW)**



**TLV2264M, TLV2264AM
FK PACKAGE
(TOP VIEW)**

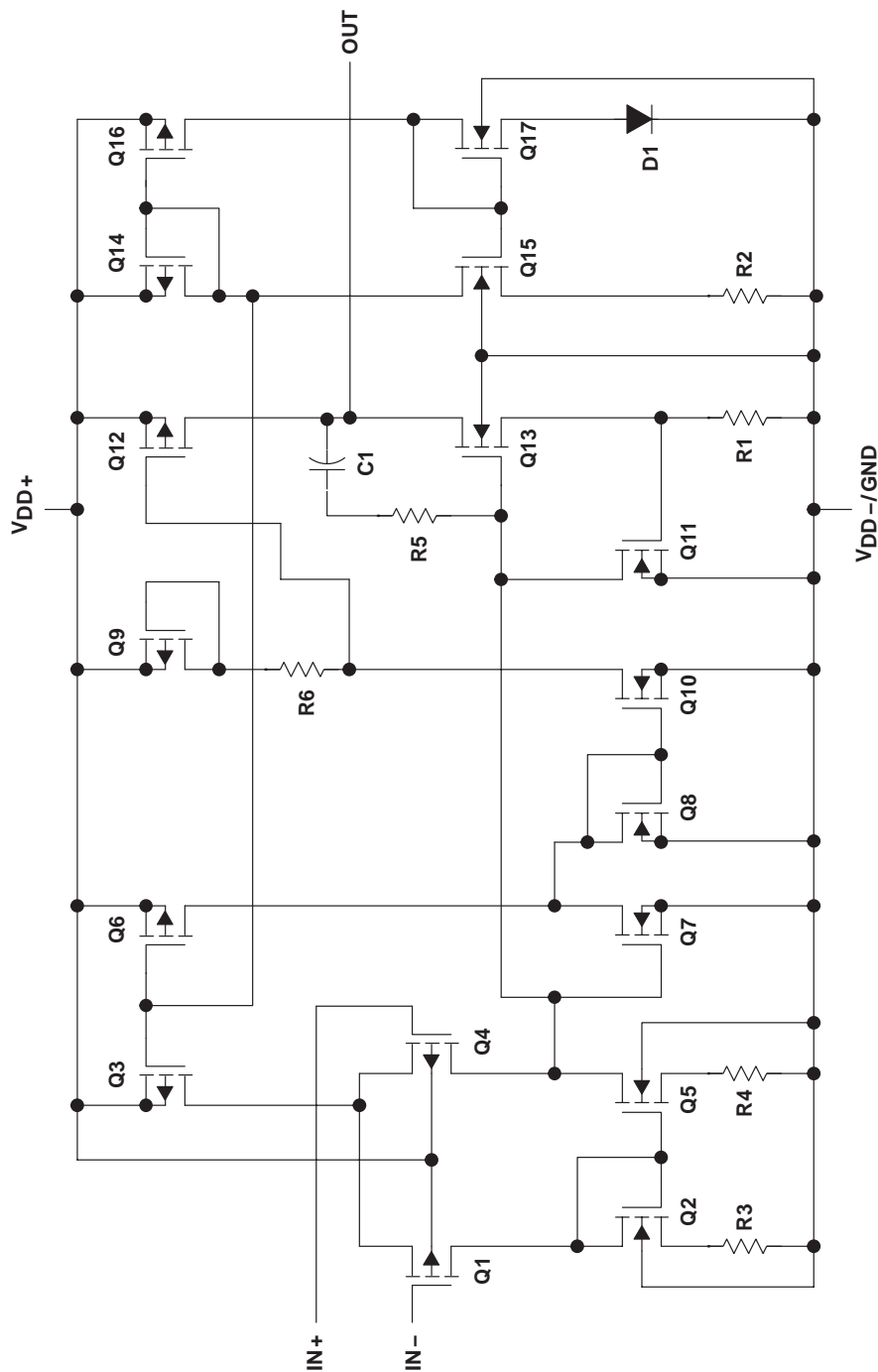


TLV226x, TLV226xA

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equivalent schematic (each amplifier)



| ACTUAL DEVICE COMPONENT COUNT† | |
|--------------------------------|---------|
| COMPONENT | TLV2252 |
| Transistors | 38 |
| Resistors | 28 |
| Diodes | 9 |
| Capacitors | 3 |

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|--|
| Supply voltage, V_{DD} (see Note 1) | 16 V |
| Differential input voltage, V_{ID} (see Note 2) | $\pm V_{DD}$ |
| Input voltage range, V_I (any input, see Note 1) | $V_{DD-} - 0.3 \text{ V}$ to V_{DD+} |
| Input current, I_I (each input) | $\pm 5 \text{ mA}$ |
| Output current, I_O | $\pm 50 \text{ mA}$ |
| Total current into V_{DD+} | $\pm 50 \text{ mA}$ |
| Total current out of V_{DD-} | $\pm 50 \text{ mA}$ |
| Duration of short-circuit current (at or below) 25°C (see Note 3) | unlimited |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, T_A : | |
| I suffix | -40°C to 125°C |
| Q suffix | -40°C to 125°C |
| M suffix | -55°C to 125°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to V_{DD-} .
 2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below $V_{DD-} - 0.3 \text{ V}$.
 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 85^\circ\text{C}$ POWER RATING | $T_A = 125^\circ\text{C}$ POWER RATING |
|---------|---|---|--|---|
| D-8 | 725 mW | 5.8 mW/°C | 377 mW | 145 mW |
| D-14 | 950 mW | 7.6 mW/°C | 494 mW | 190 mW |
| FK | 1375 mW | 11.0 mW/°C | 715 mW | 275 mW |
| J | 1375 mW | 11.0 mW/°C | 715 mW | 275 mW |
| JG | 1050 mW | 8.4 mW/°C | — | 210 mW |
| N | 1150 mW | 9.2 mW/°C | 598 mW | — |
| P | 1000 mW | 8.0 mW/°C | 520 mW | 200 mW |
| PW-8 | 525 mW | 4.2 mW/°C | 273 mW | 105 mW |
| PW-14 | 700 mW | 5.6 mW/°C | 364 mW | — |
| U | 700 mW | 5.5 mW/°C | — | 150 mW |
| W | 700 mW | 5.5 mW/°C | 370 mW | 150 mW |

recommended operating conditions

| | I SUFFIX | | Q SUFFIX | | M SUFFIX | | UNIT |
|--|-----------|-----------------|-----------|-----------------|-----------|-----------------|------|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| Supply voltage, $V_{DD\pm}$ (see Note 1) | 2.7 | 8 | 2.7 | 8 | 2.7 | 8 | V |
| Input voltage range, V_I | V_{DD-} | $V_{DD+} - 1.3$ | V_{DD-} | $V_{DD+} - 1.3$ | V_{DD-} | $V_{DD+} - 1.3$ | V |
| Common-mode input voltage, V_{IC} | V_{DD-} | $V_{DD+} - 1.3$ | V_{DD-} | $V_{DD+} - 1.3$ | V_{DD-} | $V_{DD+} - 1.3$ | V |
| Operating free-air temperature, T_A | -40 | 125 | -40 | 125 | -55 | 125 | °C |

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-} .

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TLV2262I electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T_A † | TLV2262I | | | TLV2262AI | | | UNIT |
|--|---|------------------------------|------------|-------------|------|-----------|-------------|-----|------------------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{IO} Input offset voltage | $V_{DD\pm} = \pm 1.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$ | 25°C | 300 | 2500 | | 300 | 950 | | μV |
| | | Full range | | | 3000 | | 1500 | | |
| α_{VIO} Temperature coefficient of input offset voltage | | 25°C to 85°C | 2 | | | 2 | | | $\mu\text{V}/^\circ\text{C}$ |
| Input offset voltage long-term drift (see Note 4) | | 25°C | 0.003 | | | 0.003 | | | $\mu\text{V}/\text{mo}$ |
| I_{IO} Input offset current | | 25°C | 0.5 | 60 | | 0.5 | 60 | | pA |
| | | 85°C | | 150 | | 150 | | | |
| | | Full range | | 800 | | 800 | | | |
| I_{IB} Input bias current | | 25°C | 1 | 60 | | 1 | 60 | | pA |
| | 85°C | | 150 | | 150 | | | | |
| | Full range | | 800 | | 800 | | | | |
| V_{ICR} Common-mode input voltage range | $R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$ | 25°C | 0 to 2 | -0.3 to 2.2 | | 0 to 2 | -0.3 to 2.2 | | V |
| | | Full range | 0 to 1.7 | | | 0 to 1.7 | | | |
| V_{OH} High-level output voltage | $I_{OH} = -20\ \mu\text{A}$ | 25°C | 2.99 | | | 2.99 | | | V |
| | $I_{OH} = -100\ \mu\text{A}$ | 25°C | 2.85 | | | 2.85 | | | |
| | $I_{OH} = -400\ \mu\text{A}$ | Full range | 2.825 | | | 2.825 | | | |
| | | 25°C | 2.7 | | | 2.7 | | | |
| V_{OL} Low-level output voltage | $V_{IC} = 1.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$ | 25°C | 10 | | | 10 | | | mV |
| | | 25°C | 100 | | | 100 | | | |
| | $V_{IC} = 1.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$ | Full range | 150 | | | 150 | | | |
| | | 25°C | 200 | | | 200 | | | |
| AVD Large-signal differential voltage amplification | $V_{IC} = 1.5\text{ V}$, $V_O = 1\text{ V to }2\text{ V}$ | $R_L = 50\ \text{k}\Omega$ ‡ | 25°C | 60 | 100 | | 60 | 100 | V/mV |
| | | | Full range | 30 | | | 30 | | |
| | $R_L = 1\ \text{M}\Omega$ ‡ | 25°C | 100 | | | 100 | | | |
| | | Full range | 100 | | | 100 | | | |
| $r_{i(d)}$ Differential input resistance | | 25°C | 10^{12} | | | 10^{12} | | | Ω |
| $r_{i(c)}$ Common-mode input resistance | | 25°C | 10^{12} | | | 10^{12} | | | Ω |
| $c_{i(c)}$ Common-mode input capacitance | $f = 10\ \text{kHz}$, P package | 25°C | 8 | | | 8 | | | pF |
| z_o Closed-loop output impedance | $f = 100\ \text{kHz}$, $A_V = 10$ | 25°C | 270 | | | 270 | | | Ω |
| CMRR Common-mode rejection ratio | $V_{IC} = 0\text{ to }1.7\text{ V}$, $V_O = 1.5\text{ V}$, $R_S = 50\ \Omega$ | 25°C | 65 | 75 | | 65 | 77 | | dB |
| | | Full range | 60 | | | 60 | | | |
| k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | $V_{DD} = 2.7\text{ V to }8\text{ V}$, $V_{IC} = V_{DD}/2$, No load | 25°C | 80 | 95 | | 80 | 100 | | dB |
| | | Full range | 80 | | | 80 | | | |

† Full range is -40°C to 125°C .

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLV2262I electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted) (continued)

| PARAMETER | TEST CONDITIONS | T_A † | TLV2262I | | | TLV2262AI | | | UNIT |
|-------------------------|--------------------------------|------------|----------|-----|-----|-----------|-----|---------------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| I_{DD} Supply current | $V_O = 1.5\text{ V}$, No load | 25°C | 400 | 500 | | 400 | 500 | μA | |
| | | Full range | | 500 | | | 500 | | |

† Full range is – 40°C to 125°C.

TLV2262I operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

| PARAMETER | TEST CONDITIONS | T_A † | TLV2262I | | | TLV2262AI | | | UNIT |
|---|---|----------------|----------|-------|-----|-----------|-------|------------------------------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR Slew rate at unity gain | $V_O = 1.1\text{ V to }1.9\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | 25°C | 0.35 | 0.55 | | 0.35 | 0.55 | $\text{V}/\mu\text{s}$ | |
| | | Full range | 0.3 | | | 0.3 | | | |
| V_n Equivalent input noise voltage | $f = 10\text{ Hz}$ | 25°C | | 43 | | | 43 | $\text{nV}/\sqrt{\text{Hz}}$ | |
| | $f = 1\text{ kHz}$ | 25°C | | 12 | | | 12 | | |
| $V_{N(PP)}$ Peak-to-peak equivalent input noise voltage | $f = 0.1\text{ Hz to }1\text{ Hz}$ | 25°C | | 0.6 | | | 0.6 | μV | |
| | $f = 0.1\text{ Hz to }10\text{ Hz}$ | 25°C | | 1 | | | 1 | | |
| I_n Equivalent input noise current | | 25°C | | 0.6 | | | 0.6 | $\text{fA}/\sqrt{\text{Hz}}$ | |
| THD + N Total harmonic distortion plus noise | $V_O = 0.5\text{ V to }2.5\text{ V}$, $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega$ ‡ | $A_V = 1$ | | 0.03% | | | 0.03% | | |
| | | $A_V = 10$ | | 0.05% | | | 0.05% | | |
| Gain-bandwidth product | $f = 1\text{ kHz}$, $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | 25°C | | 0.67 | | | 0.67 | MHz | |
| B_{OM} Maximum output-swing bandwidth | $V_{O(PP)} = 1\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡, $A_V = 1$, $C_L = 100\text{ pF}$ ‡ | 25°C | | 395 | | | 395 | kHz | |
| t_s Settling time | $A_V = -1$, Step = 1 V to 2 V, $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | $T_o = 0.1\%$ | | 5.6 | | | 5.6 | μs | |
| | | $T_o = 0.01\%$ | | 12.5 | | | 12.5 | | |
| ϕ_m Phase margin at unity gain | $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | 25°C | | 55° | | | 55° | | |
| | | 25°C | | 11 | | | 11 | | |
| Gain margin | | 25°C | | 11 | | | 11 | dB | |

† Full range is – 40°C to 125°C.

‡ Referenced to 1.5 V

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TLV2262I electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T_A † | TLV2262I | | | TLV2262AI | | | UNIT |
|--|---|--------------|------------------|-------------|------|------------------|-------------|------|------------------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{IO} Input offset voltage | $V_{DD} = \pm 2.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$ | 25°C | 300 | 2500 | | 300 | 950 | | μV |
| | | Full range | | | 3000 | | 1500 | | |
| α_{VIO} Temperature coefficient of input offset voltage | | 25°C to 85°C | 2 | | | 2 | | | $\mu\text{V}/^\circ\text{C}$ |
| Input offset voltage long-term drift (see Note 4) | | 25°C | 0.003 | | | 0.003 | | | $\mu\text{V}/\text{mo}$ |
| I_{IO} Input offset current | | 25°C | 0.5 | 60 | | 0.5 | 60 | | pA |
| | | 85°C | | 150 | | 150 | | | |
| | Full range | | 800 | | 800 | | | | |
| I_{IB} Input bias current | 25°C | 1 | 60 | | 1 | 60 | | pA | |
| | 85°C | | 150 | | 150 | | | | |
| | Full range | | 800 | | 800 | | | | |
| V_{ICR} Common-mode input voltage range | $ V_{IO} \leq 5\text{ mV}$, $R_S = 50\ \Omega$ | 25°C | 0 to 4 | -0.3 to 4.2 | | 0 to 4 | -0.3 to 4.2 | | V |
| | | Full range | 0 to 3.5 | | | 0 to 3.5 | | | |
| V_{OH} High-level output voltage | $I_{OH} = -20\ \mu\text{A}$ | 25°C | 4.99 | | 4.99 | | | V | |
| | | 25°C | 4.85 | 4.94 | 4.85 | 4.94 | | | |
| | | Full range | 4.82 | | 4.82 | | | | |
| | | 25°C | 4.7 | 4.85 | 4.7 | 4.85 | | | |
| $I_{OH} = -100\ \mu\text{A}$ | 25°C | 4.7 | | 4.85 | | | V | | |
| | Full range | 4.6 | | 4.6 | | | | | |
| V_{OL} Low-level output voltage | $V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$ | 25°C | 0.01 | | 0.01 | | | V | |
| | | 25°C | 0.09 | 0.15 | 0.09 | 0.15 | | | |
| | | Full range | 0.15 | | 0.15 | | | | |
| | | 25°C | 0.2 | 0.3 | 0.2 | 0.3 | | | |
| $I_{OL} = 500\ \mu\text{A}$ | 25°C | 0.2 | | 0.3 | | | V | | |
| | Full range | 0.3 | | 0.3 | | | | | |
| $V_{IC} = 2.5\text{ V}$, $I_{OL} = 1\text{ mA}$ | $V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to } 4\text{ V}$ | 25°C | 80 | 170 | 80 | 170 | | V/mV | |
| | | Full range | 55 | | 55 | | | | |
| | | 25°C | 550 | | 550 | | | | |
| $R_L = 50\text{ k}\Omega$ ‡ | | | | | | | | | |
| $R_L = 1\text{ M}\Omega$ ‡ | | | | | | | | | |
| $r_{i(d)}$ Differential input resistance | | 25°C | 10 ¹² | | | 10 ¹² | | | Ω |
| $r_{i(c)}$ Common-mode input resistance | | 25°C | 10 ¹² | | | 10 ¹² | | | Ω |
| $c_{i(c)}$ Common-mode input capacitance | $f = 10\text{ kHz}$, P package | 25°C | 8 | | | 8 | | | pF |
| z_o Closed-loop output impedance | $f = 100\text{ kHz}$, $A_V = 10$ | 25°C | 240 | | | 240 | | | Ω |
| CMRR Common-mode rejection ratio | $V_{IC} = 0\text{ to } 2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$ | 25°C | 70 | 83 | 70 | 83 | | dB | |
| | | Full range | 70 | | 70 | | | | |
| k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | $V_{DD} = 4.4\text{ V to } 8\text{ V}$, $V_{IC} = V_{DD}/2$, No load | 25°C | 80 | 95 | 80 | 95 | | dB | |
| | | Full range | 80 | | 80 | | | | |

† Full range is -40°C to 125°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLV2262I electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted) (continued)

| PARAMETER | TEST CONDITIONS | T_A † | TLV2262I | | | TLV2262AI | | | UNIT |
|-------------------------|--------------------------------|------------|----------|-----|-----|-----------|-----|-----|---------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| I_{DD} Supply current | $V_O = 2.5\text{ V}$, No load | 25°C | | 400 | 500 | | 400 | 500 | μA |
| | | Full range | | | 500 | | | 500 | |

† Full range is – 40°C to 125°C.

TLV2262I operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

| PARAMETER | TEST CONDITIONS | T_A † | TLV2262I | | | TLV2262AI | | | UNIT |
|---|---|------------|----------|--------|-----|-----------|--------|------------------------------|------------------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR Slew rate at unity gain | $V_O = 1.5\text{ V to }3.5\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | 25°C | 0.35 | 0.55 | | 0.35 | 0.55 | | $\text{V}/\mu\text{s}$ |
| | | Full range | 0.3 | | | 0.3 | | | |
| V_n Equivalent input noise voltage | $f = 10\text{ Hz}$ | 25°C | | 40 | | | 40 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| | $f = 1\text{ kHz}$ | 25°C | | 12 | | | 12 | | |
| $V_{N(PP)}$ Peak-to-peak equivalent input noise voltage | $f = 0.1\text{ Hz to }1\text{ Hz}$ | 25°C | | 0.7 | | | 0.7 | | μV |
| | $f = 0.1\text{ Hz to }10\text{ Hz}$ | 25°C | | 1.3 | | | 1.3 | | |
| I_n Equivalent input noise current | | 25°C | | 0.6 | | | 0.6 | $\text{fA}/\sqrt{\text{Hz}}$ | |
| THD + N Total harmonic distortion plus noise | $V_O = 0.5\text{ V to }2.5\text{ V}$, $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega$ ‡ | $A_V = 1$ | | 0.017% | | | 0.017% | | |
| | | $A_V = 10$ | | 0.03% | | | 0.03% | | |
| Gain-bandwidth product | $f = 50\text{ kHz}$, $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | 25°C | | 0.71 | | | 0.71 | MHz | |
| BOM Maximum output-swing bandwidth | $V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡, $A_V = 1$, $C_L = 100\text{ pF}$ ‡ | 25°C | | 185 | | | 185 | kHz | |
| t_s Settling time | $A_V = -1$, Step = 0.5 V to 2.5 V, $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | To 0.1% | | 6.4 | | | 6.4 | μs | |
| | | To 0.01% | | 14.1 | | | 14.1 | | |
| ϕ_m Phase margin at unity gain | $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | 25°C | | 56° | | | 56° | | |
| Gain margin | | 25°C | | 11 | | | 11 | dB | |

† Full range is – 40°C to 125°C.

‡ Referenced to 2.5 V

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TLV2264I electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T_A † | TLV2264I | | | TLV2264AI | | | UNIT |
|--|---|--|------------|-------------|------|-----------|-------------|---------------|------------------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{IO} Input offset voltage | | 25°C | 300 | 2500 | | 300 | 950 | μV | |
| | | Full range | | | 3000 | | 1500 | | |
| α_{VIO} Temperature coefficient of input offset voltage | | 25°C to 85°C | 2 | | | 2 | | | $\mu\text{V}/^\circ\text{C}$ |
| Input offset voltage long-term drift (see Note 4) | $V_{DD\pm} = \pm 1.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$ | 25°C | 0.003 | | | 0.003 | | | $\mu\text{V}/\text{mo}$ |
| I_{IO} Input offset current | | 25°C | 0.5 | 60 | | 0.5 | 60 | pA | |
| | | 85°C | | 150 | | | 150 | | |
| | | Full range | | 800 | | | 800 | | |
| I_{IB} Input bias current | | 25°C | 1 | 60 | | 1 | 60 | pA | |
| | | 85°C | | 150 | | | 150 | | |
| Full range | | 800 | | | | 800 | | | |
| V_{ICR} Common-mode input voltage range | $R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$ | 25°C | 0 to 2 | -0.3 to 2.2 | | 0 to 2 | -0.3 to 2.2 | V | |
| | | Full range | 0 to 1.7 | | | 0 to 1.7 | | | |
| V_{OH} High-level output voltage | $I_{OH} = -20\ \mu\text{A}$ | 25°C | 2.99 | | | 2.99 | | | V |
| | $I_{OH} = -100\ \mu\text{A}$ | 25°C | 2.85 | | | 2.85 | | | |
| | | Full range | 2.825 | | | 2.825 | | | |
| | $I_{OH} = -400\ \mu\text{A}$ | 25°C | 2.7 | | | 2.7 | | | |
| Full range | | 2.65 | | | 2.65 | | | | |
| V_{OL} Low-level output voltage | $V_{IC} = 1.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$ | 25°C | 10 | | | 10 | | | mV |
| | | 25°C | 100 | | | 100 | | | |
| | $V_{IC} = 1.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$ | Full range | 150 | | | 150 | | | |
| | | $V_{IC} = 1.5\text{ V}$, $I_{OL} = 1\text{ mA}$ | 25°C | 200 | | | 200 | | |
| Full range | 300 | | | 300 | | | | | |
| A_{VD} Large-signal differential voltage amplification | $V_{IC} = 1.5\text{ V}$, $V_O = 1\text{ to }2\text{ V}$ | $R_L = 50\ \text{k}\Omega$ ‡ | 25°C | 60 | 100 | | 60 | 100 | V/mV |
| | | | Full range | 30 | | | 30 | | |
| | | $R_L = 1\ \text{M}\Omega$ ‡ | 25°C | 100 | | | 100 | | |
| $r_{i(d)}$ Differential input resistance | | 25°C | 10^{12} | | | 10^{12} | | | Ω |
| $r_{i(c)}$ Common-mode input resistance | | 25°C | 10^{12} | | | 10^{12} | | | Ω |
| $c_{i(c)}$ Common-mode input capacitance | $f = 10\text{ kHz}$, N package | 25°C | 8 | | | 8 | | | pF |
| z_o Closed-loop output impedance | $f = 100\text{ kHz}$, $A_V = 10$ | 25°C | 270 | | | 270 | | | Ω |
| CMRR Common-mode rejection ratio | $V_{IC} = 0\text{ to }1.7\text{ V}$, $V_O = 1.5\text{ V}$, $R_S = 50\ \Omega$ | 25°C | 65 | 75 | | 65 | 77 | dB | |
| | | Full range | 60 | | | 60 | | | |
| k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | $V_{DD} = 2.7\text{ V to }8\text{ V}$, $V_{IC} = V_{DD}/2$, No load | 25°C | 80 | 95 | | 80 | 100 | dB | |
| | | Full range | 80 | | | 80 | | | |

† Full range is -40°C to 125°C .

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLV2264I electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted) (continued)

| PARAMETER | TEST CONDITIONS | T_A † | TLV2264I | | | TLV2264AI | | | UNIT |
|-----------|-------------------------------------|--------------------------------|------------|-----|-----|-----------|-----|-----|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| I_{DD} | Supply current (four amplifiers) | $V_O = 1.5\text{ V}$, No load | 25°C | 0.8 | 1 | 0.8 | 1 | mA | |
| | | | Full range | | 1 | | 1 | | |

† Full range is – 40°C to 125°C.

TLV2264I operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

| PARAMETER | TEST CONDITIONS | T_A † | TLV2264I | | | TLV2264AI | | | UNIT |
|-------------|--|------------|----------------|------|-------|-----------|------------------------|-----|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR | Slew rate at unity gain $V_O = 0.7\text{ V}$ to 1.7 V , $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | 25°C | 0.35 | 0.55 | 0.35 | 0.55 | V/ μs | | |
| | | Full range | 0.3 | | 0.3 | | | | |
| V_n | Equivalent input noise voltage $f = 10\text{ Hz}$ $f = 1\text{ kHz}$ | 25°C | | 43 | | 43 | nV/ $\sqrt{\text{Hz}}$ | | |
| | | 25°C | | 12 | | 12 | | | |
| $V_{N(PP)}$ | Peak-to-peak equivalent input noise voltage $f = 0.1\text{ Hz}$ to 1 Hz $f = 0.1\text{ Hz}$ to 10 Hz | 25°C | | 0.6 | | 0.6 | μV | | |
| | | 25°C | | 1 | | 1 | | | |
| I_n | Equivalent input noise current | 25°C | | 0.6 | | 0.6 | fA/ $\sqrt{\text{Hz}}$ | | |
| THD + N | Total harmonic distortion plus noise $V_O = 0.5\text{ V}$ to 2.5 V , $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega$ ‡ | 25°C | $A_V = 1$ | | 0.03% | | | | |
| | | | $A_V = 10$ | | 0.05% | | | | |
| | Gain-bandwidth product $f = 1\text{ kHz}$, $C_L = 100\text{ pF}$ ‡ | 25°C | | 0.67 | | 0.67 | MHz | | |
| B_{OM} | Maximum output-swing bandwidth $V_{O(PP)} = 1\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡ | 25°C | | 395 | | 395 | kHz | | |
| t_s | Settling time $A_V = -1$, Step = 1 V to 2 V , $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | 25°C | $T_o = 0.1\%$ | | 5.6 | | μs | | |
| | | | $T_o = 0.01\%$ | | 12.5 | | | | |
| ϕ_m | Phase margin at unity gain $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | 25°C | | 55° | | 55° | dB | | |
| | | 25°C | | 11 | | 11 | | | |

† Full range is – 40°C to 125°C.

‡ Referenced to 1.5 V

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TLV2264I electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T_A † | TLV2264I | | | TLV2264AI | | | UNIT |
|--|---|------------------------------|------------|-------------|----------|-----------|-------------|---------------|------------------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{IO} Input offset voltage | | 25°C | 300 | 2500 | | 300 | 950 | μV | |
| | | Full range | | | 3000 | | 1500 | | |
| α_{VIO} Temperature coefficient of input offset voltage | | 25°C to 85°C | 2 | | | 2 | | | $\mu\text{V}/^\circ\text{C}$ |
| Input offset voltage long-term drift (see Note 4) | $V_{DD\pm} = \pm 2.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$ | 25°C | 0.003 | | | 0.003 | | | $\mu\text{V}/\text{mo}$ |
| I_{IO} Input offset current | | 25°C | 0.5 | 60 | | 0.5 | 60 | pA | |
| | | 85°C | | 150 | | 150 | | | |
| | | Full range | | 800 | | 800 | | | |
| I_{IB} Input bias current | | 25°C | 1 | 60 | | 1 | 60 | pA | |
| | | 85°C | | 150 | | 150 | | | |
| | Full range | | 800 | | 800 | | | | |
| V_{ICR} Common-mode input voltage range | $ V_{IO} \leq 5\text{ mV}$, $R_S = 50\ \Omega$ | 25°C | 0 to 4 | -0.3 to 4.2 | | 0 to 4 | -0.3 to 4.2 | V | |
| | | Full range | 0 to 3.5 | | 0 to 3.5 | | | | |
| V_{OH} High-level output voltage | $I_{OH} = -20\ \mu\text{A}$ | 25°C | 4.99 | | 4.99 | | V | | |
| | | 25°C | 4.85 | 4.94 | 4.85 | 4.94 | | | |
| | | Full range | 4.82 | | 4.82 | | | | |
| | | 25°C | 4.7 | 4.85 | 4.7 | 4.85 | | | |
| V_{OL} Low-level output voltage | $V_{IC} = 2.5\text{ V}$, $I_{OL} = -400\ \mu\text{A}$ | 25°C | 0.01 | | 0.01 | | V | | |
| | | 25°C | 0.09 | 0.15 | 0.09 | 0.15 | | | |
| | | Full range | 0.15 | | 0.15 | | | | |
| | | 25°C | 0.2 | 0.3 | 0.2 | 0.3 | | | |
| A_{VD} Large-signal differential voltage amplification | $V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$ | $R_L = 50\ \text{k}\Omega$ ‡ | 25°C | 80 | 170 | 80 | 170 | V/mV | |
| | | | Full range | 55 | | 55 | | | |
| | | $R_L = 1\ \text{M}\Omega$ ‡ | 25°C | 550 | | 550 | | | |
| | | | Full range | 550 | | 550 | | | |
| $r_{i(d)}$ Differential input resistance | | 25°C | 10^{12} | | | 10^{12} | Ω | | |
| $r_{i(c)}$ Common-mode input resistance | | 25°C | 10^{12} | | | 10^{12} | Ω | | |
| $C_{i(c)}$ Common-mode input capacitance | $f = 10\ \text{kHz}$, N package | 25°C | 8 | | | 8 | pF | | |
| z_o Closed-loop output impedance | $f = 100\ \text{kHz}$, $A_V = 10$ | 25°C | 240 | | | 240 | Ω | | |
| CMRR Common-mode rejection ratio | $V_{IC} = 0\text{ to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$ | 25°C | 70 | 83 | | 70 | 83 | dB | |
| | | Full range | 70 | | 70 | | | | |
| k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | $V_{DD} = 4.4\text{ V to }8\text{ V}$, $V_{IC} = V_{DD}/2$, No load | 25°C | 80 | 95 | | 80 | 95 | dB | |
| | | Full range | 80 | | 80 | | | | |

† Full range is -40°C to 125°C .

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLV2264I electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted) (continued)

| PARAMETER | TEST CONDITIONS | T_A † | TLV2264I | | | TLV2264AI | | | UNIT |
|-----------|-------------------------------------|-----------------------------------|------------|-----|-----|-----------|-----|-----|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| I_{DD} | Supply current (four amplifiers) | $V_O = 2.5\text{ V}$, No load | 25°C | 0.8 | 1 | 0.8 | 1 | mA | |
| | | | Full range | | 1 | | 1 | | |

† Full range is – 40°C to 125°C.

TLV2264I operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

| PARAMETER | TEST CONDITIONS | T_A † | TLV2264I | | | TLV2264AI | | | UNIT | |
|-------------|---|---------------------------------------|-------------------------------------|------------|-------|-----------|--------|------------------|------|------------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| SR | Slew rate at unity gain $V_O = 1.4\text{ V to }2.6\text{ V}$, $C_L = 100\text{ pF}‡$ | $R_L = 50\text{ k}\Omega‡$ | 25°C | 0.35 | 0.55 | 0.35 | 0.55 | V/ μs | | |
| | | | Full range | 0.3 | | 0.3 | | | | |
| V_n | Equivalent input noise voltage | $f = 10\text{ Hz}$ | 25°C | 40 | | | 40 | | | nV/ $\sqrt{\text{Hz}}$ |
| | | | $f = 1\text{ kHz}$ | 12 | | | 12 | | | |
| $V_{N(PP)}$ | Peak-to-peak equivalent input noise voltage | $f = 0.1\text{ Hz to }1\text{ Hz}$ | 25°C | 0.7 | | | 0.7 | | | μV |
| | | | $f = 0.1\text{ Hz to }10\text{ Hz}$ | 1.3 | | | 1.3 | | | |
| I_n | Equivalent input noise current | | 25°C | 0.6 | | | 0.6 | | | fA/ $\sqrt{\text{Hz}}$ |
| THD + N | Total harmonic distortion plus noise $V_O = 0.5\text{ V to }2.5\text{ V}$, $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega‡$ | $A_V = 1$ | 25°C | 0.017% | | | 0.017% | | | |
| | | | | $A_V = 10$ | 0.03% | | | 0.03% | | |
| | Gain-bandwidth product $f = 50\text{ kHz}$, $C_L = 100\text{ pF}‡$ | $R_L = 50\text{ k}\Omega‡$ | 25°C | 0.71 | | | 0.71 | | | MHz |
| BOM | Maximum output-swing bandwidth $V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega‡$ | $A_V = 1$, $C_L = 100\text{ pF}‡$ | 25°C | 185 | | | 185 | | | kHz |
| t_s | Settling time $A_V = -1$, Step = 0.5 V to 2.5 V, $R_L = 50\text{ k}\Omega‡$, $C_L = 100\text{ pF}‡$ | To 0.1% | 25°C | 6.4 | | | 6.4 | | | μs |
| | | To 0.01% | | 14.1 | | | 14.1 | | | |
| ϕ_m | Phase margin at unity gain $R_L = 50\text{ k}\Omega‡$ | $C_L = 100\text{ pF}‡$ | 25°C | 56° | | | 56° | | | |
| | | | 25°C | 11 | | | 11 | | | |

† Full range is – 40°C to 125°C.

‡ Referenced to 2.5 V

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TLV2262Q and TLV2262M electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T_A † | TLV2262Q, TLV2262M | | | TLV2262AQ, TLV2262AM | | | UNIT | |
|--|--|------------------------------|-----------------------|-------------|-----|-------------------------|-------------|---------------|------------------------------|--|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| V_{IO} Input offset voltage | | 25°C | 300 | 2500 | | 300 | 950 | μV | | |
| | | Full range | | 3000 | | 1500 | | | | |
| α_{VIO} Temperature coefficient of input offset voltage | | 25°C to 125°C | 2 | | | 2 | | | $\mu\text{V}/^\circ\text{C}$ | |
| Input offset voltage long-term drift (see Note 4) | $V_{DD\pm} = \pm 1.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$ | 25°C | 0.003 | | | 0.003 | | | $\mu\text{V}/\text{mo}$ | |
| I_{IO} Input offset current | | 25°C | 0.5 | 60 | | 0.5 | 60 | pA | | |
| | | 125°C | | 800 | | 800 | | | | |
| I_{IB} Input bias current | | 25°C | 1 | 60 | | 1 | 60 | pA | | |
| | | 125°C | | 800 | | 800 | | | | |
| V_{ICR} Common-mode input voltage range | $R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$ | 25°C | 0 to 2 | -0.3 to 2.2 | | 0 to 2 | -0.3 to 2.2 | V | | |
| | | Full range | 0 to 1.7 | | | 0 to 1.7 | | | | |
| V_{OH} High-level output voltage | $I_{OH} = -20\ \mu\text{A}$ | 25°C | 2.99 | | | 2.99 | | | V | |
| | $I_{OH} = -100\ \mu\text{A}$ | 25°C | 2.85 | | | 2.85 | | | | |
| | $I_{OH} = -400\ \mu\text{A}$ | Full range | 2.82 | | | 2.82 | | | | |
| | | 25°C | 2.7 | | | 2.7 | | | | |
| V_{OL} Low-level output voltage | $V_{IC} = 1.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$ | 25°C | 10 | | | 10 | | | mV | |
| | $V_{IC} = 1.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$ | 25°C | 100 | 150 | | 100 | 150 | | | |
| | | Full range | 165 | | | 165 | | | | |
| | $V_{IC} = 1.5\text{ V}$, $I_{OL} = 1\text{ mA}$ | 25°C | 200 | 300 | | 200 | 300 | | | |
| A_{VD} Large-signal differential voltage amplification | $V_{IC} = 1.5\text{ V}$, $V_O = 1\text{ V to } 2\text{ V}$ | $R_L = 50\ \text{k}\Omega$ ‡ | 25°C | 60 | 100 | | 60 | 100 | V/mV | |
| | | $R_L = 1\ \text{M}\Omega$ ‡ | Full range | 25 | | | 25 | | | |
| | | | 25°C | 100 | | | 100 | | | |
| $r_{i(d)}$ Differential input resistance | | 25°C | 10^{12} | | | 10^{12} | | | Ω | |
| $r_{i(c)}$ Common-mode input resistance | | 25°C | 10^{12} | | | 10^{12} | | | Ω | |
| $C_{i(c)}$ Common-mode input capacitance | $f = 10\ \text{kHz}$, P package | 25°C | 8 | | | 8 | | | pF | |
| z_o Closed-loop output impedance | $f = 100\ \text{kHz}$, $A_V = 10$ | 25°C | 270 | | | 270 | | | Ω | |
| CMRR Common-mode rejection ratio | $V_{IC} = 0\text{ to } 1.7\text{ V}$, $V_O = 1.5\text{ V}$, $R_S = 50\ \Omega$ | 25°C | 65 | 75 | | 65 | 77 | dB | | |
| | | Full range | 60 | | | 60 | | | | |
| k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | $V_{DD} = 2.7\text{ V to } 8\text{ V}$, $V_{IC} = V_{DD}/2$, No load | 25°C | 80 | 95 | | 80 | 100 | dB | | |
| | | Full range | 80 | | | 80 | | | | |

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLV2262Q and TLV2262M electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted) (continued)

| PARAMETER | TEST CONDITIONS | T_A † | TLV2262Q, TLV2262M | | | TLV2262AQ, TLV2262AM | | | UNIT |
|-------------------------|--------------------------------|------------|-----------------------|-----|-----|-------------------------|-----|---------------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| I_{DD} Supply current | $V_O = 1.5\text{ V}$, No load | 25°C | 400 | 500 | | 400 | 500 | μA | |
| | | Full range | | 500 | | | 500 | | |

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

TLV2262Q and TLV2262M operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

| PARAMETER | TEST CONDITIONS | T_A † | TLV2262Q, TLV2262M | | | TLV2262AQ, TLV2262AM | | | UNIT |
|---|--|--|-----------------------|-------|------|-------------------------|-------|------------------------------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR Slew rate at unity gain | $V_O = 0.5\text{ V}$ to 1.7 V , $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | 25°C | 0.35 | 0.55 | | 0.35 | 0.55 | $\text{V}/\mu\text{s}$ | |
| | | Full range | 0.25 | | | 0.25 | | | |
| V_n Equivalent input noise voltage | $f = 10\text{ Hz}$ | 25°C | | 43 | | | 43 | $\text{nV}/\sqrt{\text{Hz}}$ | |
| | $f = 1\text{ kHz}$ | 25°C | | 12 | | | 12 | | |
| $V_{N(PP)}$ Peak-to-peak equivalent input noise voltage | $f = 0.1\text{ Hz}$ to 1 Hz | 25°C | | 0.6 | | | 0.6 | μV | |
| | $f = 0.1\text{ Hz}$ to 10 Hz | 25°C | | 1 | | | 1 | | |
| I_n Equivalent input noise current | | 25°C | | 0.6 | | | 0.6 | $\text{fA}/\sqrt{\text{Hz}}$ | |
| THD + N Total harmonic distortion plus noise | $V_O = 0.5\text{ V}$ to 2.5 V , $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega$ ‡ | $A_V = 1$ | | 0.03% | | | 0.03% | | |
| | | $A_V = 10$ | | 0.05% | | | 0.05% | | |
| Gain-bandwidth product | $f = 1\text{ kHz}$, $C_L = 100\text{ pF}$ ‡ | $R_L = 50\text{ k}\Omega$ ‡, | 25°C | | 0.67 | | 0.67 | MHz | |
| BOM Maximum output-swing bandwidth | $V_{O(PP)} = 1\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡, | $A_V = 1$, $C_L = 100\text{ pF}$ ‡ | 25°C | | 395 | | 395 | kHz | |
| t_s Settling time | $A_V = -1$, Step = 1 V to 2 V , $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | $T_o = 0.1\%$ | 25°C | | 5.6 | | 5.6 | μs | |
| | | $T_o = 0.01\%$ | | | 12.5 | | 12.5 | | |
| ϕ_m Phase margin at unity gain | $R_L = 50\text{ k}\Omega$ ‡, | $C_L = 100\text{ pF}$ ‡ | 25°C | | 55° | | 55° | | |
| Gain margin | | | 25°C | | 11 | | 11 | | dB |

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 1.5 V

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TLV2262Q and TLV2262M electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T_A † | TLV2262Q, TLV2262M | | | TLV2262AQ, TLV2262AM | | | UNIT |
|--|--|------------------------------|-----------------------|-------------|-----------|-------------------------|-------------|---------------|------------------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{IO} Input offset voltage | $V_{DD} = \pm 2.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$ | 25°C | 300 | 2500 | | 300 | 950 | μV | |
| | | Full range | | 3000 | | 1500 | | | |
| α_{VIO} Temperature coefficient of input offset voltage | | 25°C to 125°C | 2 | | | 2 | | | $\mu\text{V}/^\circ\text{C}$ |
| Input offset voltage long-term drift (see Note 4) | | 25°C | 0.003 | | | 0.003 | | | $\mu\text{V}/\text{mo}$ |
| I_{IO} Input offset current | | 25°C | 0.5 | 60 | | 0.5 | 60 | pA | |
| | | 125°C | 800 | | | 800 | | | |
| I_{IB} Input bias current | | 25°C | 1 | 60 | | 1 | 60 | pA | |
| | | 125°C | 800 | | | 800 | | | |
| V_{ICR} Common-mode input voltage range | $ V_{IO} \leq 5\text{ mV}$, $R_S = 50\ \Omega$ | 25°C | 0 to 4 | -0.3 to 4.2 | | 0 to 4 | -0.3 to 4.2 | V | |
| | | Full range | 0 to 3.5 | | 0 to 3.5 | | | | |
| V_{OH} High-level output voltage | $I_{OH} = -20\ \mu\text{A}$ | 25°C | 4.99 | | 4.99 | | V | | |
| | $I_{OH} = -100\ \mu\text{A}$ | 25°C | 4.85 | 4.94 | 4.85 | 4.94 | | | |
| | $I_{OH} = -400\ \mu\text{A}$ | Full range | 4.82 | | 4.82 | | | | |
| | | 25°C | 4.7 | 4.85 | 4.7 | 4.85 | | | |
| V_{OL} Low-level output voltage | $V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$ | 25°C | 0.01 | | 0.01 | | V | | |
| | | 25°C | 0.09 | 0.15 | 0.09 | 0.15 | | | |
| | $V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$ | Full range | 0.15 | | 0.15 | | | | |
| | | 25°C | 0.2 | 0.3 | 0.2 | 0.3 | | | |
| A_{VD} Large-signal differential voltage amplification | $V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$ | $R_L = 50\ \text{k}\Omega$ ‡ | 25°C | 80 | 170 | 80 | 170 | V/mV | |
| | | $R_L = 1\ \text{M}\Omega$ ‡ | Full range | 50 | | 50 | | | |
| | | | 25°C | 550 | | 550 | | | |
| $r_{i(d)}$ Differential input resistance | | 25°C | 10^{12} | | 10^{12} | | Ω | | |
| $r_{i(c)}$ Common-mode input resistance | | 25°C | 10^{12} | | 10^{12} | | Ω | | |
| $C_{i(c)}$ Common-mode input capacitance | $f = 10\ \text{kHz}$, P package | 25°C | 8 | | 8 | | pF | | |
| Z_o Closed-loop output impedance | $f = 100\ \text{kHz}$, $A_V = 10$ | 25°C | 240 | | 240 | | Ω | | |
| CMRR Common-mode rejection ratio | $V_{IC} = 0\text{ to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$ | 25°C | 70 | 83 | 70 | 83 | dB | | |
| | | Full range | 70 | | 70 | | | | |
| k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | $V_{DD} = 4.4\text{ V to }8\text{ V}$, $V_{IC} = V_{DD}/2$, No load | 25°C | 80 | 95 | 80 | 95 | dB | | |
| | | Full range | 80 | | 80 | | | | |

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLV2262Q and TLV2262M electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted) (continued)

| PARAMETER | TEST CONDITIONS | T_A † | TLV2262Q, TLV2262M | | | TLV2262AQ, TLV2262AM | | | UNIT |
|-------------------------|--------------------------------|------------|-----------------------|-----|-----|-------------------------|-----|---------------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| I_{DD} Supply current | $V_O = 2.5\text{ V}$, No load | 25°C | 400 | 500 | | 400 | 500 | μA | |
| | | Full range | | 500 | | | 500 | | |

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

TLV2262Q and TLV2262M operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

| PARAMETER | TEST CONDITIONS | T_A † | TLV2262Q, TLV2262M | | | TLV2262AQ, TLV2262AM | | | UNIT |
|---|--|--|-----------------------|------|--------|-------------------------|------------------------------|------------------------------|------------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR Slew rate at unity gain | $V_O = 0.5\text{ V}$ to 3.5 V , $C_L = 100\text{ pF}$ ‡ | $R_L = 50\text{ k}\Omega$ ‡ | 25°C | 0.35 | 0.55 | | 0.35 | 0.55 | $\text{V}/\mu\text{s}$ |
| | | | Full range | 0.25 | | | 0.25 | | |
| V_n Equivalent input noise voltage | $f = 10\text{ Hz}$ $f = 1\text{ kHz}$ | 25°C | | 40 | | 40 | | $\text{nV}/\sqrt{\text{Hz}}$ | |
| | | | | 12 | | 12 | | | |
| $V_{N(PP)}$ Peak-to-peak equivalent input noise voltage | $f = 0.1\text{ Hz}$ to 1 Hz $f = 0.1\text{ Hz}$ to 10 Hz | 25°C | | 0.7 | | 0.7 | | μV | |
| | | | | 1.3 | | 1.3 | | | |
| I_n Equivalent input noise current | | 25°C | | 0.6 | | 0.6 | $\text{fA}/\sqrt{\text{Hz}}$ | | |
| THD + N Total harmonic distortion plus noise | $V_O = 0.5\text{ V}$ to 2.5 V , $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega$ ‡ | $A_V = 1$ $A_V = 10$ | 25°C | | 0.017% | | 0.017% | | |
| | | | | | 0.03% | | 0.03% | | |
| Gain-bandwidth product | $f = 50\text{ kHz}$, $C_L = 100\text{ pF}$ ‡ | $R_L = 50\text{ k}\Omega$ ‡ | 25°C | | 0.71 | | 0.71 | MHz | |
| B_{OM} Maximum output-swing bandwidth | $V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡ | $A_V = 1$, $C_L = 100\text{ pF}$ ‡ | 25°C | | 185 | | 185 | kHz | |
| t_s Settling time | $A_V = -1$, Step = 0.5 V to 2.5 V , $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | To 0.1% | 25°C | | 6.4 | | 6.4 | μs | |
| | | To 0.01% | | | 14.1 | | 14.1 | | |
| ϕ_m Phase margin at unity gain Gain margin | $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | 25°C | | 56° | | 56° | dB | | |
| | | | | 11 | | 11 | | | |

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

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TLV2264Q and TLV2264M electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T_A † | TLV2264Q, TLV2264M | | | TLV2264AQ, TLV2264AM | | | UNIT | |
|--|--|--|-----------------------|----------|-------------|-------------------------|-------------|-----|------------------------------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| V_{IO} Input offset voltage | | 25°C | 300 | | 2500 | 300 | | 950 | μV | |
| | | Full range | 3000 | | | 1500 | | | | |
| α_{VIO} Temperature coefficient of input offset voltage | | 25°C to 125°C | 2 | | | 2 | | | $\mu\text{V}/^\circ\text{C}$ | |
| Input offset voltage long-term drift (see Note 4) | $V_{DD} = \pm 1.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$ | 25°C | 0.003 | | | 0.003 | | | $\mu\text{V}/\text{mo}$ | |
| I_{IO} Input offset current | | 25°C | 0.5 | 60 | | 0.5 | 60 | | pA | |
| | | 125°C | 800 | | | 800 | | | | |
| I_{IB} Input bias current | | 25°C | 1 | | 60 | 1 | | 60 | pA | |
| | | 125°C | 800 | | | 800 | | | | |
| V_{ICR} Common-mode input voltage range | | $R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$ | 25°C | 0 to 2 | -0.3 to 2.2 | 0 to 2 | -0.3 to 2.2 | | V | |
| | Full range | | 0 to 1.7 | 0 to 1.7 | | | | | | |
| V_{OH} High-level output voltage | $I_{OH} = -20\ \mu\text{A}$ | 25°C | 2.99 | | | 2.99 | | | V | |
| | $I_{OH} = -100\ \mu\text{A}$ | 25°C | 2.85 | | | 2.85 | | | | |
| | $I_{OH} = -400\ \mu\text{A}$ | Full range | 2.82 | | | 2.82 | | | | |
| | | 25°C | 2.7 | | 300 | 2.7 | | 300 | | |
| V_{OL} Low-level output voltage | $V_{IC} = 1.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$ | 25°C | 10 | | | 10 | | | mV | |
| | $V_{IC} = 1.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$ | 25°C | 100 | 150 | | 100 | 150 | | | |
| | | Full range | 150 | | | 150 | | | | |
| | $V_{IC} = 1.5\text{ V}$, $I_{OL} = 1\text{ mA}$ | 25°C | 200 | 300 | | 200 | 300 | | | |
| Full range | | 300 | | | 300 | | | | | |
| AVD Large-signal differential voltage amplification | $V_{IC} = 1.5\text{ V}$, $V_O = 1\text{ V to }2\text{ V}$ | $R_L = 50\ \text{k}\Omega$ ‡ | 25°C | 60 | 100 | | 60 | 100 | | V/mV |
| | | | Full range | 25 | | | 25 | | | |
| | | $R_L = 1\ \text{M}\Omega$ ‡ | 25°C | 100 | | | 100 | | | |
| $r_{i(d)}$ Differential input resistance | | 25°C | 10^{12} | | | 10^{12} | | | Ω | |
| $r_{i(c)}$ Common-mode input resistance | | 25°C | 10^{12} | | | 10^{12} | | | Ω | |
| $c_{i(c)}$ Common-mode input capacitance | $f = 10\text{ kHz}$, N package | 25°C | 8 | | | 8 | | | pF | |
| z_o Closed-loop output impedance | $f = 100\text{ kHz}$, $A_V = 10$ | 25°C | 270 | | | 270 | | | Ω | |
| CMRR Common-mode rejection ratio | $V_{IC} = 0\text{ to }1.7\text{ V}$, $V_O = 1.5\text{ V}$, $R_S = 50\ \Omega$ | 25°C | 65 | 75 | | 65 | 77 | | dB | |
| | | Full range | 60 | | | 60 | | | | |
| k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | $V_{DD} = 2.7\text{ V to }8\text{ V}$, $V_{IC} = V_{DD}/2$, No load | 25°C | 80 | 95 | | 80 | 100 | | dB | |
| | | Full range | 80 | | | 80 | | | | |

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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TLV2264Q and TLV2264M electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted) (continued)

| PARAMETER | TEST CONDITIONS | T_A † | TLV2264Q, TLV2264M | | | TLV2264AQ, TLV2264AM | | | UNIT |
|-----------|--|------------|-----------------------|-----|-----|-------------------------|-----|-----|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| I_{DD} | Supply current (four amplifiers) $V_O = 1.5\text{ V}$, No load | 25°C | 0.8 | | 1 | 0.8 | | 1 | mA |
| | | Full range | | | 1 | | | 1 | |

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

TLV2264Q and TLV2264M operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

| PARAMETER | TEST CONDITIONS | T_A † | TLV2264Q, TLV2264M | | | TLV2264AQ, TLV2264AM | | | UNIT | |
|-------------|--|--|-----------------------|------|-----|-------------------------|------|-----|------------------------------|---------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| SR | Slew rate at unity gain $V_O = 0.5\text{ V}$ to 1.7 V , $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | 25°C | 0.35 | 0.55 | | 0.35 | 0.55 | | $\text{V}/\mu\text{s}$ | |
| | | Full range | 0.25 | | | 0.25 | | | | |
| V_n | Equivalent input noise voltage | $f = 10\text{ Hz}$ | 25°C | | | 43 | | | $\text{nV}/\sqrt{\text{Hz}}$ | |
| | | $f = 1\text{ kHz}$ | 25°C | | | 12 | | | | |
| $V_{N(PP)}$ | Peak-to-peak equivalent input noise voltage | $f = 0.1\text{ Hz}$ to 1 Hz | 25°C | | | 0.6 | | | μV | |
| | | $f = 0.1\text{ Hz}$ to 10 Hz | 25°C | | | 1 | | | | |
| I_n | Equivalent input noise current | 25°C | 0.6 | | | 0.6 | | | $\text{fA}/\sqrt{\text{Hz}}$ | |
| THD + N | Total harmonic distortion plus noise $V_O = 0.5\text{ V}$ to 2.5 V , $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega$ ‡ | $A_V = 1$ | 25°C | | | 0.03% | | | | |
| | | $A_V = 10$ | 25°C | | | 0.05% | | | | |
| | Gain-bandwidth product | $f = 1\text{ kHz}$, $C_L = 100\text{ pF}$ ‡ | 25°C | | | 0.67 | | | MHz | |
| B_{OM} | Maximum output-swing bandwidth | $V_{O(PP)} = 1\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | 25°C | | | 395 | | | kHz | |
| t_s | Settling time | $A_V = -1$, Step = 1 V to 2 V , $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | $T_o = 0.1\%$ | 25°C | | | 5.6 | | | μs |
| | | | $T_o = 0.01\%$ | 25°C | | | 12.5 | | | |
| ϕ_m | Phase margin at unity gain | $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | 25°C | | | 55° | | | | |
| | Gain margin | | 25°C | | | 11 | | | | |

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 1.5 V

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TLV2264Q and TLV2264M electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T_A † | TLV2264Q, TLV2264M | | | TLV2264AQ, TLV2264AM | | | UNIT |
|--|--|-----------------------------|-----------------------|-------------|-----|-------------------------|-------------|---------------|------------------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{IO} Input offset voltage | | 25°C | 300 | 2500 | | 300 | 950 | μV | |
| | | Full range | | 3000 | | 1500 | | | |
| α_{VIO} Temperature coefficient of input offset voltage | $V_{DD} \pm = \pm 2.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$ | 25°C to 125°C | 2 | | | 2 | | | $\mu\text{V}/^\circ\text{C}$ |
| Input offset voltage long-term drift (see Note 4) | | 25°C | 0.003 | | | 0.003 | | | $\mu\text{V}/\text{mo}$ |
| I_{IO} Input offset current | | 25°C | 0.5 | 60 | | 0.5 | 60 | pA | |
| | | 125°C | | 800 | | 800 | | | |
| I_{IB} Input bias current | 25°C | 1 | 60 | | 1 | 60 | pA | | |
| | 125°C | | 800 | | 800 | | | | |
| V_{ICR} Common-mode input voltage range | $ V_{IO} \leq 5\text{ mV}$, $R_S = 50\ \Omega$ | 25°C | 0 to 4 | -0.3 to 4.2 | | 0 to 4 | -0.3 to 4.2 | V | |
| | | Full range | 0 to 3.5 | | | 0 to 3.5 | | | |
| V_{OH} High-level output voltage | $I_{OH} = -20\ \mu\text{A}$ | 25°C | 4.99 | | | 4.99 | | | V |
| | $I_{OH} = -100\ \mu\text{A}$ | 25°C | 4.85 | 4.94 | | 4.85 | 4.94 | | |
| | $I_{OH} = -400\ \mu\text{A}$ | Full range | 4.82 | | | 4.82 | | | |
| | | 25°C | 4.7 | 4.85 | | 4.7 | 4.85 | | |
| V_{OL} Low-level output voltage | $V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$ | 25°C | 0.01 | | | 0.01 | | | V |
| | | 25°C | 0.09 | 0.15 | | 0.09 | 0.15 | | |
| | $V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$ | Full range | 0.15 | | | 0.15 | | | |
| | | 25°C | 0.2 | 0.3 | | 0.2 | 0.3 | | |
| V_{OL} Low-level output voltage | $V_{IC} = 2.5\text{ V}$, $I_{OL} = 1\text{ mA}$ | 25°C | 0.2 | 0.3 | | 0.2 | 0.3 | V | |
| | | Full range | 0.3 | | | 0.3 | | | |
| | | 25°C | 80 | 170 | | 80 | 170 | | |
| AVD Large-signal differential voltage amplification | $V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$ | $R_L = 50\text{ k}\Omega$ ‡ | 25°C | 80 | 170 | | 80 | 170 | V/mV |
| | | | Full range | 50 | | | 50 | | |
| | | $R_L = 1\text{ M}\Omega$ ‡ | 25°C | 550 | | | 550 | | |
| $r_{i(d)}$ Differential input resistance | | 25°C | 10^{12} | | | 10^{12} | | | Ω |
| $r_{i(c)}$ Common-mode input resistance | | 25°C | 10^{12} | | | 10^{12} | | | Ω |
| $C_{i(c)}$ Common-mode input capacitance | $f = 10\text{ kHz}$, N package | 25°C | 8 | | | 8 | | | pF |
| z_o Closed-loop output impedance | $f = 100\text{ kHz}$, $A_V = 10$ | 25°C | 240 | | | 240 | | | Ω |
| CMRR Common-mode rejection ratio | $V_{IC} = 0\text{ to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$ | 25°C | 70 | 83 | | 70 | 83 | dB | |
| | | Full range | 70 | | | 70 | | | |
| k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | $V_{DD} = 4.4\text{ V to }8\text{ V}$, $V_{IC} = V_{DD}/2$, No load | 25°C | 80 | 95 | | 80 | 95 | dB | |
| | | Full range | 80 | | | 80 | | | |

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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TLV2264Q and TLV2264M electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted) (continued)

| PARAMETER | TEST CONDITIONS | T_A † | TLV2264Q, TLV2264M | | | TLV2264AQ, TLV2264AM | | | UNIT |
|-----------|----------------------------------|--------------------------------|--------------------|-----|-----|----------------------|-----|-----|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| I_{DD} | Supply current (four amplifiers) | $V_O = 2.5\text{ V}$, No load | 25°C | 0.8 | 1 | 0.8 | 1 | mA | |
| | | | Full range | | 1 | | 1 | | |

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

TLV2264Q and TLV2264M operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

| PARAMETER | TEST CONDITIONS | T_A † | TLV2264Q, TLV2264M | | | TLV2264AQ, TLV2264AM | | | UNIT | |
|-------------|---|---|---------------------------------------|-------------|------|----------------------|------|------------------|------|------------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| SR | Slew rate at unity gain | $V_O = 0.5\text{ V}$ to 3.5 V , $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | 25°C | 0.35 | 0.55 | 0.35 | 0.55 | V/ μs | | |
| | | | Full range | 0.25 | | 0.25 | | | | |
| V_n | Equivalent input noise voltage | $f = 10\text{ Hz}$ | 25°C | 40 | | | 40 | | | nV/ $\sqrt{\text{Hz}}$ |
| | | | $f = 1\text{ kHz}$ | 12 | | | 12 | | | |
| $V_{N(PP)}$ | Peak-to-peak equivalent input noise voltage | $f = 0.1\text{ Hz}$ to 1 Hz | 25°C | 0.7 | | | 0.7 | | | μV |
| | | | $f = 0.1\text{ Hz}$ to 10 Hz | 1.3 | | | 1.3 | | | |
| I_n | Equivalent input noise current | | 25°C | 0.6 | | | 0.6 | | | fA/ $\sqrt{\text{Hz}}$ |
| THD + N | Total harmonic distortion plus noise | $V_O = 0.5\text{ V}$ to 2.5 V , $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega$ ‡ | 25°C | $A_V = 1$ | | 0.017% | | 0.017% | | |
| | | | | $A_V = 10$ | | 0.03% | | 0.03% | | |
| | Gain-bandwidth product | $f = 50\text{ kHz}$, $C_L = 100\text{ pF}$ ‡, $R_L = 50\text{ k}\Omega$ ‡ | 25°C | 0.71 | | | 0.71 | | | MHz |
| BOM | Maximum output-swing bandwidth | $V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡, $A_V = 1$, $C_L = 100\text{ pF}$ ‡ | 25°C | 185 | | | 185 | | | kHz |
| t_s | Settling time | $A_V = -1$, Step = 0.5 V to 2.5 V , $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | 25°C | T_o 0.1% | | 6.4 | | 6.4 | | μs |
| | | | | T_o 0.01% | | 14.1 | | 14.1 | | |
| ϕ_m | Phase margin at unity gain | $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | 25°C | 56° | | | 56° | | | |
| | Gain margin | | 25°C | 11 | | | 11 | | | |

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 2.5 V



TLV226x, TLV226xA
Advanced LinCMOS™ RAIL-TO-RAIL
OPERATIONAL AMPLIFIERS

SLOS186C – FEBRUARY 1997 – REVISED AUGUST 2006

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2262
 INPUT OFFSET VOLTAGE

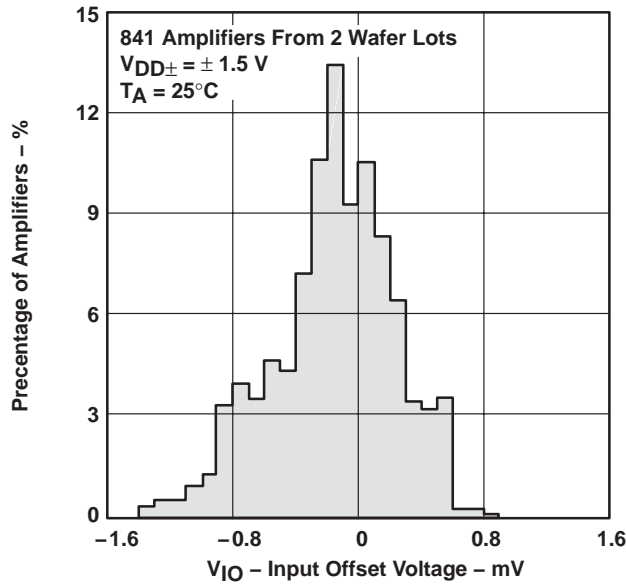


Figure 2

DISTRIBUTION OF TLV2262
 INPUT OFFSET VOLTAGE

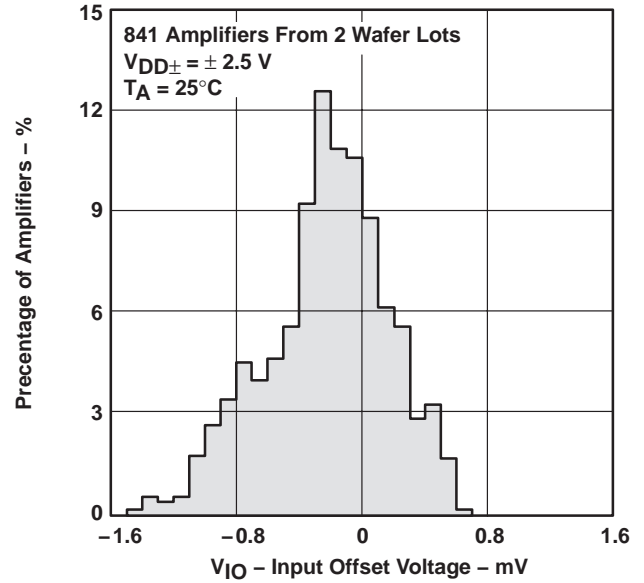


Figure 3

DISTRIBUTION OF TLV2264
 INPUT OFFSET VOLTAGE

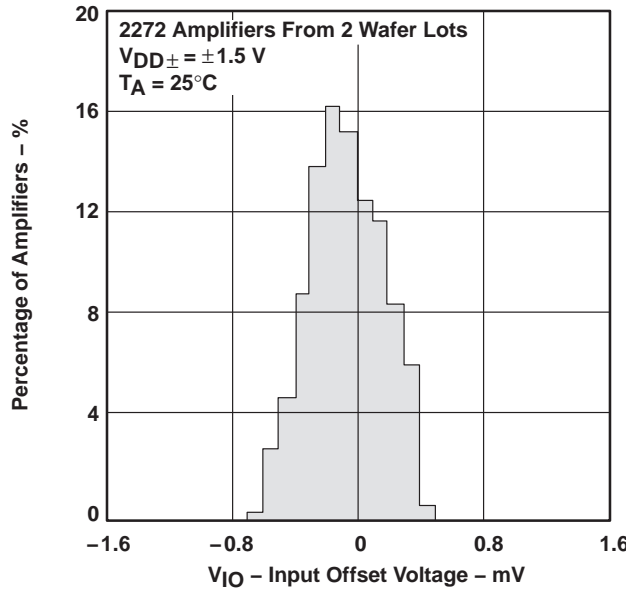


Figure 4

DISTRIBUTION OF TLV2264
 INPUT OFFSET VOLTAGE

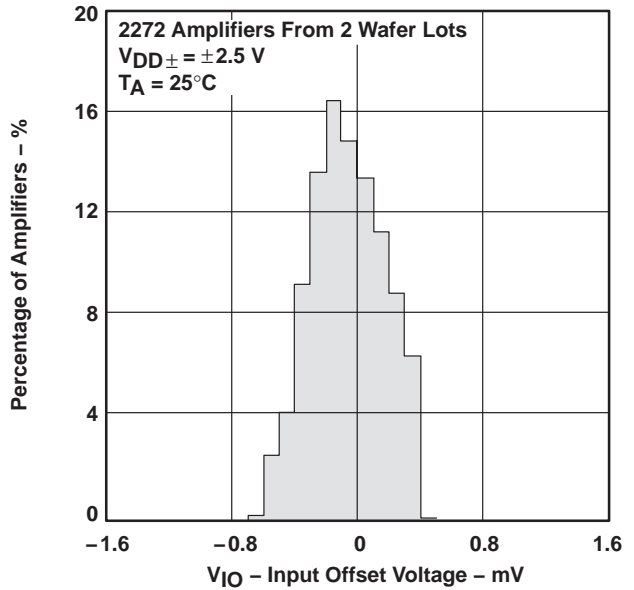


Figure 5

TYPICAL CHARACTERISTICS

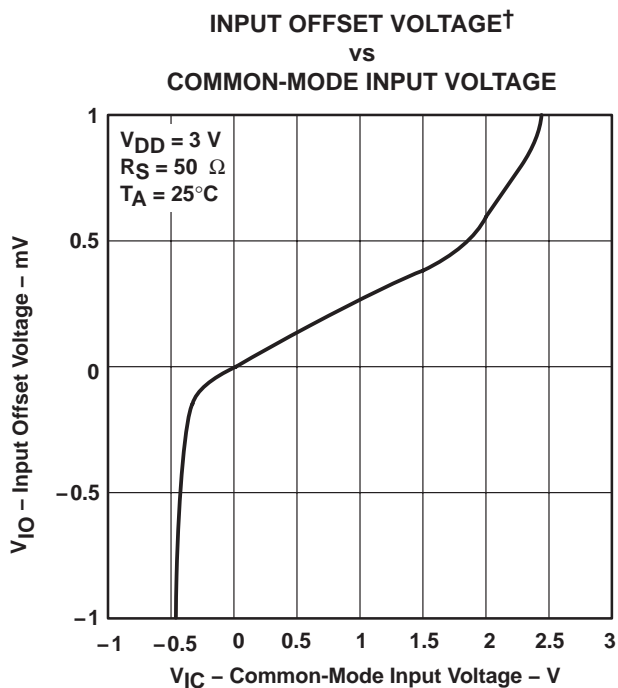


Figure 6

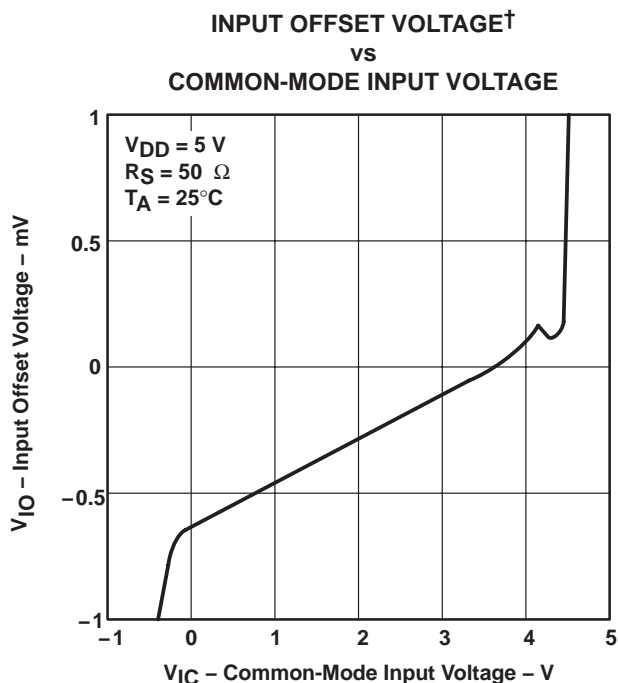


Figure 7

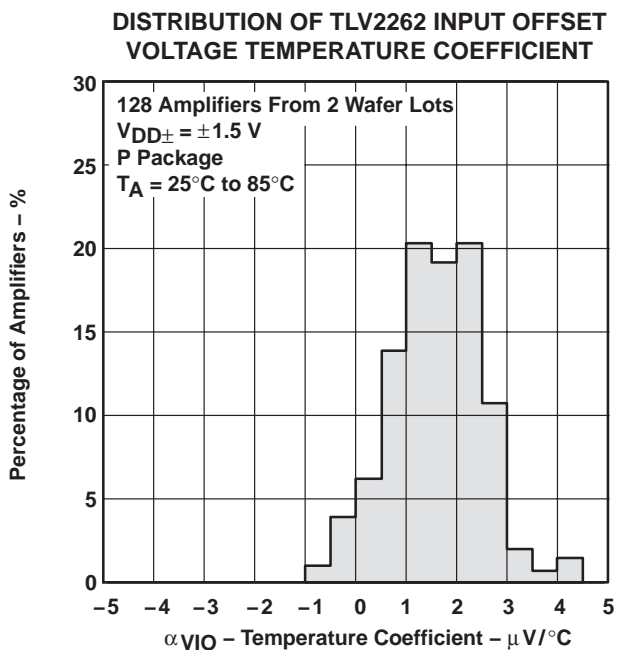


Figure 8

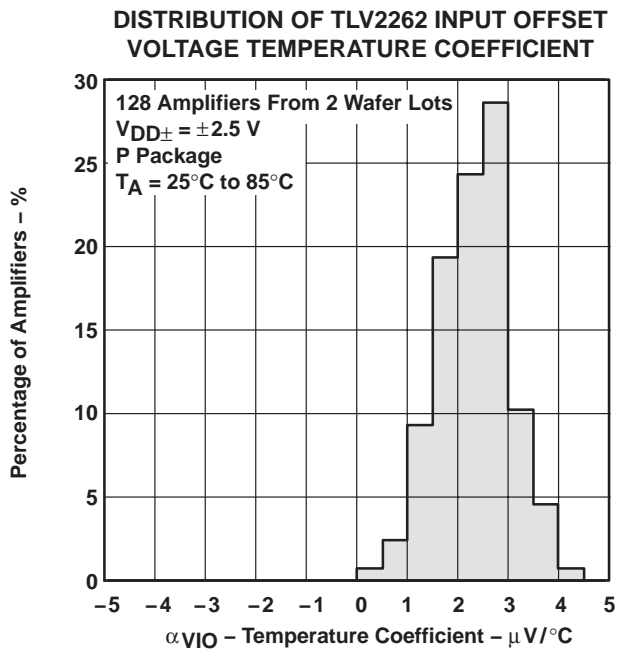


Figure 9

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

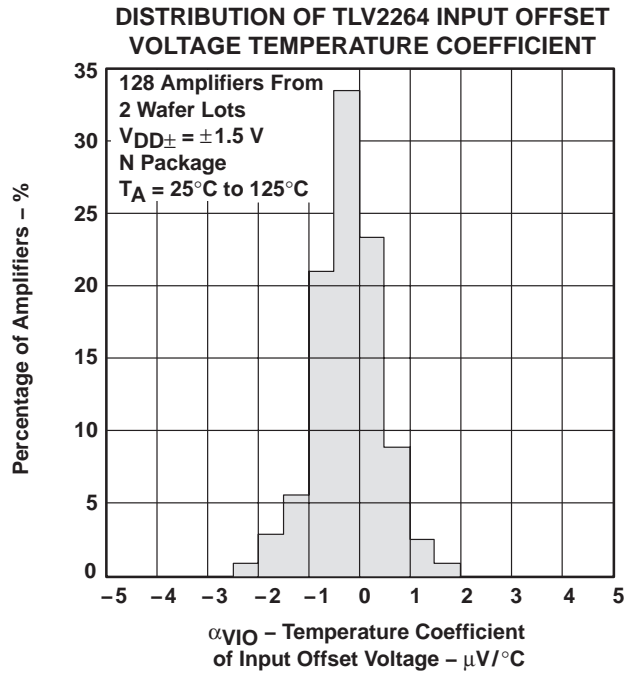


Figure 10

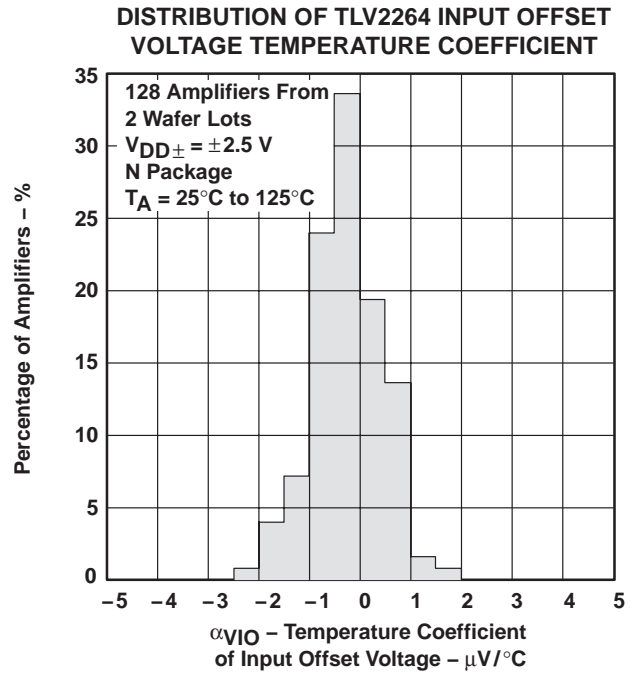


Figure 11

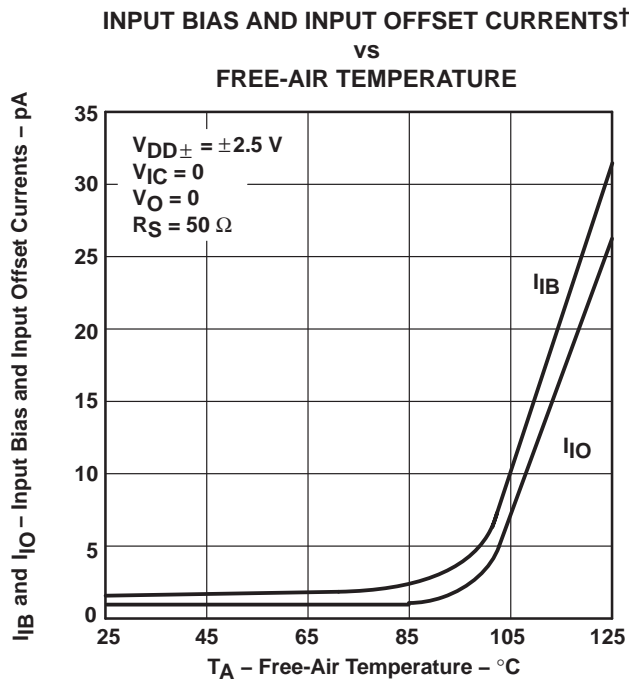


Figure 12

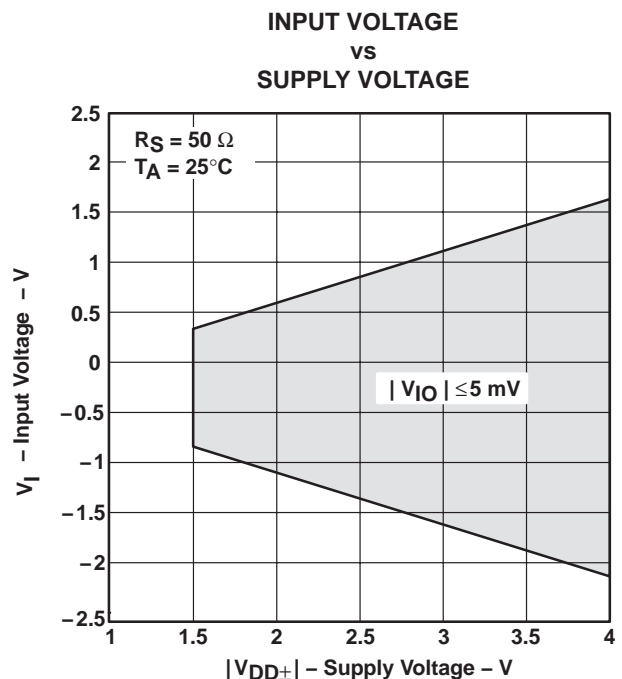


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

**INPUT VOLTAGE†‡
 vs
 FREE-AIR TEMPERATURE**

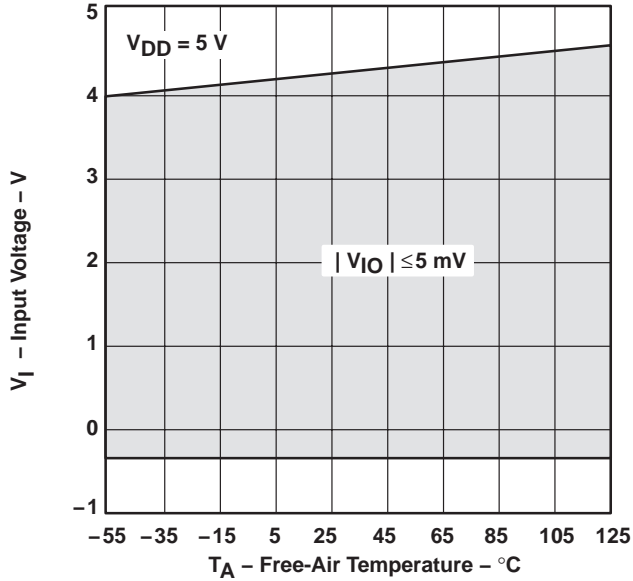


Figure 14

**HIGH-LEVEL OUTPUT VOLTAGE†‡
 vs
 HIGH-LEVEL OUTPUT CURRENT**

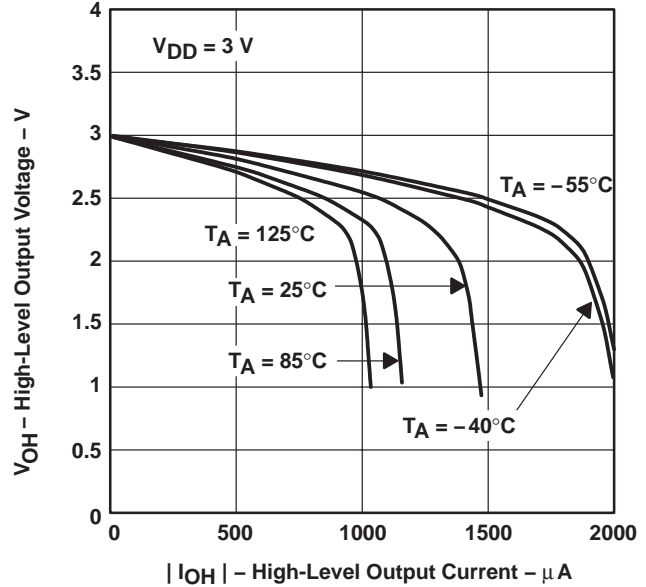


Figure 15

**LOW-LEVEL OUTPUT VOLTAGE†
 vs
 LOW-LEVEL OUTPUT CURRENT**

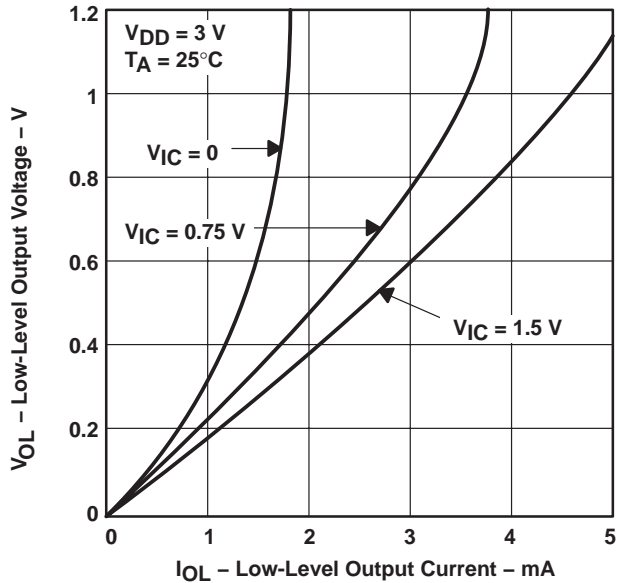


Figure 16

**LOW-LEVEL OUTPUT VOLTAGE†‡
 vs
 LOW-LEVEL OUTPUT CURRENT**

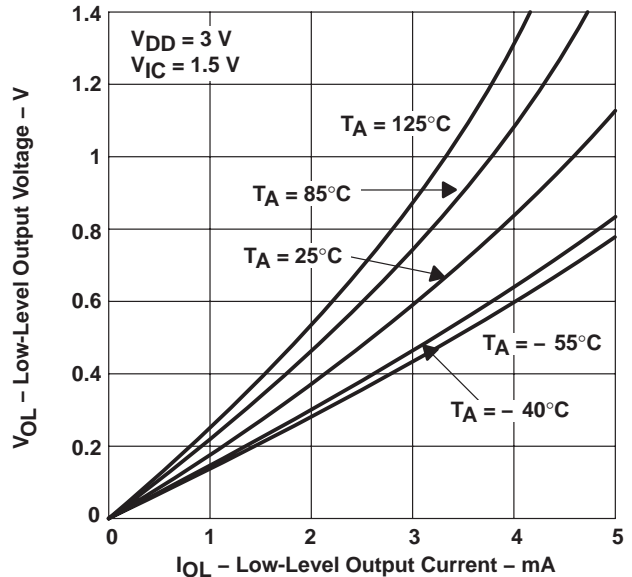


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

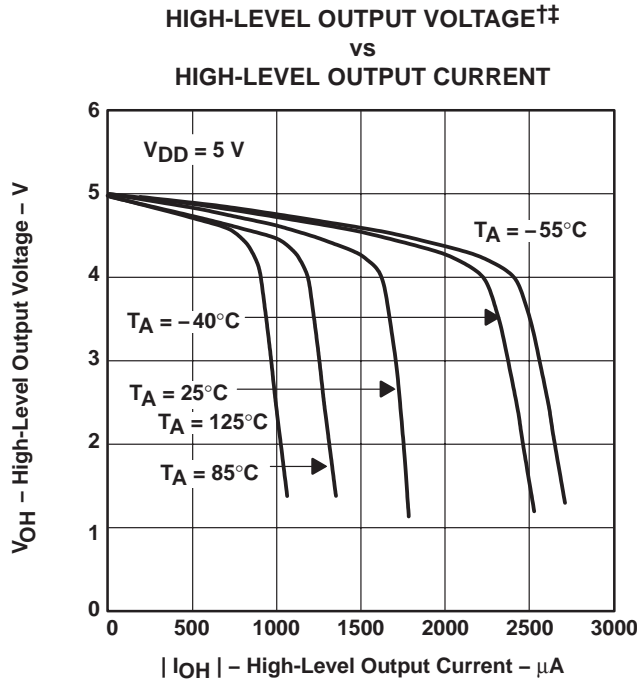


Figure 18

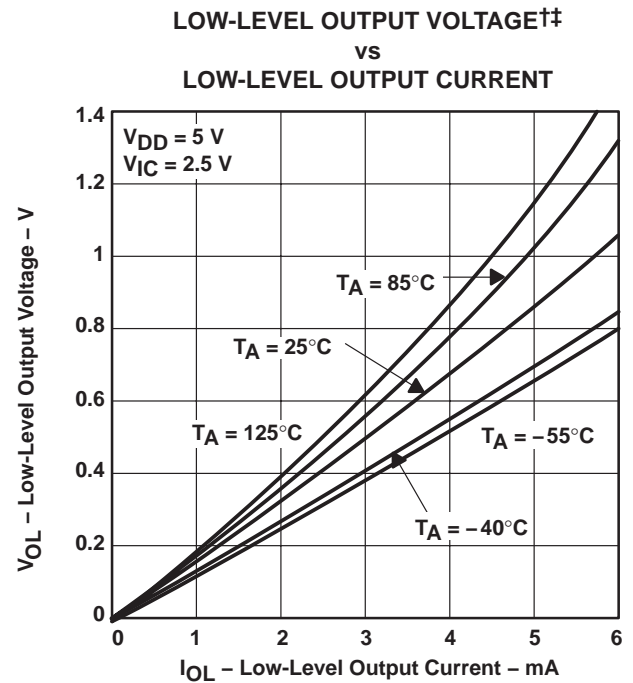


Figure 19

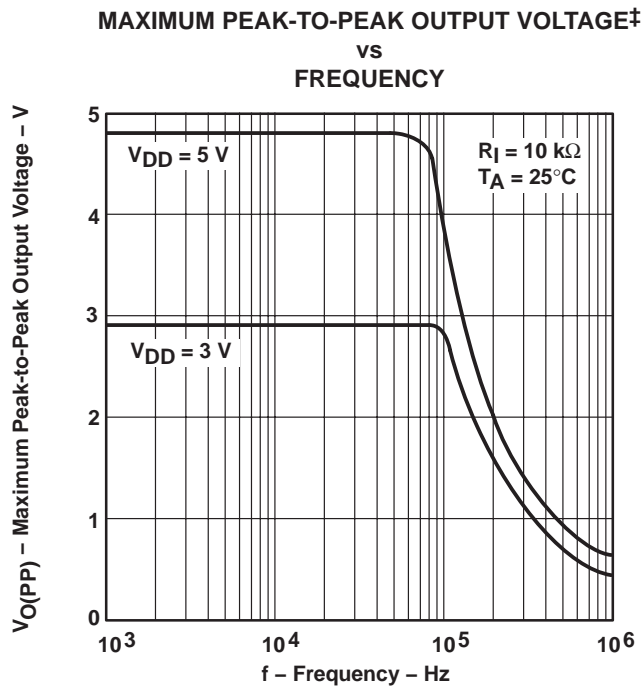


Figure 20

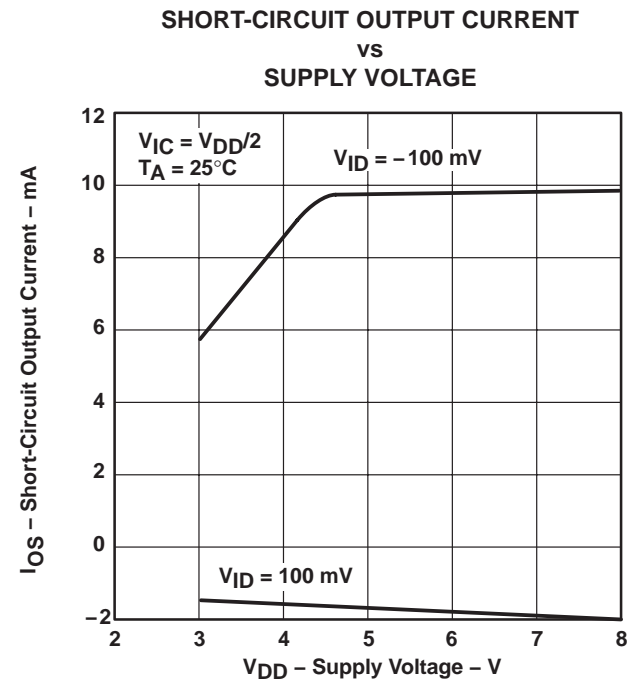


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where $V_{DD} = 5 V$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3 V$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT†
vs
FREE-AIR TEMPERATURE



Figure 22

DIFFERENTIAL INPUT VOLTAGE‡
vs
OUTPUT VOLTAGE

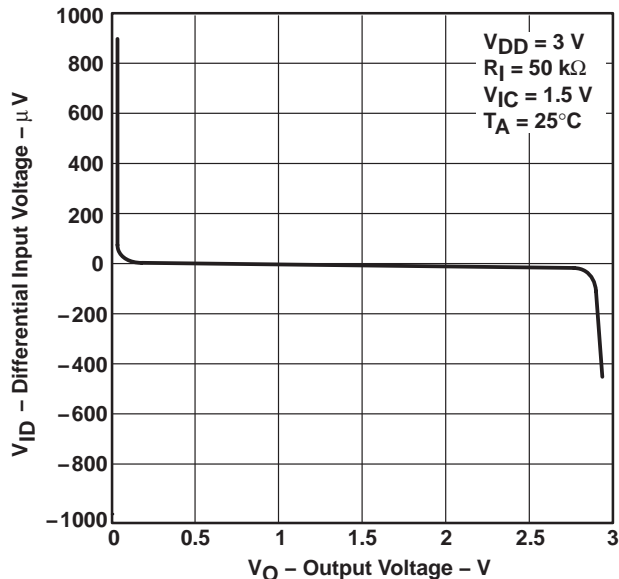


Figure 23

DIFFERENTIAL INPUT VOLTAGE‡
vs
OUTPUT VOLTAGE

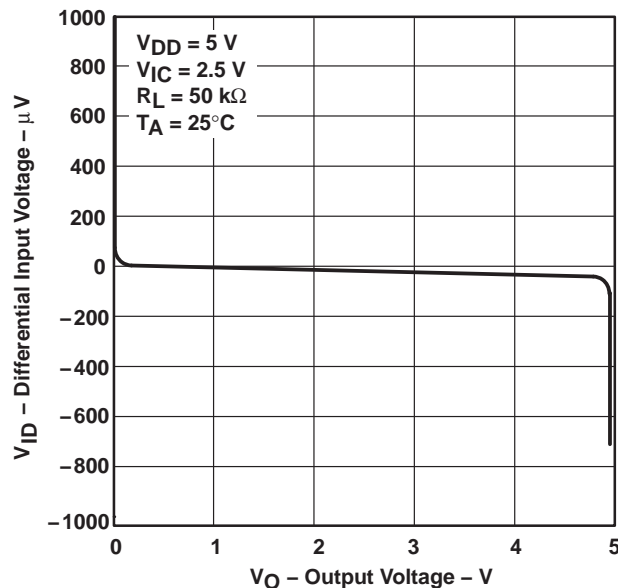


Figure 24

DIFFERENTIAL VOLTAGE AMPLIFICATION‡
vs
LOAD RESISTANCE



Figure 25

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
 AMPLIFICATION AND PHASE MARGIN†
 vs
 FREQUENCY

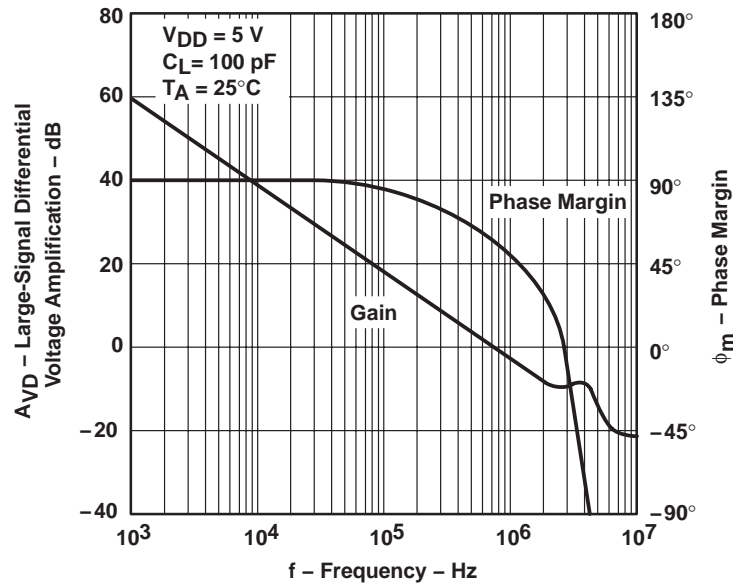


Figure 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
 AMPLIFICATION AND PHASE MARGIN†
 vs
 FREQUENCY

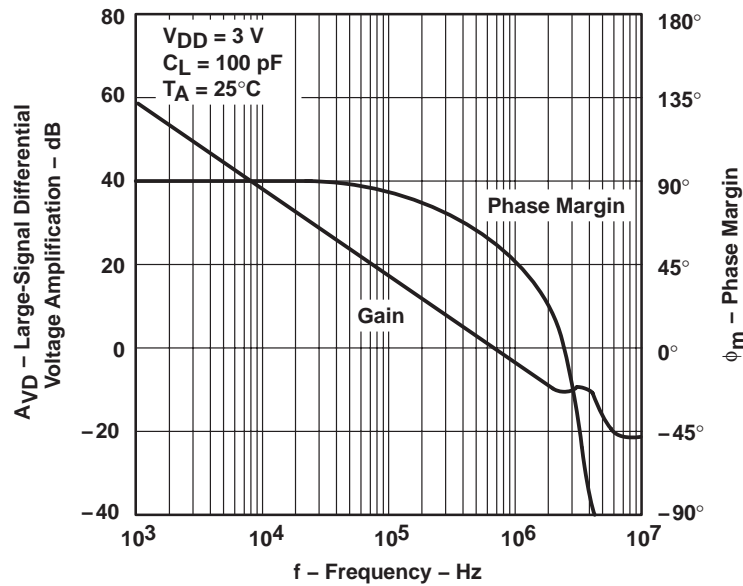


Figure 27

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†‡
vs
FREE-AIR TEMPERATURE

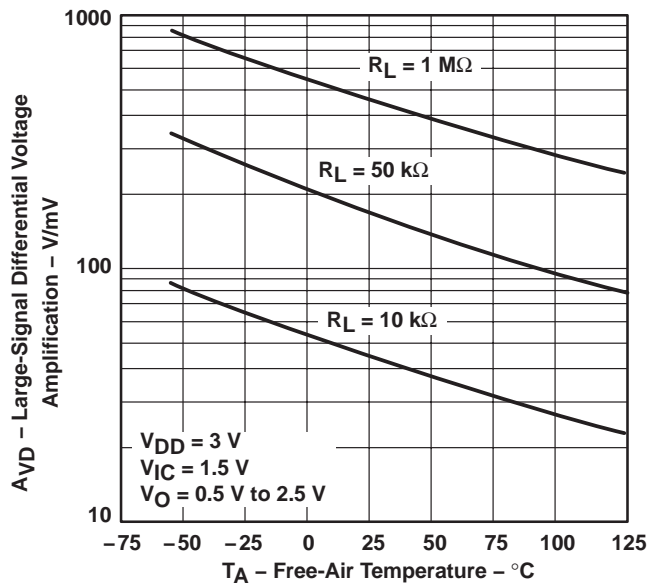


Figure 28

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†‡
vs
FREE-AIR TEMPERATURE

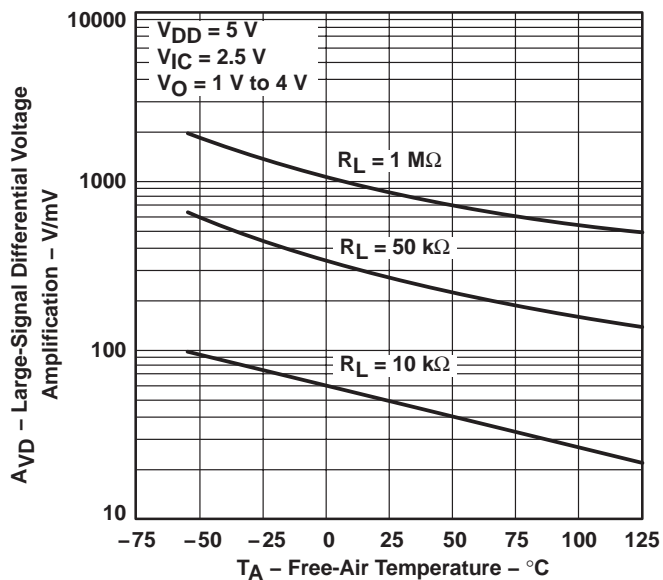


Figure 29

OUTPUT IMPEDANCE‡
vs
FREQUENCY



Figure 30

OUTPUT IMPEDANCE‡
vs
FREQUENCY

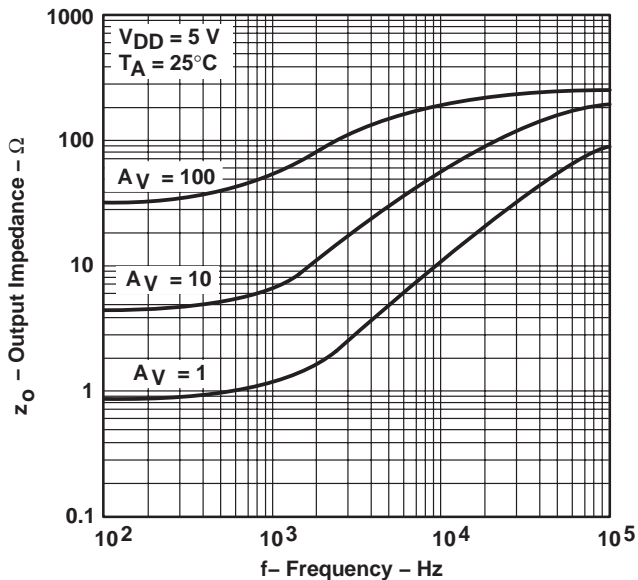


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

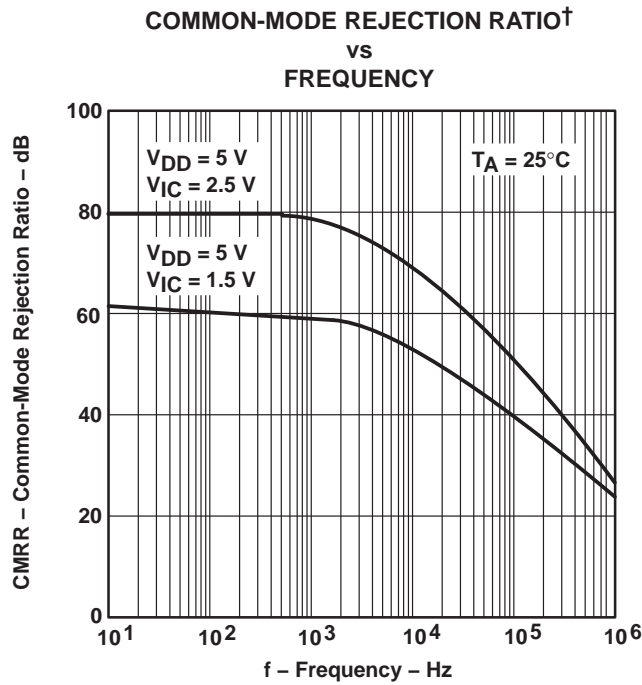


Figure 32

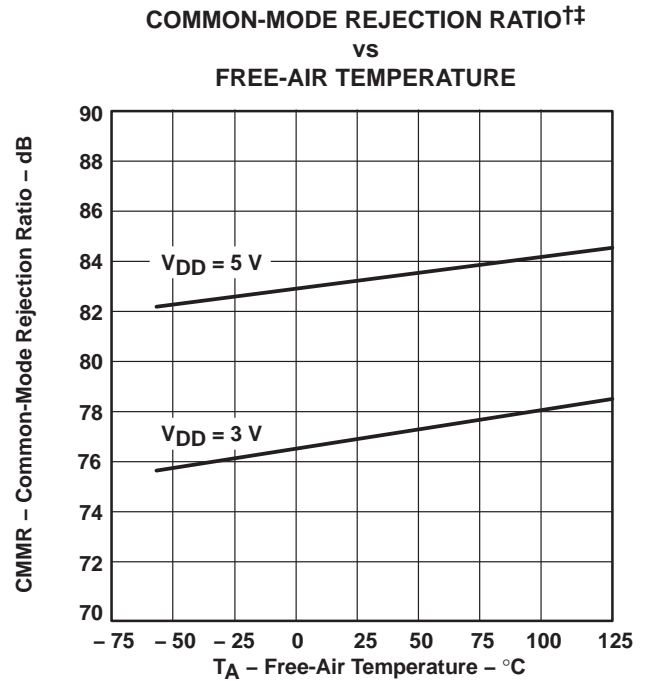


Figure 33

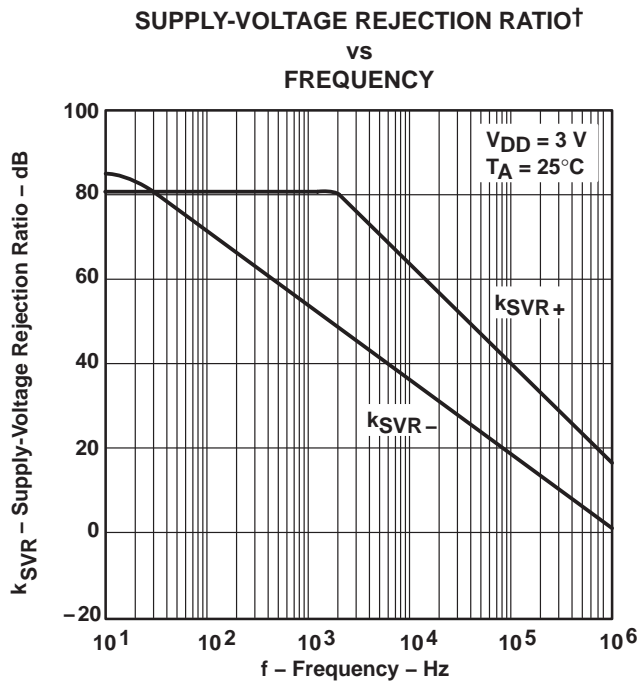


Figure 34

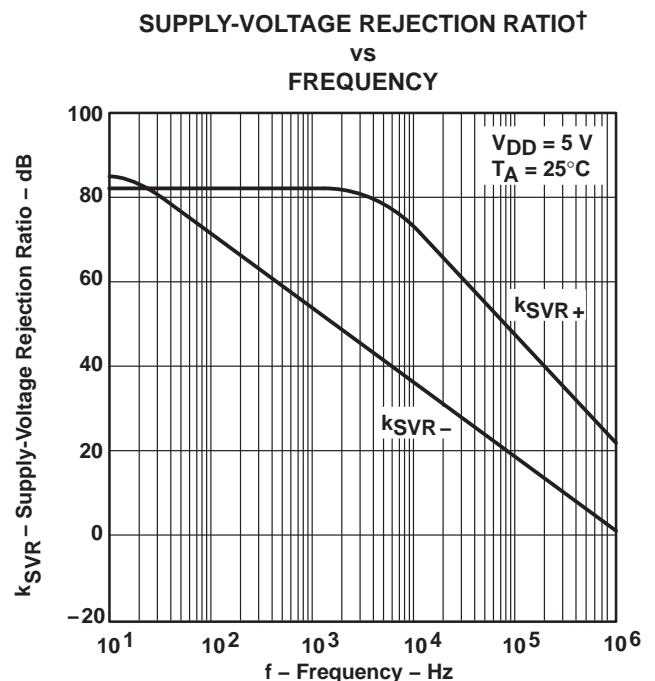


Figure 35

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.
 ‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



Figure 36

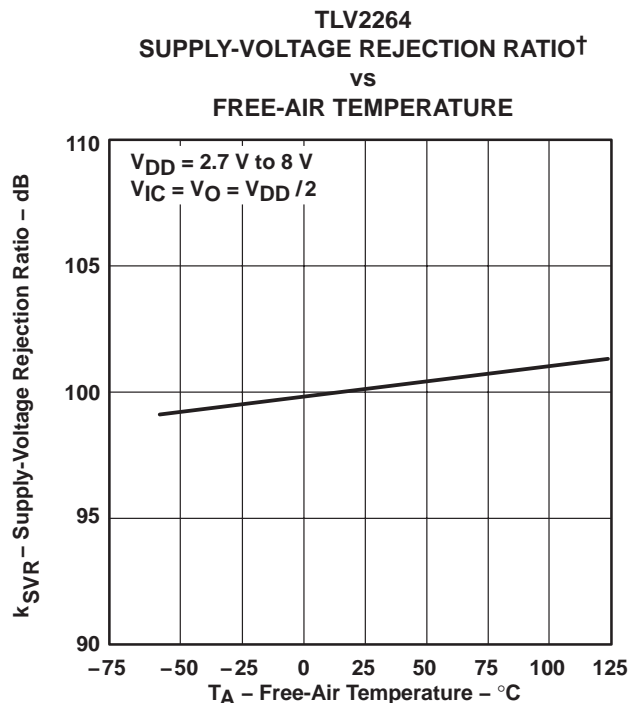


Figure 37

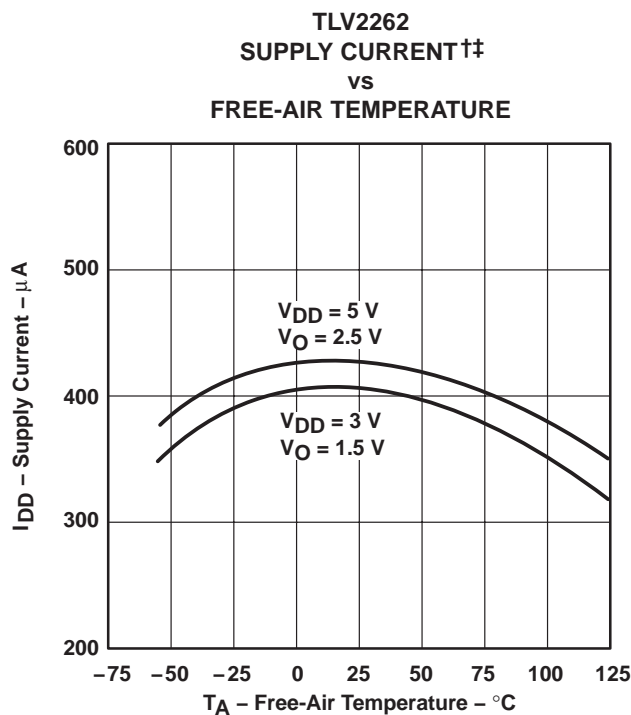


Figure 38

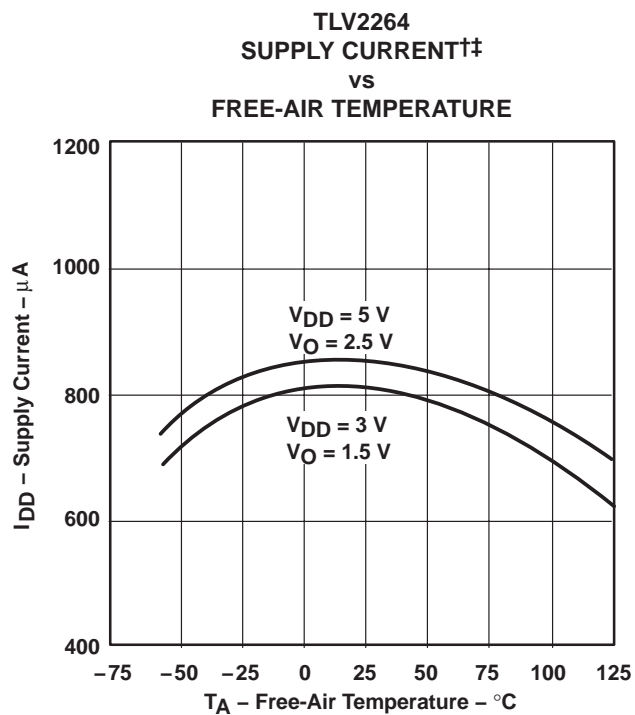
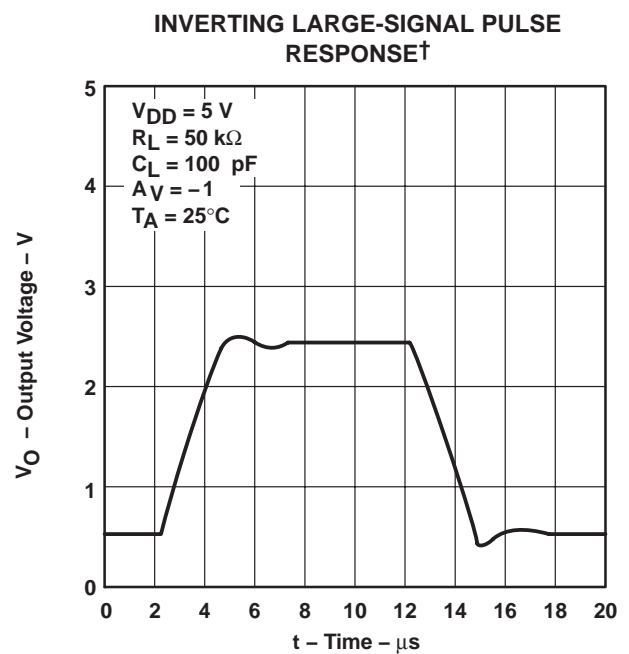
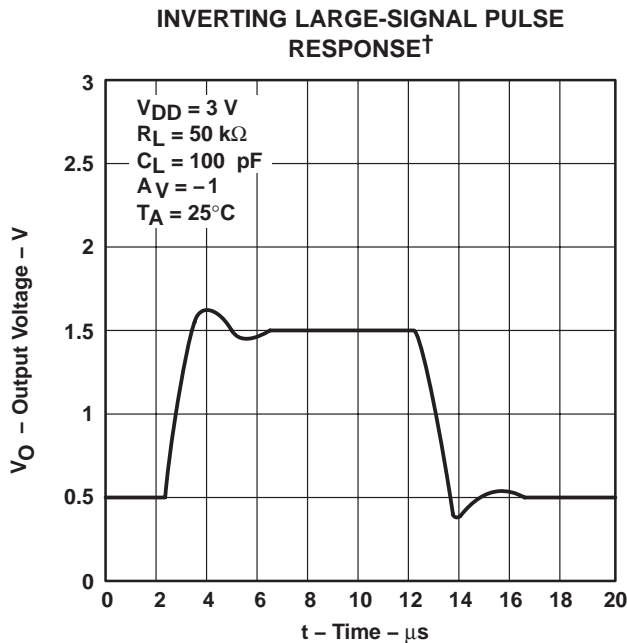
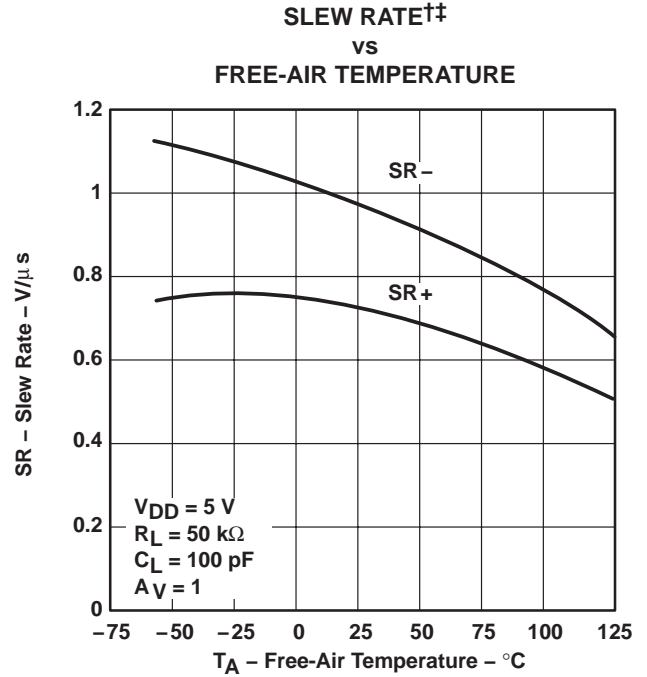


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3 \text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS



† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.
 ‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

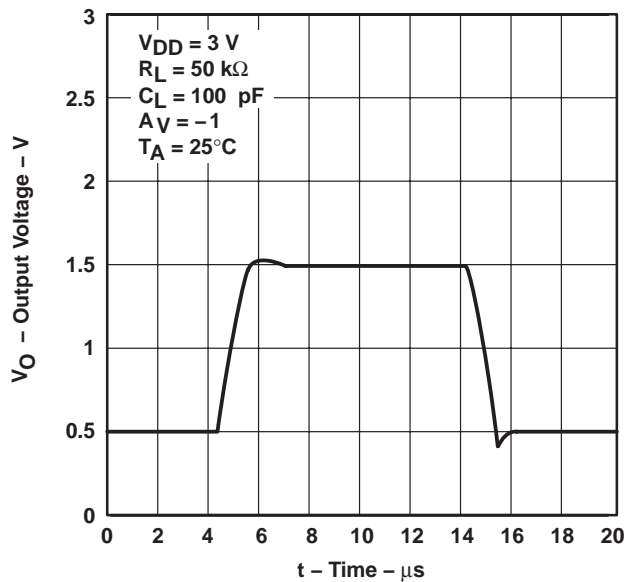


Figure 44

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

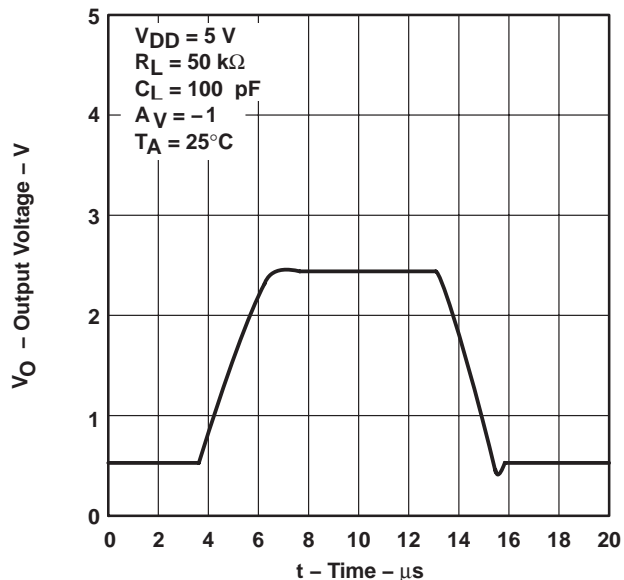


Figure 45

INVERTING SMALL-SIGNAL PULSE RESPONSE†

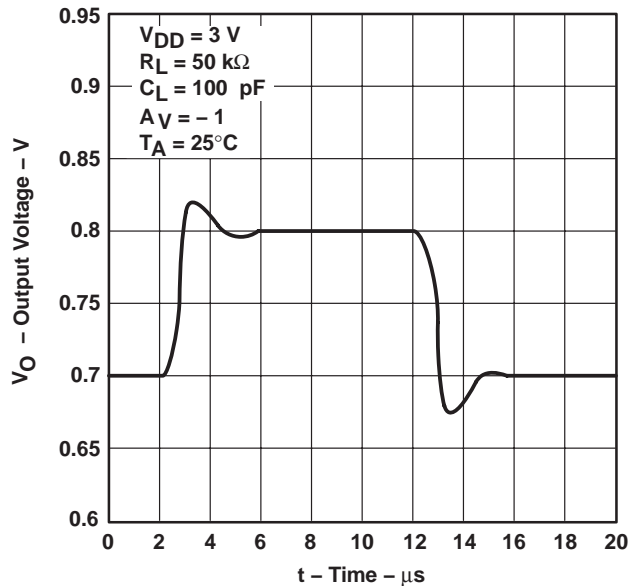


Figure 46

INVERTING SMALL-SIGNAL PULSE RESPONSE†

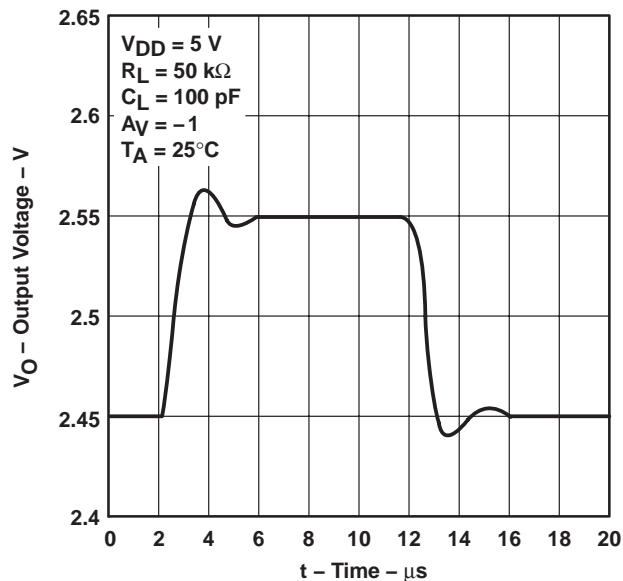


Figure 47

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

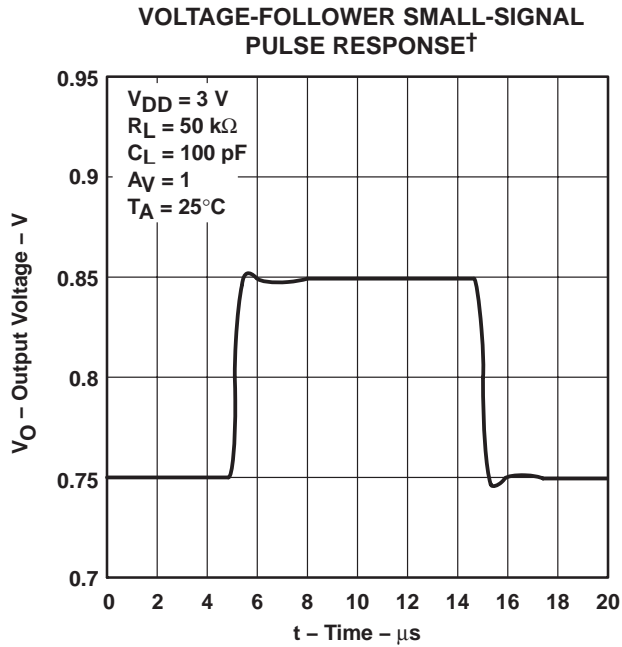


Figure 48



Figure 49

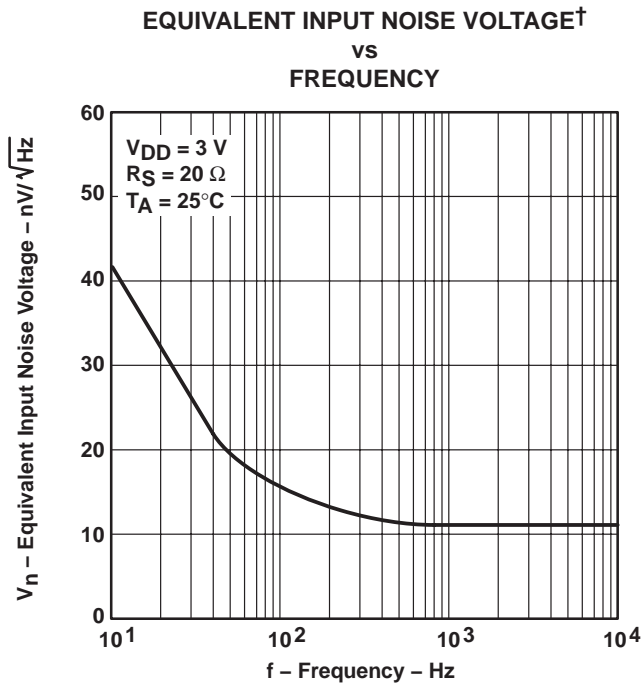


Figure 50

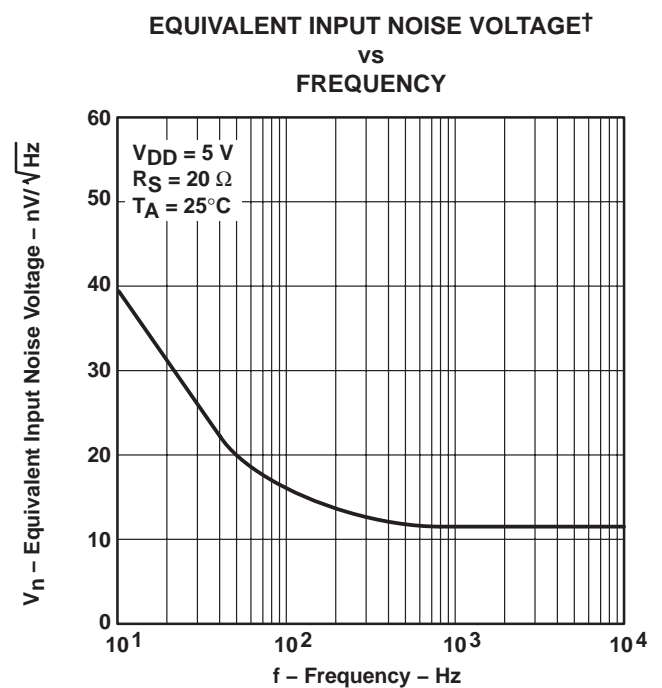


Figure 51

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

**INPUT NOISE VOLTAGE OVER
 A 10-SECOND PERIOD†**

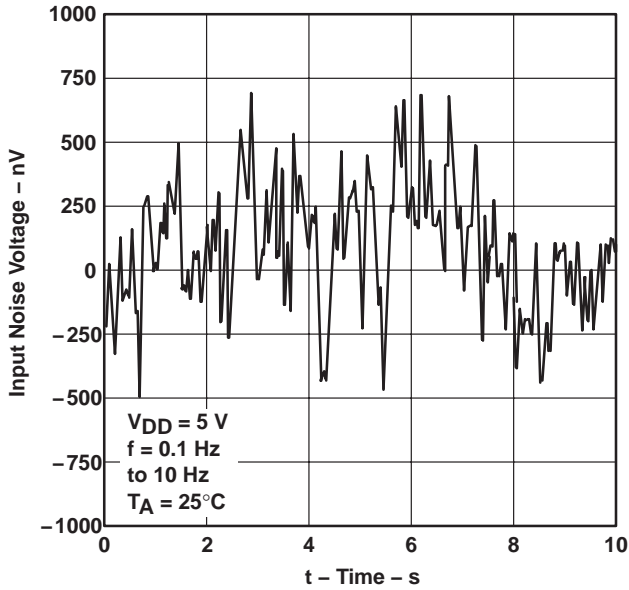


Figure 52

**INTEGRATED NOISE VOLTAGE
 VS
 FREQUENCY**

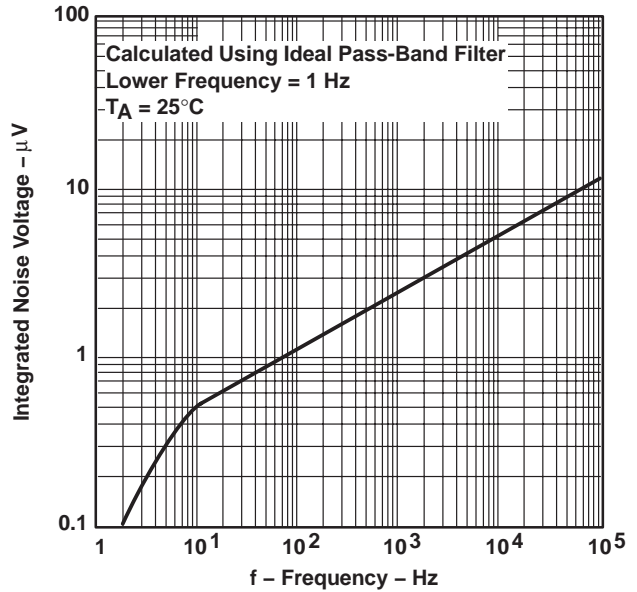


Figure 53

**TOTAL HARMONIC DISTORTION PLUS NOISE†
 VS
 FREQUENCY**

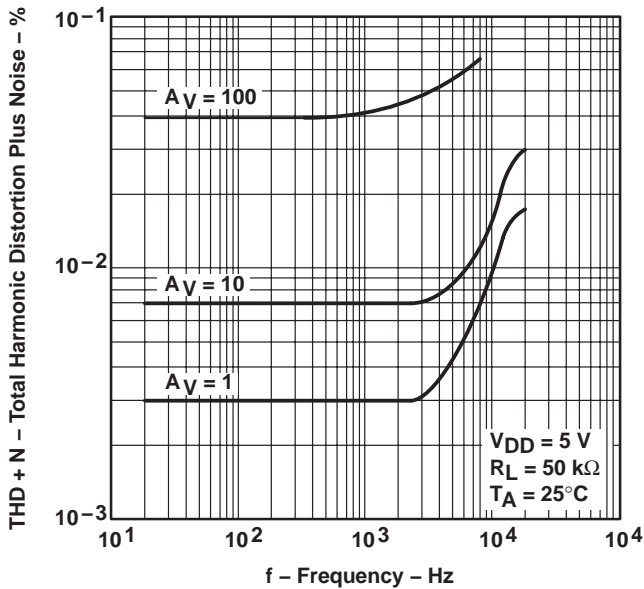


Figure 54

**GAIN-BANDWIDTH PRODUCT
 VS
 SUPPLY VOLTAGE**

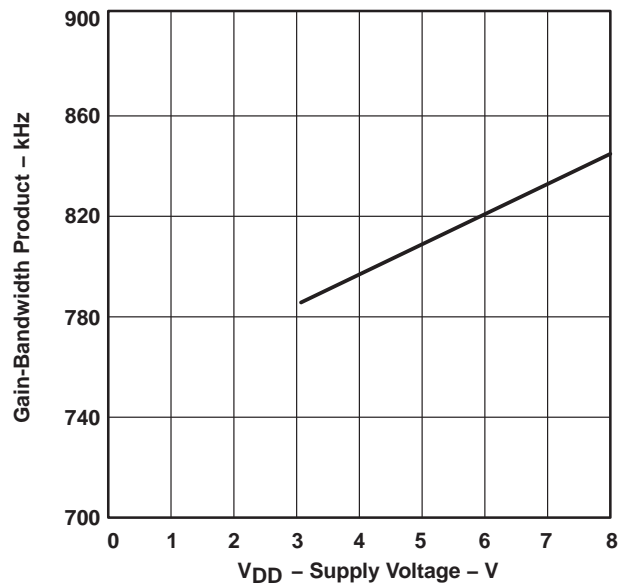


Figure 55

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

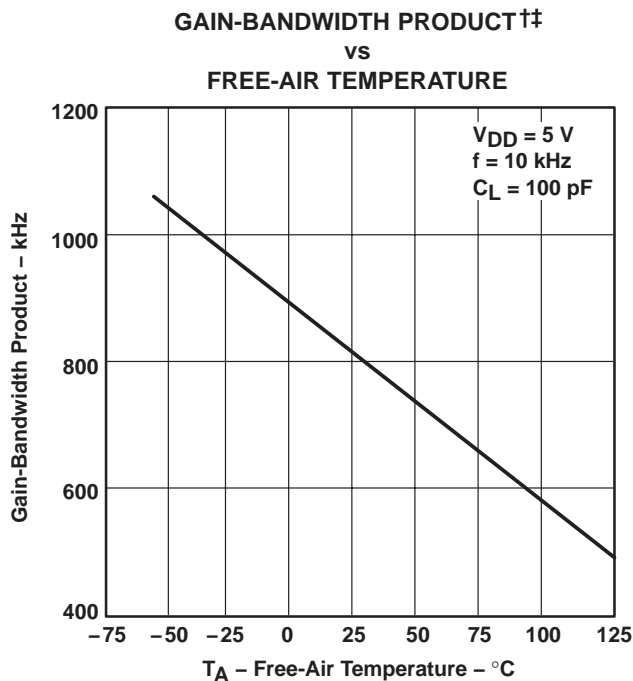


Figure 56

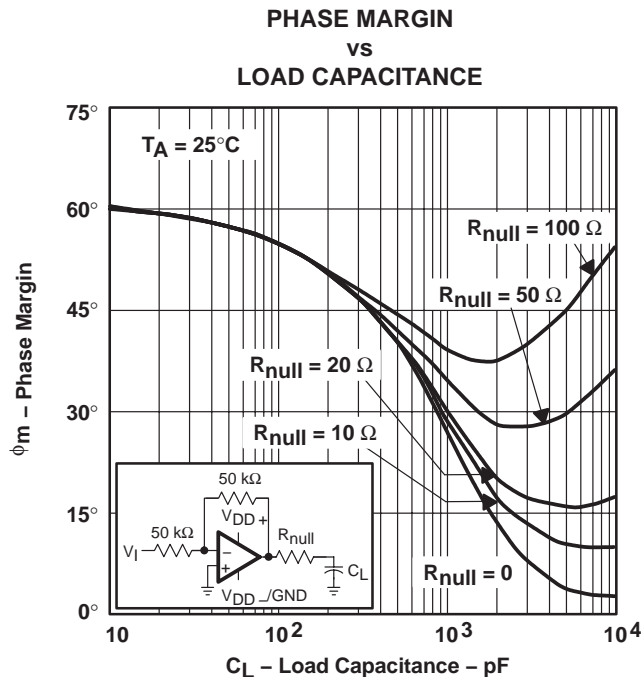


Figure 57

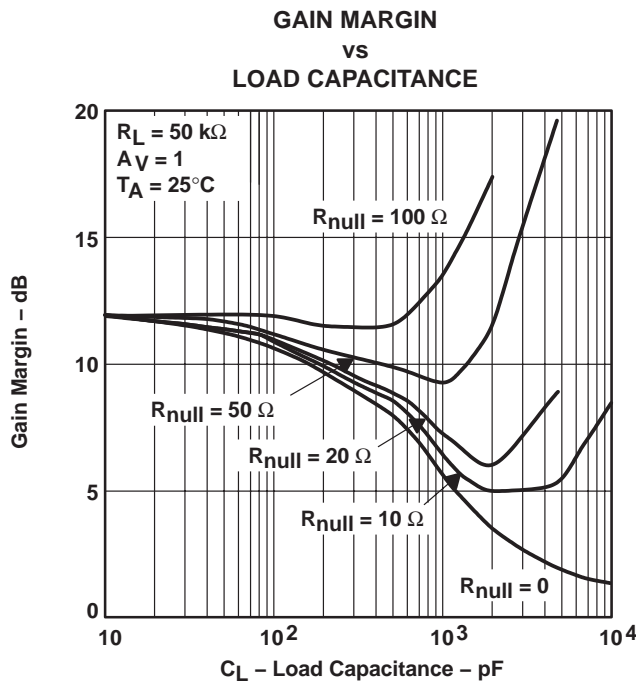


Figure 58

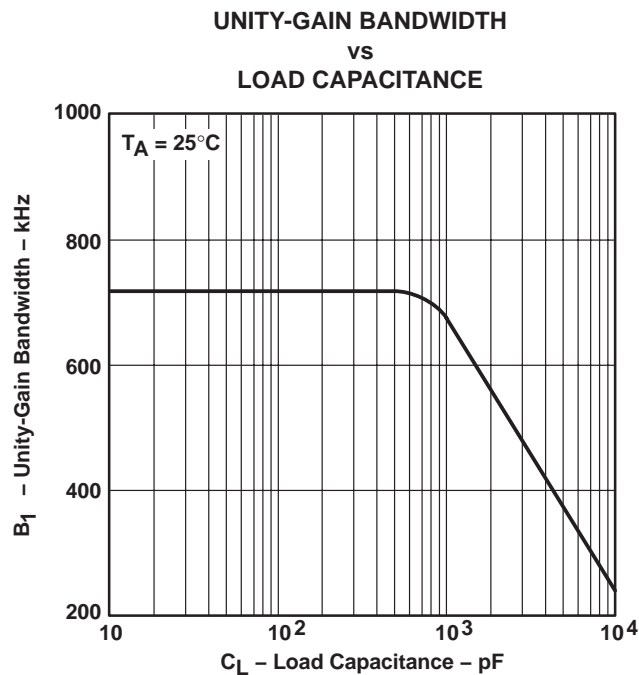
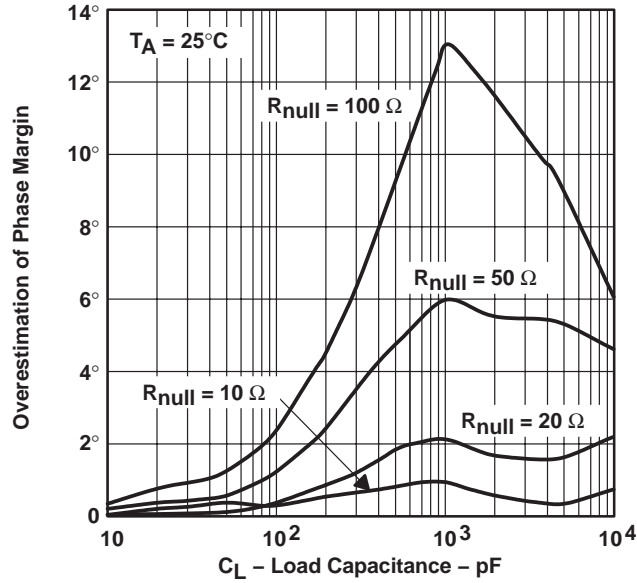


Figure 59

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.
†† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

OVERESTIMATION OF PHASE MARGIN†
vs
LOAD CAPACITANCE



† See application information

Figure 60

APPLICATION INFORMATION

driving large capacitive loads

The TLV226x is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 51 and Figure 52 illustrate its ability to drive loads greater than 400 pF while maintaining good gain and phase margins ($R_{null} = 0$).

A smaller series resistor (R_{null}) at the output of the device (see Figure 61) improves the gain and phase margins when driving large capacitive loads. Figure 51 and Figure 52 show the effects of adding series resistances of 10 Ω , 20 Ω , 50 Ω , and 100 Ω . The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation (1) can be used.

$$\Delta\theta_{m1} = \tan^{-1} \left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L \right) \quad (1)$$

Where :

$\Delta\theta_{m1}$ = improvement in phase margin

UGBW = unity-gain bandwidth frequency

R_{null} = output series resistance

C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 53). To use equation 1, UGBW must be approximated from Figure 53.

Using equation 1 alone overestimates the improvement in phase margin as illustrated in Figure 59. The overestimation is caused by the decrease in the frequency of the pole associated with the load, providing additional phase shift and reducing the overall improvement in phase margin. The pole associated with the load is reduced by the factor calculated in equation 2.

$$F = \frac{1}{1 + g_m \times R_{null}} \quad (2)$$

Where :

F = factor reducing frequency of pole

g_m = small-signal output transconductance (typically 4.83×10^{-3} mhos)

R_{null} = output series resistance

For the TLV226x, the pole associated with the load is typically 7 MHz with 100-pF load capacitance. This value varies inversely with C_L : at $C_L = 10$ pF, use 70 MHz, at $C_L = 1000$ pF, use 700 kHz, and so on.

Reducing the pole associated with the load introduces phase shift, thereby reducing phase margin. This results in an error in the increase in phase margin expected by considering the zero alone (equation 1). Equation 3 approximates the reduction in phase margin due to the movement of the pole associated with the load. The result of this equation can be subtracted from the result of the equation 1 to better approximate the improvement in phase margin.

APPLICATION INFORMATION

driving large capacitive loads (continued)

$$\Delta\theta_{m2} = \tan^{-1} \left[\frac{UGBW}{(F \times P_2)} \right] - \tan^{-1} \left(\frac{UGBW}{P_2} \right) \tag{3}$$

Where :

$\Delta\theta_{m2}$ = reduction in phase margin

UGBW = unity-gain bandwidth frequency

F = factor from equation (2)

P_2 = unadjusted pole (70 MHz @ 10 pF, 7 MHz @ 100 pF, etc.)

Using these equations with Figure 60 and Figure 61 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitive loads.

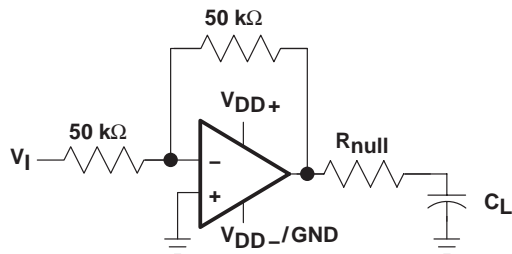


Figure 61. Series-Resistance Circuit

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSPice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 62 are generated using the TLV226x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Intergrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

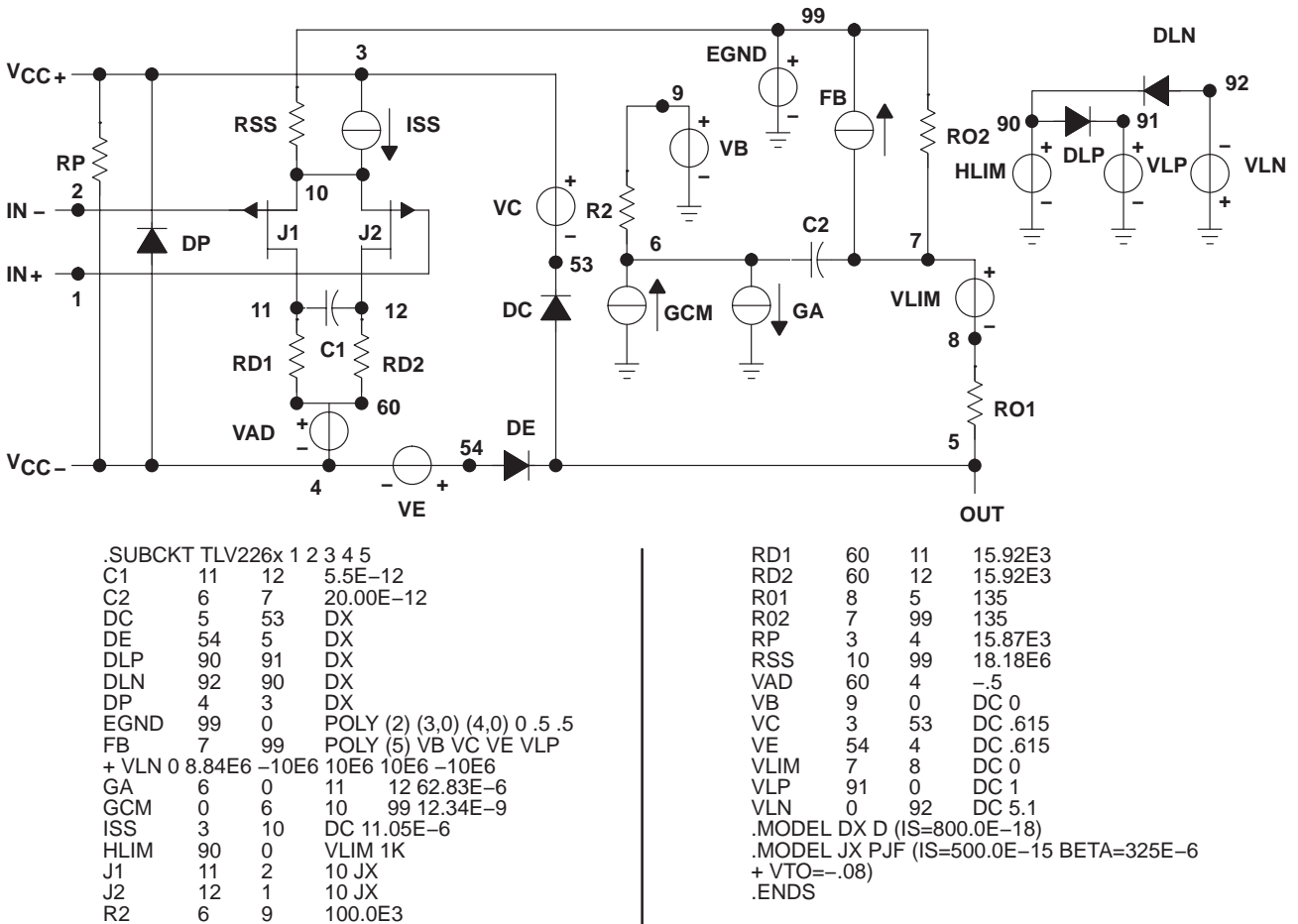


Figure 62. Boyle Macromodel and Subcircuit

PSPice and *Parts* are trademarks of MicroSim Corporation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|------------------------------------|-------------------------|
| 5962-9550401QPA | ACTIVE | CDIP | JG | 8 | 50 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 9550401QPA TLV2262M | Samples |
| 5962-9550403QHA | ACTIVE | CFP | U | 10 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 9550403QHA TLV2262AM | Samples |
| 5962-9550403QPA | ACTIVE | CDIP | JG | 8 | 50 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 9550403QPA TLV2262AM | Samples |
| 5962-9550404QCA | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9550404QC A TLV2264AMJB | Samples |
| 5962-9550404QDA | ACTIVE | CFP | W | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9550404QD A TLV2264AMWB | Samples |
| TLV2262AID | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | V2262A | Samples |
| TLV2262AIDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | V2262A | Samples |
| TLV2262AIP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2262AI | Samples |
| TLV2262AIPWR | ACTIVE | TSSOP | PW | 8 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TY262A | Samples |
| TLV2262AMJGB | ACTIVE | CDIP | JG | 8 | 50 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 9550403QPA TLV2262AM | Samples |
| TLV2262AMUB | ACTIVE | CFP | U | 10 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 9550403QHA TLV2262AM | Samples |
| TLV2262ID | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | V2262I | Samples |
| TLV2262IDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | V2262I | Samples |
| TLV2262IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| TLV2262IP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2262IP | Samples |
| TLV2262IPWR | ACTIVE | TSSOP | PW | 8 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TY2262 | Samples |
| TLV2262MJGB | ACTIVE | CDIP | JG | 8 | 50 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 9550401QPA TLV2262M | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|------------------------------------|-------------------------|
| TLV2264AID | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | V2264AI | Samples |
| TLV2264AIDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | V2264AI | Samples |
| TLV2264AIDRG4 | ACTIVE | SOIC | D | 14 | 2500 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| TLV2264AIN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2264AIN | Samples |
| TLV2264AIPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | P2264AI | Samples |
| TLV2264AMJB | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9550404QC A TLV2264AMJB | Samples |
| TLV2264AMWB | ACTIVE | CFP | W | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9550404QD A TLV2264AMWB | Samples |
| TLV2264AQD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV2264A | Samples |
| TLV2264ID | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV2264I | Samples |
| TLV2264IDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV2264I | Samples |
| TLV2264IN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2264IN | Samples |
| TLV2264IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | P2264I | Samples |
| TLV2264QD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV2264 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLV2262, TLV2262A, TLV2262AM, TLV2262M, TLV2264A, TLV2264AM :

● Catalog : [TLV2262A](#), [TLV2262](#), [TLV2264A](#)

● Automotive : [TLV2262A-Q1](#), [TLV2262A-Q1](#), [TLV2264A-Q1](#), [TLV2264A-Q1](#)

● Military : [TLV2262M](#), [TLV2262AM](#), [TLV2264AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV2262AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2262AIPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV2262IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2262IPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV2264AIDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV2264AIPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV2264IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV2264IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV2262AIDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV2262AIPWR | TSSOP | PW | 8 | 2000 | 356.0 | 356.0 | 35.0 |
| TLV2262IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV2262IPWR | TSSOP | PW | 8 | 2000 | 356.0 | 356.0 | 35.0 |
| TLV2264AIDR | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| TLV2264AIPWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| TLV2264IDR | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| TLV2264IPWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9550403QHA | U | CFP | 10 | 25 | 506.98 | 26.16 | 6220 | NA |
| 5962-9550404QDA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| TLV2262AID | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TLV2262AIP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TLV2262AMUB | U | CFP | 10 | 25 | 506.98 | 26.16 | 6220 | NA |
| TLV2262ID | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TLV2262IP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TLV2264AID | D | SOIC | 14 | 50 | 507 | 8 | 3940 | 4.32 |
| TLV2264AIN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| TLV2264AMWB | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| TLV2264AQD | D | SOIC | 14 | 50 | 505.46 | 6.76 | 3810 | 4 |
| TLV2264AQD | D | SOIC | 14 | 50 | 507 | 8 | 3940 | 4.32 |
| TLV2264ID | D | SOIC | 14 | 50 | 507 | 8 | 3940 | 4.32 |
| TLV2264IN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| TLV2264QD | D | SOIC | 14 | 50 | 505.46 | 6.76 | 3810 | 4 |

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

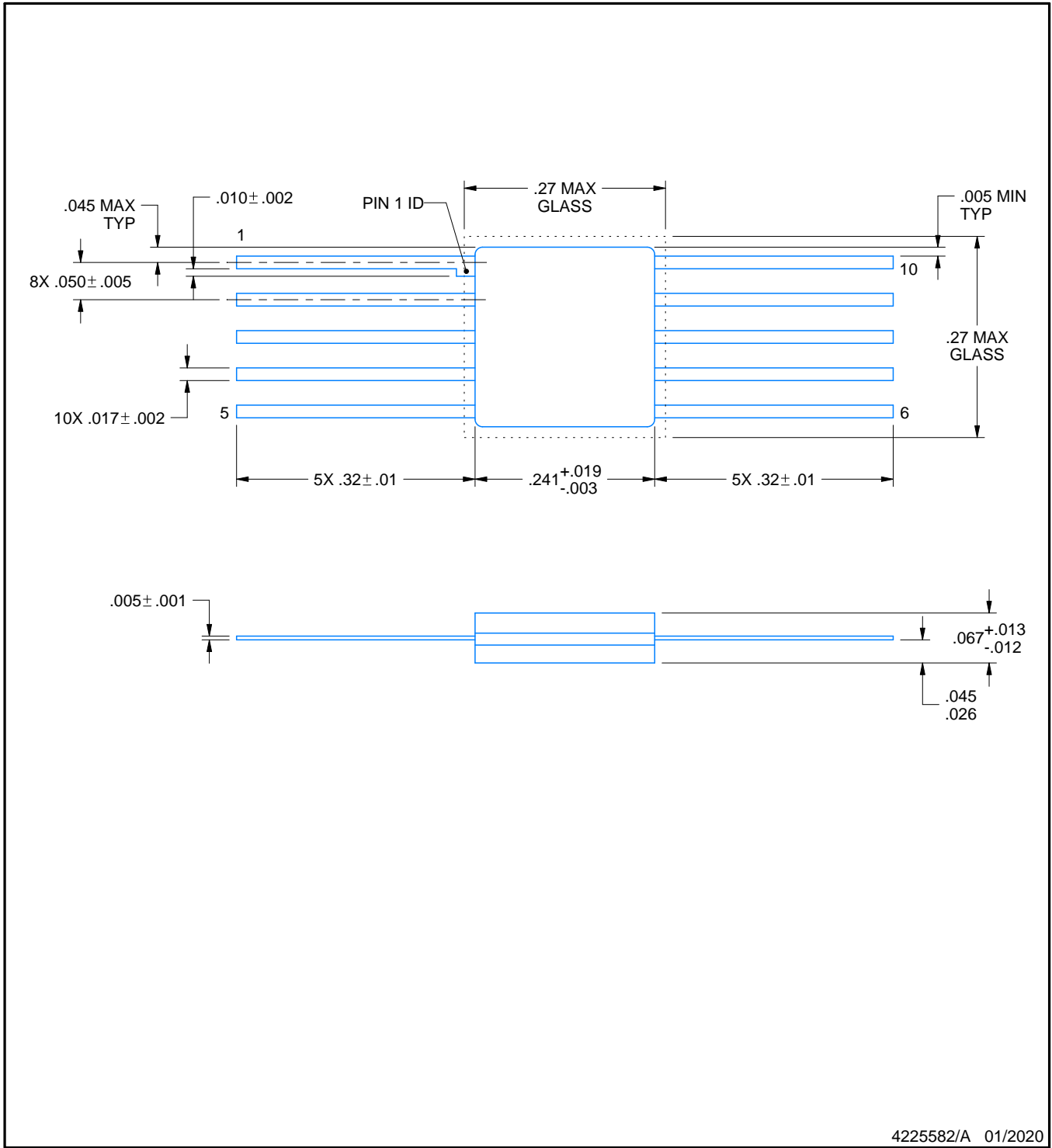
U0010A



PACKAGE OUTLINE

CFP - 2.03 mm max height

CERAMIC FLATPACK



4225582/A 01/2020

NOTES:

1. All linear dimensions are in inches. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE





D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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