

P54/74FCT138/A/C (P54/74PCT138/A/C) HIGH SPEED 1-OF-8 DECODER



FEATURES

- Function, Pinout, and Drive Compatible with the FCT and F Logic
- FCT-C speed at 4.7ns max. (Com'I)
FCT-A speed at 5.8ns max. (Com'I)
- CMOS V_{OH} Levels for Low Power Consumption
— Typically 1/3 of FAST Bipolar Logic
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Inputs and Outputs Interface Directly with TTL, NMOS, and CMOS Devices
- Outputs Meet Levels Required for CMOS Static RAM Low Power Standby Mode
- 64 mA Sink Current (Com'I), 48 mA (MII)
15 mA Source Current (Com'I), 12 mA (MII)
- Dual 1-of-8 Decoder with Enables
- Manufactured In 0.8 micron PACE Technology™



DESCRIPTION

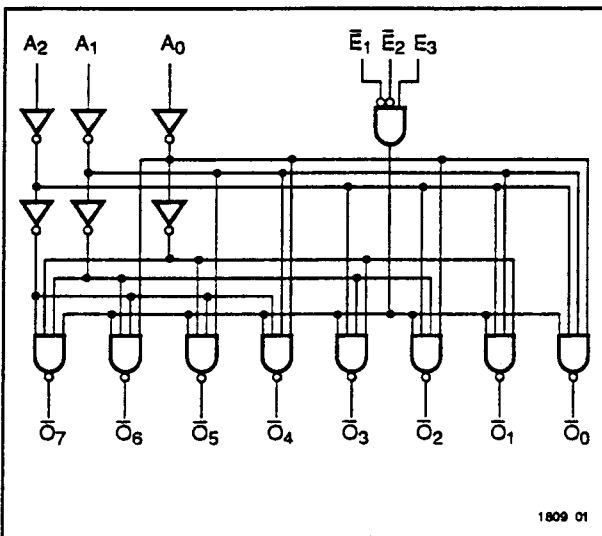
The 'FCT138 are 1-of-8 decoders. The 'FCT138 accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provide eight mutually exclusive active LOW outputs ($\bar{O}_0 - \bar{O}_7$). The 'FCT138 features three enable inputs, two active LOW (\bar{E}_1, \bar{E}_2) and one active HIGH (E_3). All outputs will be HIGH unless \bar{E}_1 and \bar{E}_2 are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 'FCT138 devices and one inverter.

The 'FCT138 is manufactured using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.8 micron effective channel lengths giving 500 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V.

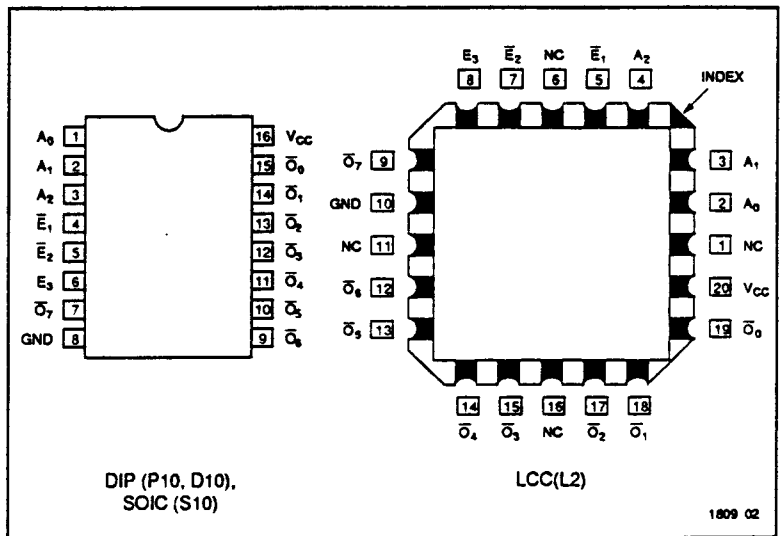


FUNCTIONAL BLOCK DIAGRAM



1809 01

PIN CONFIGURATIONS



DIP (P10, D10),
SOIC (S10)

LCC(L2)

1809 02

ABSOLUTE MAXIMUM RATINGS^{1,2}

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +150	°C
T_A	Ambient Temperature Under Bias	-65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	-0.5 to +7.0	V
I_{IN}	Input Current	-30 to +5.0	mA

Notes:

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1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_{OUT}	Voltage Applied to Output	-0.5 to $V_{CC} + 0.5$	V

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2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	-55°C	+125°C
Commercial	0°C	+70°C

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Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter	Min	Typ ¹	Max	Units	V_{CC}	Conditions	
V_{IH}	Input HIGH Voltage	2.0		$V_{CC} + 0.5$	V			
V_{IL}	Input LOW Voltage	-0.5		0.8	V			
V_H	Hysteresis		0.35		V		All inputs	
V_{CD}	Input Clamp Diode Voltage		-0.7	-1.2	V	MIN	$I_{IN} = -18mA$	
V_{OH}	Output HIGH Voltage	$V_{CC} = 3V, V_{IN} = 0.2V, \text{ or } V_{CC} - 0.2V$		$V_{CC} - 0.2$	V_{CC}	V	$I_{OH} = -32\mu A$	
		Military/Commercial (CMOS)	$V_{CC} - 0.2$	V_{CC}	V	MIN	$I_{OH} = -300\mu A$	
		Military (TTL)	2.4	4.3	V	MIN	$I_{OH} = -12mA$	
		Commercial (TTL)	2.4	4.3	V	MIN	$I_{OH} = -15mA$	
V_{OL}	Output LOW Voltage	$V_{CC} = 3V, V_{IN} = 0.2V, \text{ or } V_{CC} - 0.2V$			GND	V	$I_{OL} = 300\mu A$	
		Military/Commercial (CMOS) ³		GND	0.2	V	MIN	$I_{OL} = 300\mu A$
		Military (TTL)		0.3	0.5	V	MIN	$I_{OL} = 32mA$
		Commercial (TTL)		0.3	0.5	V	MIN	$I_{OL} = 48mA$
		Commercial (TTL)		0.3	0.5	V	MIN	$I_{OL} = 64mA$
I_{IH}	Input HIGH Current			5	μA	MAX	$V_{IN} = V_{CC}$	
I_{IL}	Input LOW Current			-5	μA	MAX	$V_{IN} = GND$	
I_{IH}	Input HIGH Current ³			5	μA	MAX	$V_{OUT} = 2.7V$	
I_{IL}	Input LOW Current ³			-5	μA	MAX	$V_{OUT} = 0.5V$	
I_{OS}	Output Short Circuit Current ²	-60	-120		mA	MAX	$V_{OUT} = 0.0V$	
C_{IN}	Input Capacitance ³		5	10	pF		All inputs	
C_{OUT}	Output Capacitance ³		9	12	pF		All outputs	

Notes:

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- Typical limits are at $V_{CC} = 5.0V, T_A = +25^\circ C$ ambient.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect

operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

- This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ ¹	Max	Units	Conditions
I_{CC}	Quiescent Power Supply Current (CMOS inputs)	0.003	0.5	mA	$V_{CC} = \text{MAX}$, $f_1 = 0$, Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 3.4V^2$, $f_1 = 0$, Outputs Open
I_{CCD}	Dynamic Power Supply Current ³	0.15	0.3	mA/ mHz	$V_{CC} = \text{MAX}$, One Input Toggling, 50% Duty Cycle, Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current ⁵	1.7	4.5	mA	$V_{CC} = \text{MAX}$, $f_1 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, One Input Toggling, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.0	5.5	mA	$V_{CC} = \text{MAX}$, $f_1 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, One Input Toggling, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$

Notes:

- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient and maximum loading.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_o/2 + f_1 N_1)$
 $\Delta I_{CC} = \text{Quiescent Current with CMOS input levels}$

$\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
($V_{IN} = 3.4V$)

$D_H = \text{Duty Cycle for TTL Inputs High}$

$N_T = \text{Number of TTL Inputs at } D_H$

$I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$

$f_o = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$

$f_1 = \text{Output Frequency}$

$N_1 = \text{Number of Inputs at } f_1$

All currents are in milliamps and all frequencies are in megahertz.

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TRUTH TABLE

Inputs						Outputs							
\bar{E}_1	\bar{E}_2	E_3	A_0	A_1	A_2	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3	\bar{O}_4	\bar{O}_5	\bar{O}_6	\bar{O}_7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level, L=LOW Voltage Level, X=Don't Care

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AC CHARACTERISTICS

Sym	Parameter	'FCT138				'FCT138A				'FCT138C				Units	Fig. No.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.		
t_{PLH} t_{PHL}	Prop Delay A_0 to \overline{O}_n	1.5	12.0	1.5	9.0	1.5	7.8	1.5	5.8	1.5	6.0	1.5	4.7	ns	1, 5
t_{PLH} t_{PHL}	Prop Delay \overline{E}_1 or \overline{E}_2 to \overline{O}_n	1.5	12.5	1.5	9.0	1.5	8.0	1.5	5.9	1.5	6.5	1.5	5.0	ns	1, 5
t_{PLH} t_{PHL}	Prop Delay E_3 to \overline{O}_n	1.5	12.5	1.5	9.0	1.5	8.0	1.5	5.9	1.5	6.5	1.5	5.0	ns	1, 5

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Notes:

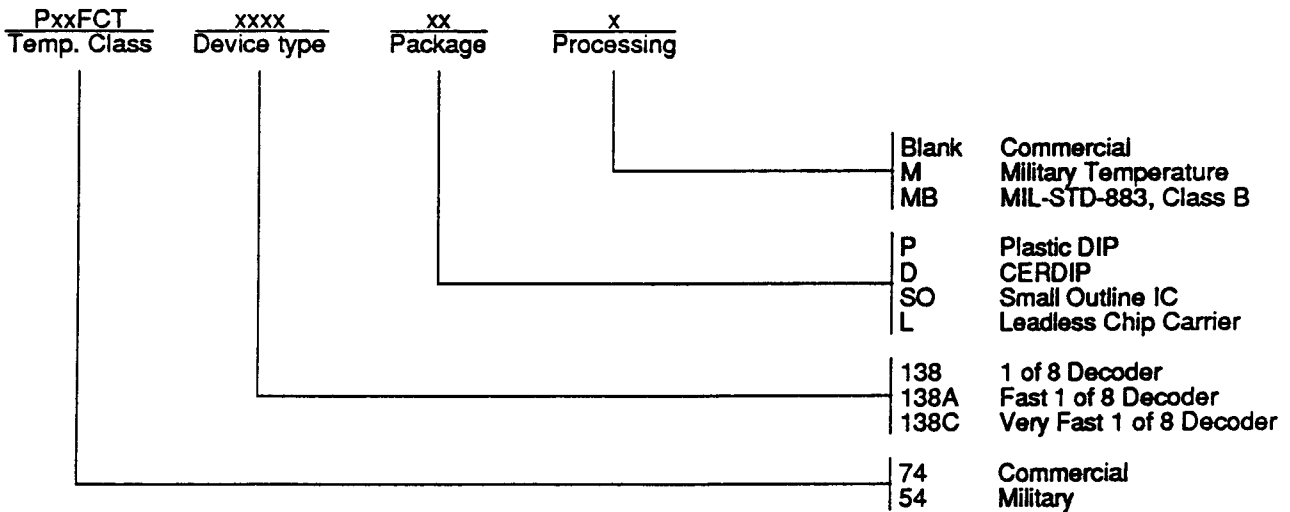
1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. With one data channel toggling, $t_w(L) = t_w(H) = 2.0ns$ and $t_r = t_f = 1.0ns$

DEFINITION OF FUNCTIONAL TERMS

PIN Names	Description
$A_0 - A_2$	Address Inputs
$\overline{E}_1 - \overline{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
$\overline{O}_0 - \overline{O}_7$	Outputs (Active LOW)

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ORDERING INFORMATION



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