CD74FCT16652T, CD74FCT162652T

December 1996

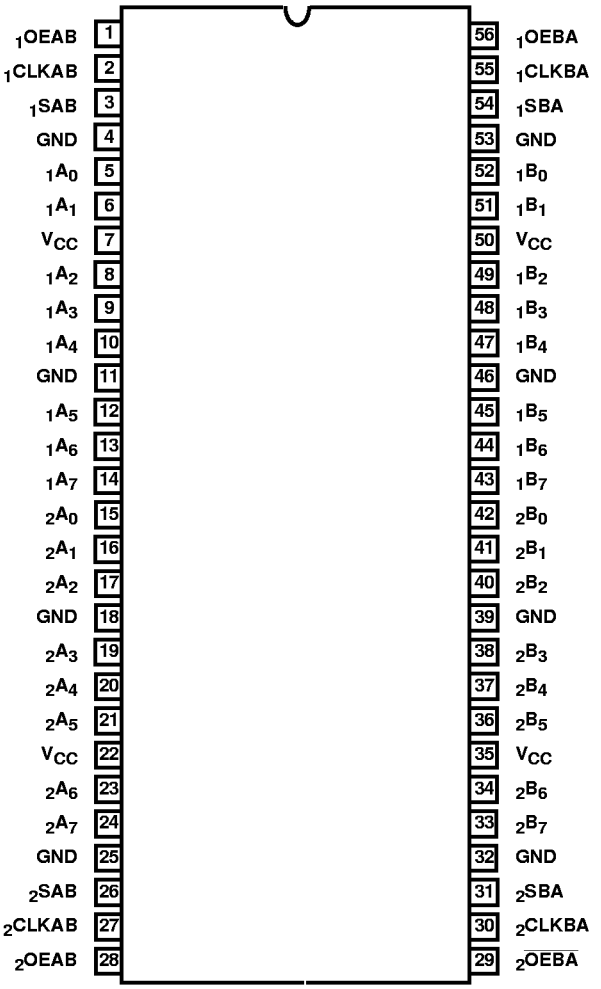
Fast CMOS 16-Bit Registered Transceivers

Features

- **These Devices are High-speed, Low Power Devices with High Current Drive**
- **V_{CC} = 5V ±10%**
- **Hysteresis on All Inputs**
- **CD74FCT16652T**
  - **High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA**
  - **Power Off Disable Outputs Permit "Live Insertion"**
  - **Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162652T**
  - **Balanced Output Drivers: ±24mA**
  - **Reduced System Switching Noise**
  - **Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C**

Pinout

CD74FCT16652T, CD74FCT162652T
(SSOP, TSSOP)
TOP VIEW



Description

Harris' CD74FCT16652T and CD74FCT162652T are produced in an advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

These devices are 16-bit registered transceivers organized as two independent 8-bit bus transceivers designed with three-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Each 8-bit transceiver utilizes the enable controls ($_X$OEAB and $_X\overline{OEBA}$) to control the transceiver functions. The Select ($_X$SAB and $_X$SBA) control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The CD74FCT16652T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT162652T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Ordering Information

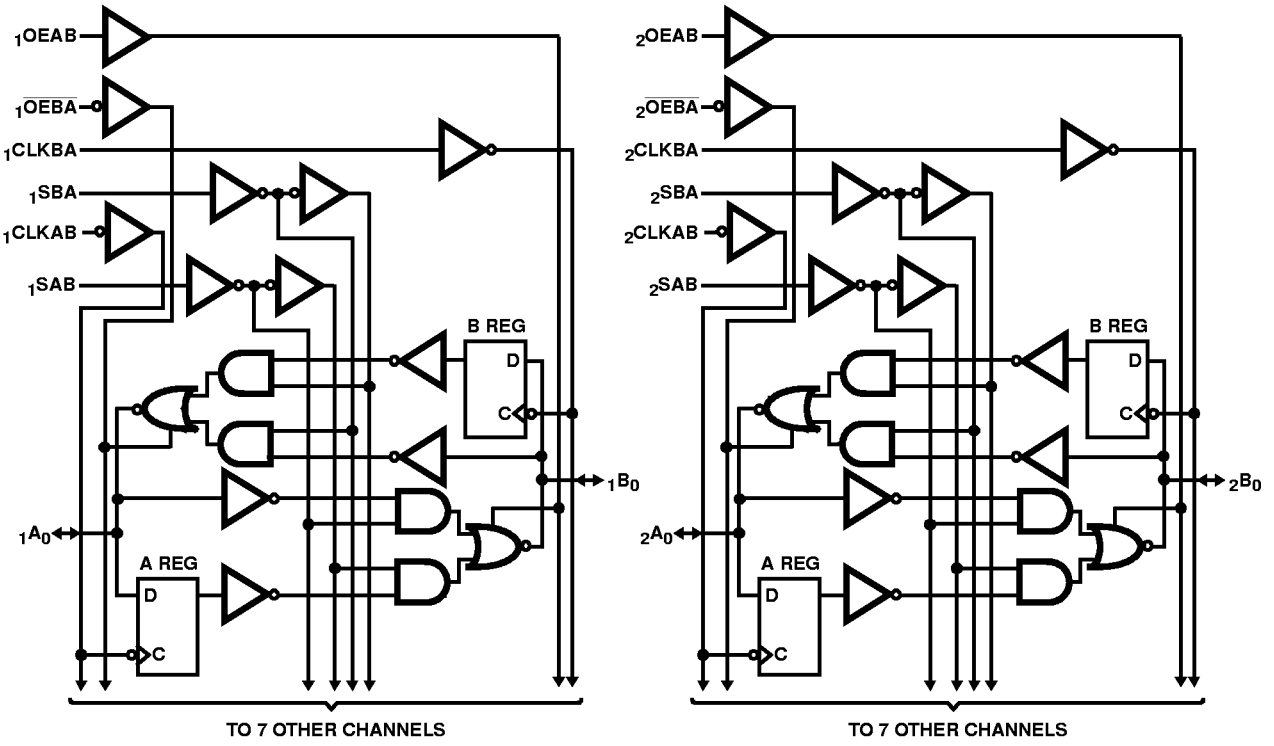
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16652ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16652ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16652CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16652CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16652DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16652ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16652TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16652TSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162652ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162652ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162652CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162652CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162652DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162652ETSM	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162652TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162652TSM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the varient in the tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4203.2**

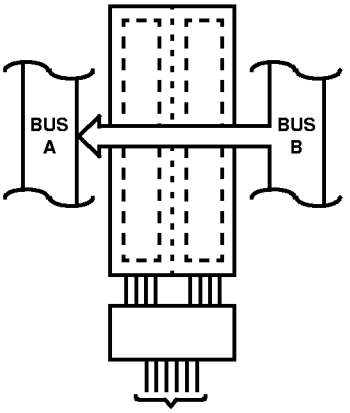
Functional Block Diagram



TRUTH TABLE

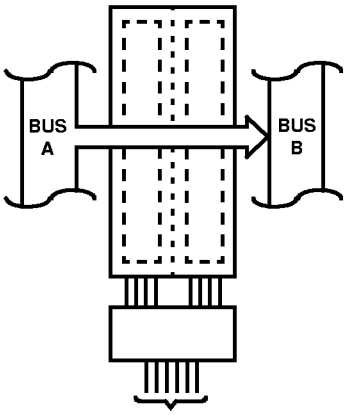
FUNCTION/OPERATION	INPUTS						DATA I/O	
	$_X$OEAB	$_X\overline{\text{OEBA}}$	$_X$CLKAB	$_X$CLKBA	$_X$SAB	$_X$SBA	$_XA_X$	$_XB_X$
Isolation	L	H	H or L	H or L	X	X	Input	Input
Store A and B Data	L	H	↑	↑	X	X		
Store A, Hold B	X	H	↑	H or L	X	X	Input	Unspecified (Note 1)
Store A in Both Registers	H	H	↑	↑	X (Note 2)	X	Input	Output
Hold A, Store B	L	X	H or L	↑	X	X	Unspecified (Note 1)	Input
Store B in Both Registers	L	L	↑	↑	X	X (Note 2)	Output	Input
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	H	H	X	X	L	X	Input	Output
Stored A Data to B Bus	H	H	H or L	X	H	X		
Stored A Data to B Bus and Stored B Data to A Bus	H	L	H or L	H or L	H	H	Output	Output

1. The data output functions may be enabled or disabled by various signals at the xOEAB or x$\overline{\text{OEBA}}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.
   H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   ↑= LOW-to-HIGH transition



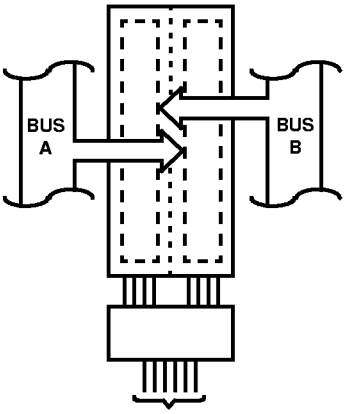
$_X$OEAB	$_X\overline{OEBA}$	$_X$CLKAB	$_X$CLKBA	$_X$SAB	$_X$SBA
L	L	X	X	X	L

FIGURE 1. REAL-TIME TRANSFER BUS B TO A



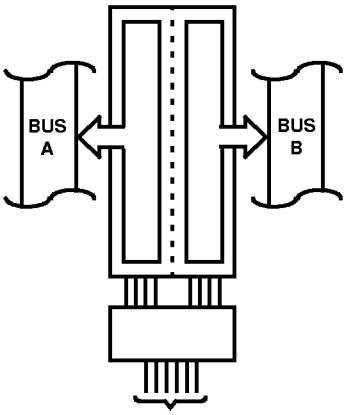
$_X$OEAB	$_X\overline{OEBA}$	$_X$CLKAB	$_X$CLKBA	$_X$SAB	$_X$SBA
H	H	X	X	L	X

FIGURE 2. REAL-TIME TRANSFER BUS A TO B



$_X$OEAB	$_X\overline{OEBA}$	$_X$CLKAB	$_X$CLKBA	$_X$SAB	$_X$SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

FIGURE 3. STORAGE FROM A AND/OR B



$_X$OEAB	$_X\overline{OEBA}$	$_X$CLKAB	$_X$CLKBA	$_X$SAB	$_X$SBA
H	L	H or L	H or L	H	H

FIGURE 4. TRANSFER STORES DATA TO A AND/OR B

Pin Descriptions

PIN NAME	DESCRIPTION
$_X$A$_X$	Data Register A Inputs Data Register B Outputs
$_X$B$_X$	Data Register B Inputs Data Register A Outputs
$_X$CLKAB, $_X$CLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
$_X$OEAB, $_X\overline{OEBA}$	Output Enable Inputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40^oC to 85^oC
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} ($^oC/W$)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETERS	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, $T_A = -40^oC$ to 85^oC, $V_{CC} = 5.0V \pm 10\%$							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = Vcc	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 6), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 6), V_{OUT} = 2.5		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV
CD74FCT16652T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range, $T_A = -40^oC$ to 85^oC, $V_{CC} = 5.0V \pm 10\%$							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA
CD74FCT162652T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range, $T_A = -40^oC$ to 85^oC, $V_{CC} = 5.0V \pm 10\%$							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, $V_{IN} = V_{IH}$ or V_{IL}, V_{OUT} = 1.5V (Note 6)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, $V_{IN} = V_{IH}$ or V_{IL}, V_{OUT} = 1.5V (Note 6)		-60	-115	-150	mA

Electrical Specifications (Continued)

PARAMETERS	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 7)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 7)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 8)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 9)	I_{CCD}	V_{CC} = Max, Outputs Open xOEAB = $x\overline{OEBA}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	75	120	µA/ MHz
Total Power Supply Current (Note 11)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle xOEAB = $x\overline{OEBA}$ = GND One Bit Toggling f_i = 5MHz, 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	0.8	1.7 (Note 10)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.3	3.2 (Note 10)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle xOEAB = $x\overline{OEBA}$ = GND 16 Bits Toggling f_i = 2.5MHz, 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	3.8	6.5 (Note 10)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	8.3	22.0 (Note 10)	mA

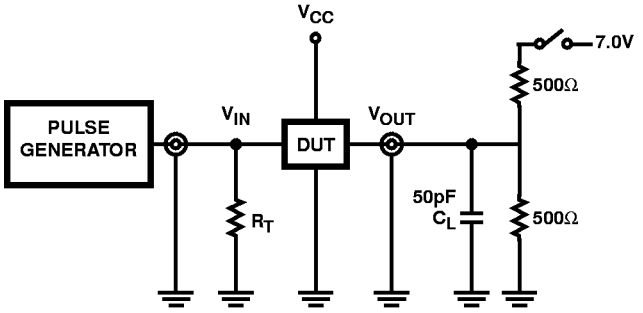
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 12) TEST CONDITIONS	T		AT		CT		DT		UNITS
			(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	
Propagation Delay Bus to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.4	ns
Output Enable Time $_X$OEAB or $_X\overline{OEBA}$ to Bus	t_{PZH}, t_{PZL}		2.0	14.0	2.0	9.8	1.5	7.8	1.5	5.0	ns
Output Disable Time (Note 14) $_X$OEAB or $_X\overline{OEBA}$ to Bus	t_{PHZ}, t_{PLZ}		2.0	9.0	2.0	6.3	1.5	6.3	1.5	4.3	ns
Propagation Delay Clock to Bus	t_{PLH}, t_{PHL}		2.0	9.0	2.0	6.3	1.5	5.7	1.5	4.4	ns
Propagation Delay $_X$SBA or $_X$SAB to Bus	t_{PLH}, t_{PHL}		2.0	11.0	2.0	7.7	1.5	6.2	1.5	5.0	ns
Setup Time HIGH or LOW, Bus to Clock	t_{SU}		4.0	-	2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, Bus to Clock	t_H		2.0	-	1.5	-	1.5	-	1.0	-	ns
Clock Pulse Width HIGH or LOW (Note 14)	t_W		6.0	-	5.0	-	5.0	-	3.0	-	ns
Output Skew (Note 15)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

4. For conditions shown as Max or Min, use appropriate value specified under Electrical Characteristics for the applicable device type.
5. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
6. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
7. This parameter is determined by device characterization but is not production tested.
8. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
10. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
11. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
12. See test circuit and wave forms.
13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. This parameter is guaranteed but not production tested.
15. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

16. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 5. TEST CIRCUIT

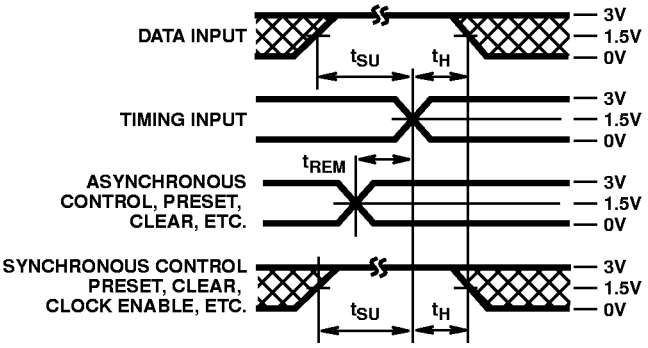


FIGURE 6. SETUP, HOLD, AND RELEASE TIMING

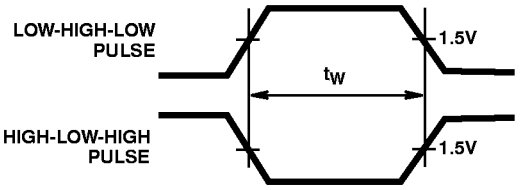


FIGURE 7. PULSE WIDTH

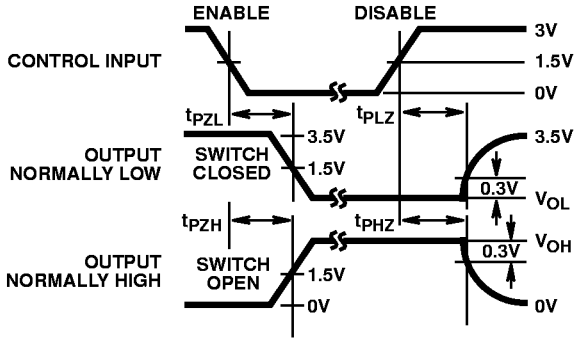


FIGURE 8. ENABLE AND DISABLE TIMING

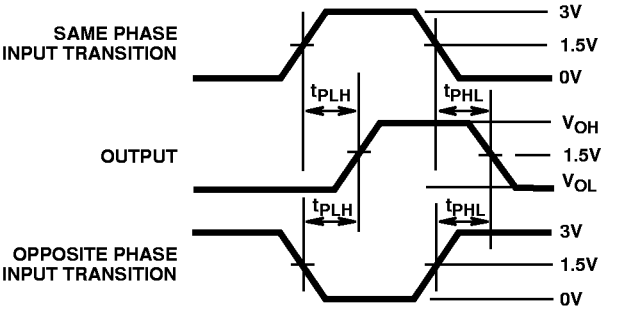


FIGURE 9. PROPAGATION DELAY