



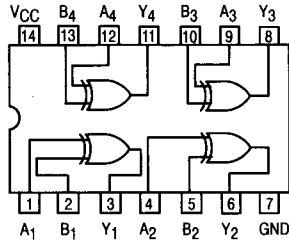
Quad 2-Input Exclusive OR Gate

ELECTRICALLY TESTED PER:
MIL-M-38510/30502

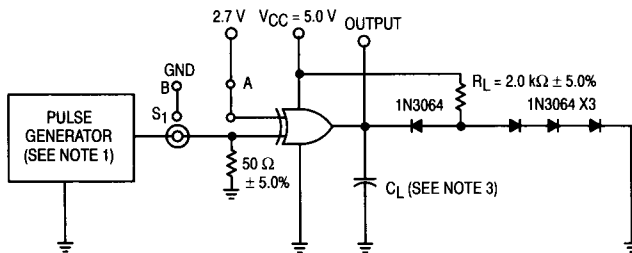
Military 54LS86



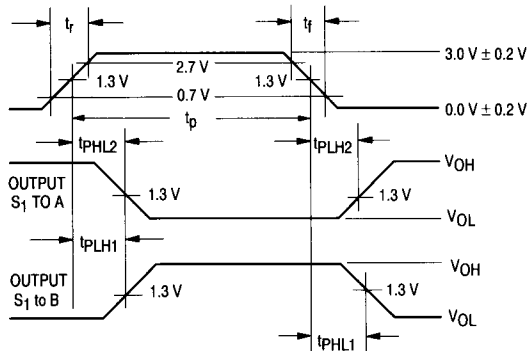
LOGIC DIAGRAM



AC TEST CIRCUIT



WAVEFORMS



AVAILABLE AS:

- 1) JAN: JM38510/30502BXA
- 2) SMD: N/A
- 3) 883: 54LS86/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
A1	1	1	2	VCC
B1	2	2	3	GND
Y1	3	3	4	VCC
A2	4	4	6	VCC
B2	5	5	8	GND
Y2	6	6	9	VCC
GND	7	7	10	GND
Y3	8	8	12	VCC
A3	9	9	13	VCC
B3	10	10	14	GND
Y4	11	11	16	VCC
A4	12	12	18	VCC
B4	13	13	19	GND
VCC	14	14	20	VCC

BURN-IN CONDITIONS:

VCC = 5.0 V MIN/6.0 V MAX

NOTES:

1. Pulse generator has the following characteristics: $V_{gen} = 3.0 \pm 0.2$ V, $t_f \leq 6.0$ ns, $t_r \leq 15$ ns. PRR ≤ 1.0 MHz, $t_p = 0.5$ μ s, and $Z_{OUT} \approx 50\Omega$.
2. Each gate tested separately.
3. $C_L = 50$ pF $\pm 10\%$, including scope probe, wiring and stray capacitance.
4. Voltage measurements are to be made with respect to network ground terminal.
5. $R_L = 2.0$ k Ω $\pm 5.0\%$.

54LS86

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OL} = - 400 μA, V _{IL} = 0.7 V, V _{IN} = 2.0 V on other input.
V _{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IL} = 0.7 V on both inputs.
V _{IC}	Input Clamping Voltage		- 1.5					V	V _{CC} = 4.5 V, I _{IN} = - 18 mA, other input is open.
I _{IH}	Logical "1" Input Current		40		40		40	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other input = 0 V.
I _{IHH}	Logical "1" Input Current		200		200		200	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, other input = 0 V.
I _{IL}	Logical "0" Input Current	- 225	- 705	- 225	- 705	- 225	- 705	μA	V _{CC} = 5.5 V, V _{IN} = 0.4 V, other input = 5.5 V.
I _{OS}	Output Short Circuit Current	- 15	- 100	- 15	- 100	- 15	- 100	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V, other input = 0 V, V _{OUT} = 0 V.
I _{CC}	Power Supply Current		10		10		10	mA	V _{CC} = 5.5 V, V _{IN} = 0 V (all inputs).
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.4 V, and V _{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL1} t _{PHL1}	Propagation Delay /Data-Output Output High-Low	2.0 —	22 17	2.0 —	29 24	2.0 —	29 24	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ.
t _{PLH1} t _{PLH1}	Propagation Delay /Data-Output Output Low-High	2.0 —	28 23	2.0 —	37 32	2.0 —	37 32	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ.
t _{PHL2} t _{PHL2}	Propagation Delay /Data-Output Output High-Low	2.0 —	27 23	2.0 —	35 30	2.0 —	35 30	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ.
t _{PLH2} t _{PLH2}	Propagation Delay /Data-Output Output Low-High	2.0 —	32 30	2.0 —	40 38	2.0 —	40 38	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ.

NOTE:

- The limits specified for C_L = 15 pF are guaranteed but not tested.