TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TB62725P, TB62725F, TB62725FN

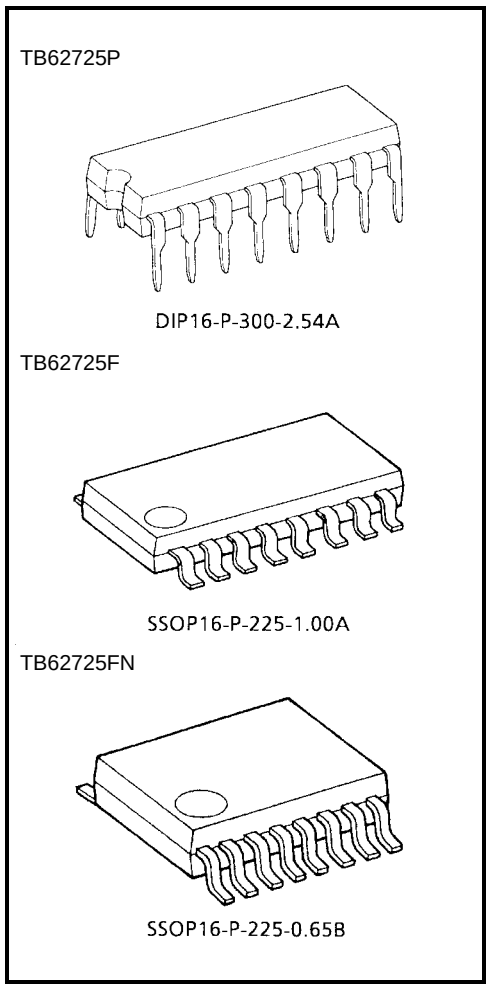
8-bit Constant-Current LED Driver with Operating Voltage of 3.3 V

The TB62725 series is comprised of constant-current drivers designed for LEDs and LED displays. The output current value can be set using an external resistor.

As a result, all outputs will have virtually the same current levels.

This driver incorporates a 8-bit constant-current output, a 8-bit shift register, a 8-bit latch and a gate circuit.

These drivers have been designed using the Bi-CMOS process.



Weight
DIP16-P-300-2.54A: 1.11 g (typ.)
SSOP16-P-225-1.00A: 0.14 g (typ.)
SSOP16-P-225-0.65B: 0.07 g (typ.)

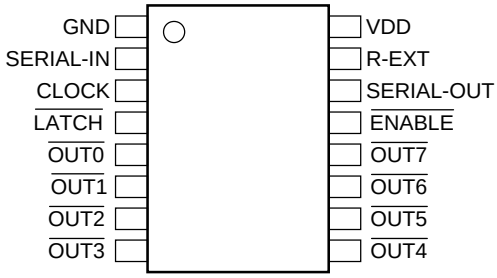
Features

- Output current capability and number of outputs:
  90 mA × 8 outputs
- Constant current range: 2~80 mA
- Application output voltage:
  0.7 V (output current 2~80 mA)
  0.4 V (output current 2~40 mA)
- For anode-common LEDs
- Input signal voltage level: 3.3-V CMOS level (Schmitt trigger input)
- Maximum output terminal voltage: 17 V
- Serial data transfer rate: 20 MHz (max, cascade connection)
- Operating temperature range T_{opr} = −40~85°C
- Package:
  Type P: DIP16-P-300-2.54A
  Type F: SSOP16-P-225-1.00A
  Type FN: SSOP16-P-225-0.65B
- Package and pin layout: Pin layout and functionality are similar to those of the TB62705. (Each characteristic value is different.)
- Constant-current error accuracy (all outputs on)

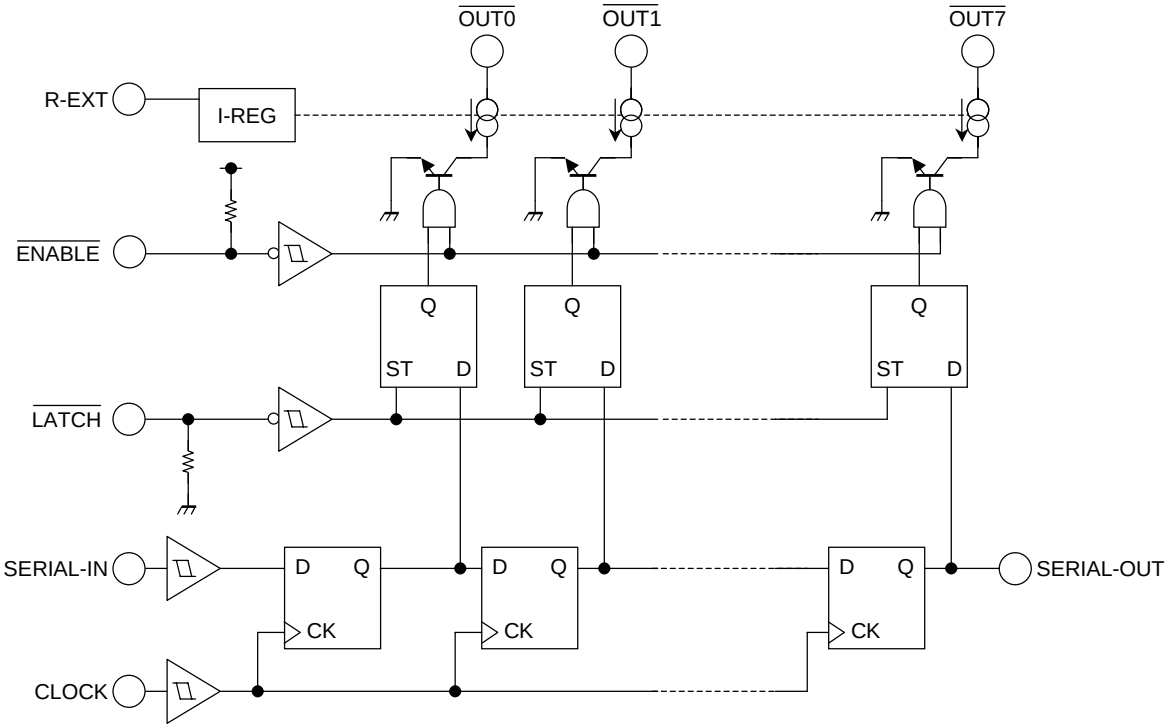
	Current accuracy		
	between bits	between ICs	
≧ 0.4 V			2~40 mA
≧ 0.7 V			2~80 mA

Pin Assignment (top view)

Pin layout and functionality are similar to those of the TB62705C. (each characteristic value is different.)



Block Diagram

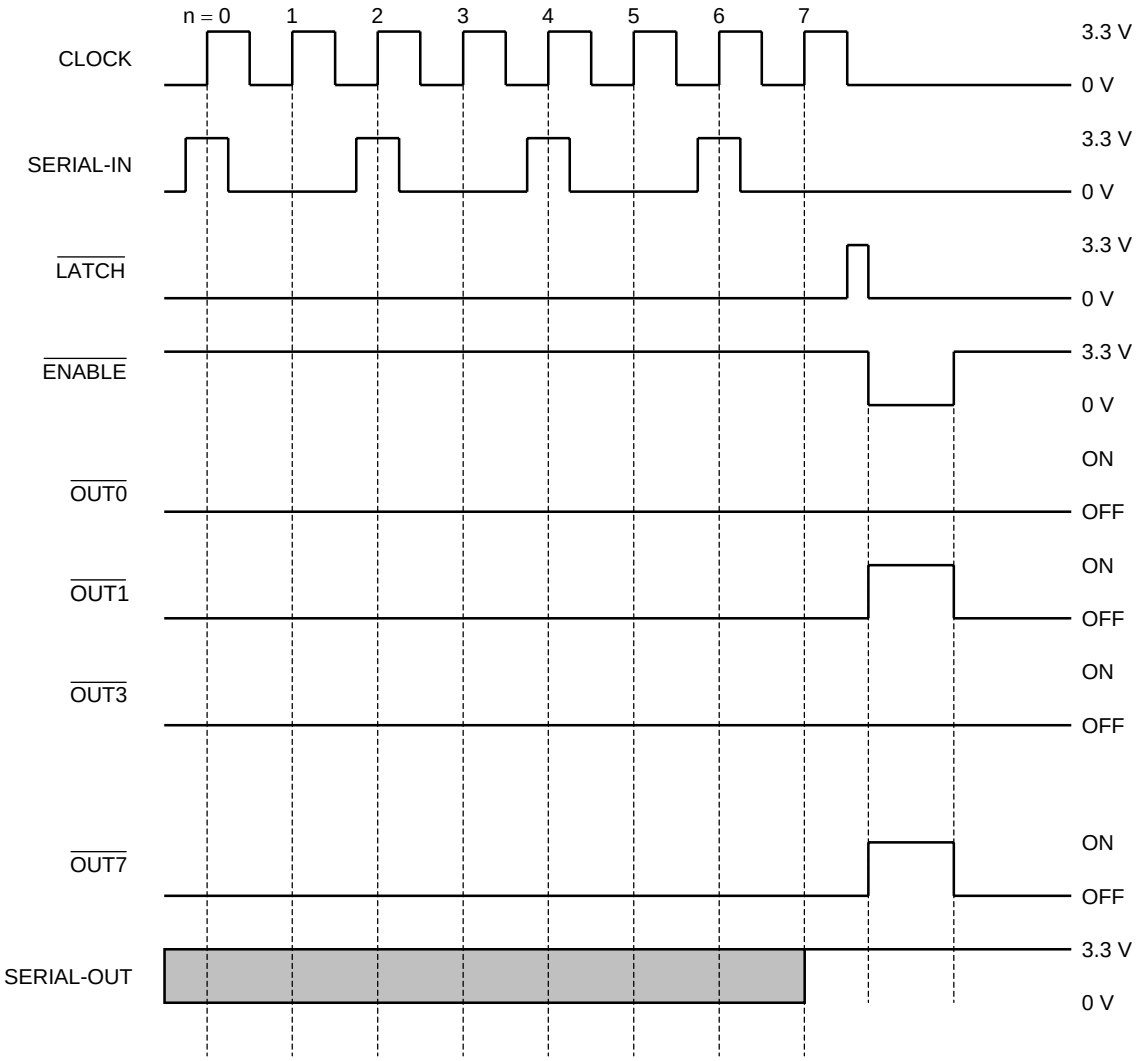


Truth Table

CLOCK	LATCH	ENABLE	SERIAL-IN	OUT0 ⋯ OUT5 ⋯ OUT7	SERIAL-OUT
↑	H	L	Dn	Dn ⋯ Dn – 5 ⋯ Dn – 7	Dn – 7
↑	L	L	Dn + 1	No Change	Dn – 6
↑	H	L	Dn + 2	Dn + 2 ⋯ Dn – 3 ⋯ Dn – 5	Dn – 5
↓	X	L	Dn + 3	Dn + 2 ⋯ Dn – 3 ⋯ Dn – 5	Dn – 5
↓	X	H	Dn + 3	OFF	Dn – 5

Note 1: $\overline{OUT0}$ ~ $\overline{OUT7}$ = ON when Dn = “H”; $\overline{OUT1}$ ~ $\overline{OUT7}$ = OFF when Dn = “L”.
In order to ensure that the level of the power supply voltate is correct, an external resistor must be connected between R-EXT and GND.

Timing Diagram



Warning: Latch circuit is leveled-latch circuit. Be careful because it is not triggered-latch circuit.

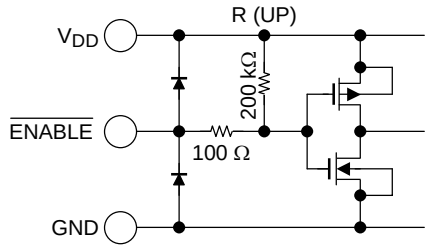
Note 2: The latches circuit holds data by pulling the $\overline{\text{LATCH}}$ terminal Low.
And, when $\overline{\text{LATCH}}$ terminal is a “H” level, latch circuit doesn’t hold data, and it passes from the input to the output.
When $\overline{\text{ENABLE}}$ terminal is a “L” level, output terminal $\overline{\text{OUT0}}$ ~ $\overline{\text{OUT7}}$ respond to the data, and on & off does.
And, when $\overline{\text{ENABLE}}$ terminal is a “H” level, it offs with the output terminal regardless of the data.

Terminal Description

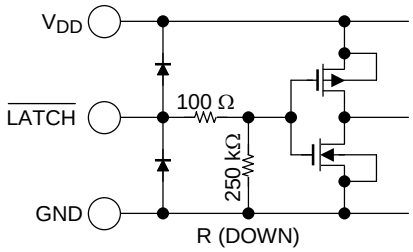
Pin No.	Pin Name	Function
1	GND	GND terminal for control logic.
2	SERIAL-IN	Input terminal for serial data for data shift register.
3	CLOCK	Input terminal for clock for data shift on rising edge.
4	$\overline{\text{LATCH}}$	Input terminal for data strobe. When the $\overline{\text{LATCH}}$ input is driven High, data is latched. When it is pulled Low, data is hold.
5~12	$\overline{\text{OUT0}}$ ~ $\overline{\text{OUT7}}$	Constant-current output terminals.
13	$\overline{\text{ENABLE}}$	Input terminal for output enable. All outputs ($\overline{\text{OUT0}}$ ~ $\overline{\text{OUT7}}$) are turned off, when the $\overline{\text{ENABLE}}$ terminal is driven High. And are turned on, when the terminal is driven Low.
14	SERIAL-OUT	Output terminal for serial data input on SERIAL-IN terminal.
15	R-EXT	Input terminal used to connect an external resistor. This regulated the output current.
16	V_{DD}	3.3-V supply voltage terminal.

Equivalent Circuits for Inputs and Outputs

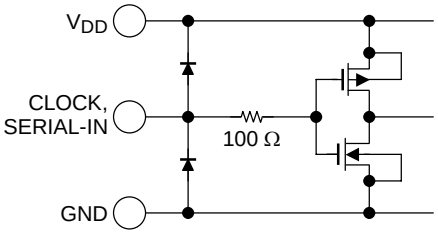
$\overline{\text{ENABLE}}$ terminal



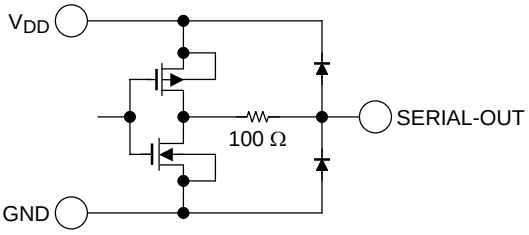
$\overline{\text{LATCH}}$ terminal



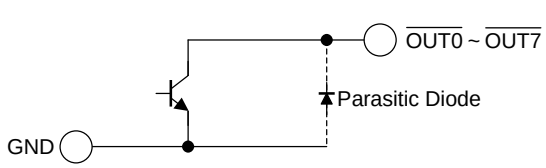
CLOCK, SERIAL-IN terminal



SERIAL-OUT terminal



$\overline{\text{OUT0}}$ ~ $\overline{\text{OUT7}}$ terminals



Maximum Ratings (T_{opr} = 25°C)

Characteristics		Symbol	Rating	Unit
Supply voltage		V_{DD}	7	V
Input voltage		V_{IN}	−0.2~V_{DD} + 0.2	V
Output current		I_{OUT}	90	mA/ch
Output voltage		V_{OUT}	−0.2~17	V
Power Dissipation (Note 3)	P-type (when not mounted)	P_{d1}	1.47	W
	F/FN-type (when not mounted)	P_{d2}	0.37	
	F/FN-type (On PCB)		0.78	
Thermal Resistance (Note 3)	P-type (when not mounted)	$R_{th\ (j\text{-}a)\ 1}$	85	°C/W
	F/FN-type (when not mounted)	$R_{th\ (j\text{-}a)\ 2}$	330	
	F/FN-type (On PCB)		160	
Operating Temperature		T_{opr}	−40~85	°C
Storage Temperature		T_{stg}	−55~150	°C

Note 3: N-Type: Powes dissipation is derated by 11.76 mW/°C if device is mounted on PCB and ambient temperature is above 25°C.
F- and FN-Type: Powes dissipation is derated by 7.69 mW/°C if device is mounted on PCB and ambient temperature is above 25°C.

With device mounted on glass-epoxy PCB of less than 40% Cu and of dimensions
50 mm × 50 mm × 1.6 mm

Recommended Operating Conditions (T_{opr} = –40°C ~85°C unless otherwise specified)

Characteristics		Symbol	Conditions		Min	Typ.	Max	Unit
Supply voltage		V_{DD}	—		3	3.3	3.6	V
Output voltage		V_{OUT}	—		—	0.7	4	V
Output current		I_{OUT}	Each DC 1 circuit		2	—	80	mA/ch
		I_{OH}	SERIAL-OUT		—	—	−1	mA
		I_{OL}	SERIAL-OUT		—	—	1	
Input voltage		V_{IH}	—		0.7 × V_{DD}	—	V_{DD} + 0.15	mA
		V_{IL}			−0.15	—	0.3 × V_{DD}	
Clock frequency		f_{CLK}	Cascade Connected		—	—	20	MHz
$\overline{\text{LATCH}}$ pulse width		t_{wLAT}	—		50	—	—	ns
$\overline{\text{ENABLE}}$ pulse width (Note 4)		t_{wENA}	$I_{OUT} \geqq$ 20 mA		2	—	—	μs
			$I_{OUT} \leqq$ 20 mA		3	—	—	
CLOCK pulse width		t_{wCLK}	—		25	—	—	ns
Set-up time for CLOCK terminal		t_{SETUP1}			10	—	—	
Hold time for CLOCK terminal		t_{HOLD}			5	—	—	
Set-up time for $\overline{\text{LATCH}}$ terminal		t_{SETUP2}			50	—	—	
Power dissipation	P-type	P_{d1}	T_{opr} = 85°C	When not mounted	—	—	0.82	W
	F-type	P_{d2}		On PCB	—	—	0.35	
	FN-type	P_{d3}			—	—	0.35	

Note 4: When the pulse of the “L” level is inputted to the $\overline{\text{ENABLE}}$ terminal held in the “H” level.

Electrical Characteristics (T_{opr} = 25°C, V_{DD} = 3.3 V unless otherwise specified)

Characteristics	Symbol	Test Circuit	Conditions		Min	Typ.	Max	Unit
Supply voltage	V_{DD}	—	Normal operation		3.0	3.3	3.6	V
Output current	I_{OUT1}	—	V_{OUT} = 0.4 V	R_{EXT} = 490 Ω	29.8	35.1	40.3	mA
	I_{OUT2}	—	V_{OUT} = 0.7 V	R_{EXT} = 250 Ω	58.4	68.7	79.0	
Output current Error between bits	ΔI_{OUT1}	—	V_{OUT} = 0.4 V, All outouts ON	R_{EXT} = 490 Ω	—	±1.5	±6	%
	ΔI_{OUT2}	—	V_{OUT} = 0.7 V, All outouts ON	R_{EXT} = 250 Ω	—	±1.5	±6	
Output leakage current	I_{OZ}	—	V_{OUT} = 15 V		—	1	5	μA
Input voltage	V_{IH}	—	—		0.7 V_{DD}	—	V_{DD}	V
	V_{IL}	—	—		GND	—	0.3 V_{DD}	
SOUT terminal Output voltage	V_{OH}	—	I_{OH} = 1.0 mA		—	—	0.3	V
	V_{OL}	—	I_{OL} = −1.0 mA		3	—	—	
Output current Supply voltage Regulation	%/V_{DD}	—	V_{DD} = 3 V → 3.6 V		—	−1.5	−5	%
Pull-up resistor	$R_{(Up)}$	—	$\overline{ENABLE}$ terminal		100	200	400	kΩ
Pull-down resistor	$R_{(Down)}$	—	$\overline{LATCH}$ terminal		125	250	500	
Supply current	$I_{DD\ (OFF)\ 1}$	—	V_{OUT} = 15.0 V	R_{EXT} = OPEN	—	1	2	mA
	$I_{DD\ (OFF)\ 2}$	—	V_{OUT} = 15.0 V, All outputs OFF	R_{EXT} = 490 Ω	1	3	5	
	$I_{DD\ (OFF)\ 3}$	—	V_{OUT} = 15.0 V, All outputs OFF	R_{EXT} = 250 Ω	3	6	8	
	$I_{DD\ (ON)\ 1}$	—	V_{OUT} = 0.7 V, All outputs ON	R_{EXT} = 490 Ω	—	6	9	
		—	Same as the above, T_{opr} = −40°C		—	—	15	
	$I_{DD\ (ON)\ 2}$	—	V_{OUT} = 0.7 V, All outputs ON	R_{EXT} = 250 Ω	—	12	17	
		—	Same as the above, T_{opr} = −40°C		—	—	29	

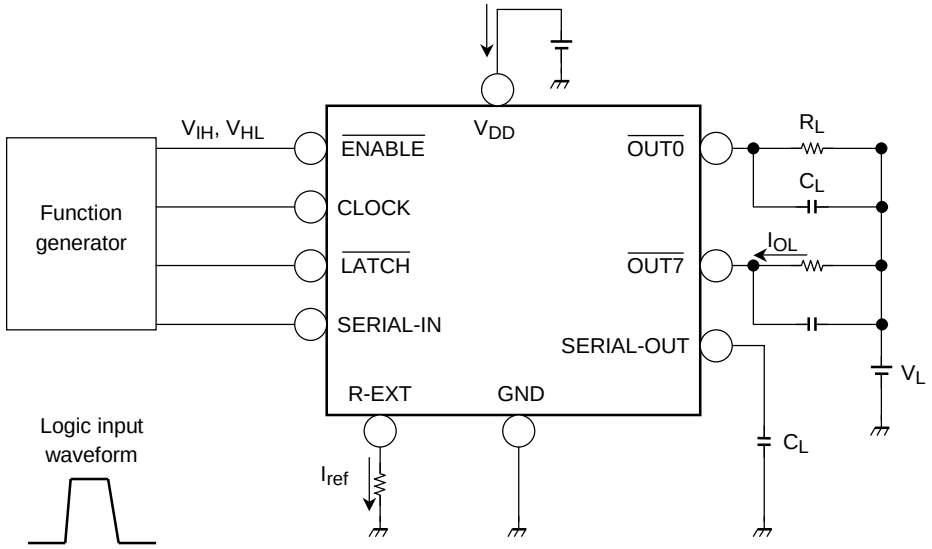
Switching Characteristics (T_{opr} = 25°C unless otherwise specifed)

Characteristics	Symbol	Test circuit	Conditions	Min	Typ.	Max	Unit
Propagation delay time	t_{pLH1}	—	CLK- $\overline{OUTn}$, $\overline{LATCH}$ = "H", $\overline{ENABLE}$ = "L"	—	150	300	ns
	t_{pLH2}	—	$\overline{LATCH}$ - $\overline{OUTn}$, $\overline{ENABLE}$ = "L"	—	140	300	
	t_{pLH3}	—	$\overline{ENABLE}$ - $\overline{OUTn}$, $\overline{LATCH}$ = "H"	—	140	300	
	t_{pLH}	—	CLK-SERIAL OUT	2	5	—	
	t_{pHL1}	—	CLK- $\overline{OUTn}$, $\overline{LATCH}$ = "H", $\overline{ENABLE}$ = "L"	—	170	340	
	t_{pHL2}	—	$\overline{LATCH}$ - $\overline{OUTn}$, $\overline{ENABLE}$ = "L"	—	170	340	
	t_{pHL3}	—	$\overline{ENABLE}$ - $\overline{OUTn}$, $\overline{LATCH}$ = "H"	—	170	340	
	t_{pHL}	—	CLK-SERIAL OUT	2	5	—	
Output rise time	t_{or}	—	10~90% of voltage waveform	40	85	150	ns
Output fall time	t_{of}	—	90~10% of voltage waveform	40	70	150	ns
Maximum CLOCK rise time	t_r	—	Cascade connection isn't guarantee. (Note 5)	—	—	5	us
Maximum CLOCK fall time	t_f	—		—	—	5	us

Conditions: (Refer to test circuit.)
T_{opr} = 25°C, V_{DD} = V_{IH} = 3.3 V, V_{OUT} = 0.7 V, V_{IL} = 0 V, R_{EXT} = 490 Ω, I_{OUT} = 37.5 mA,
V_L = 3.0 V, R_L = 60 Ω, C_L = 10.5 pF

Note 5: If the device is connected in a cascade and t_r/t_f for the waveform is large, it may not be possible to achieve the timing required for data transfer. Please consider the timings carefully.

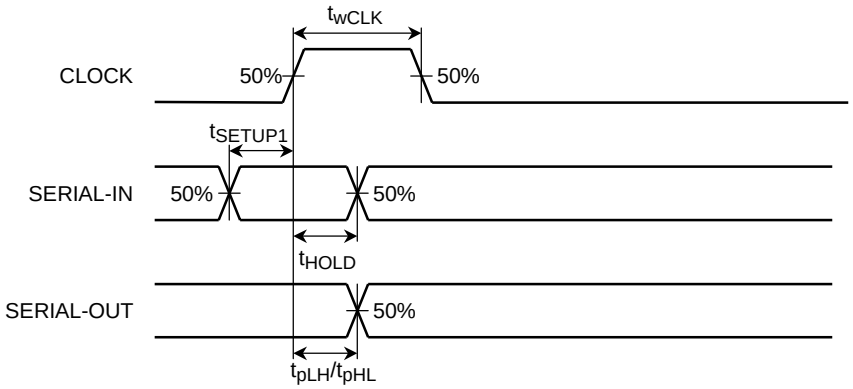
Test Circuit



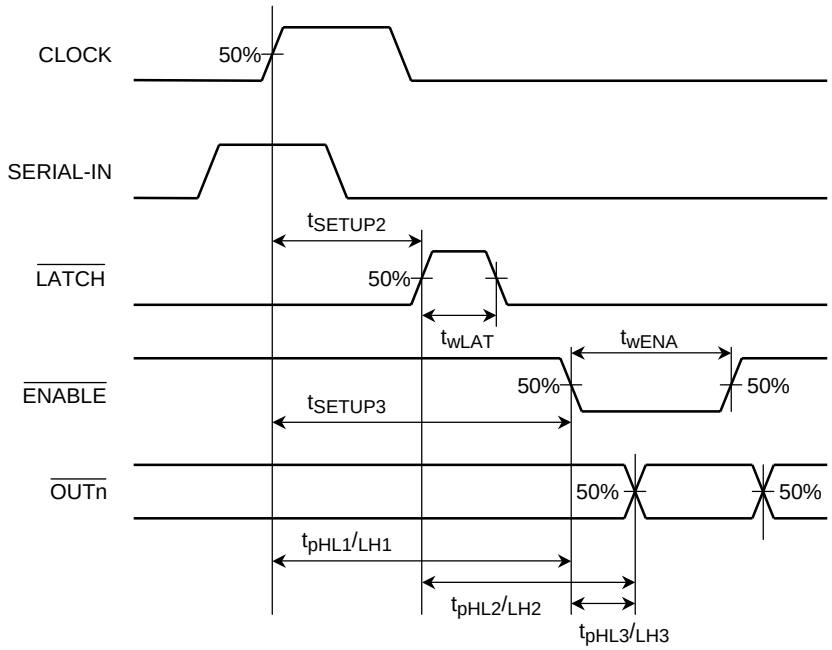
V_{DD} = V_{IH} = 3.3 V
V_{IL} = 0 V
t_r = t_f = 10 ns
(10% to 90%)

Timing Waveforms

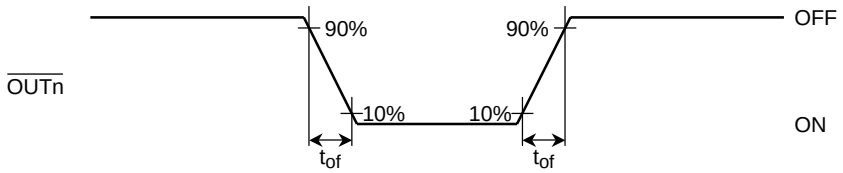
1. CLOCK, SERIAL-IN, SERIAL-OUT



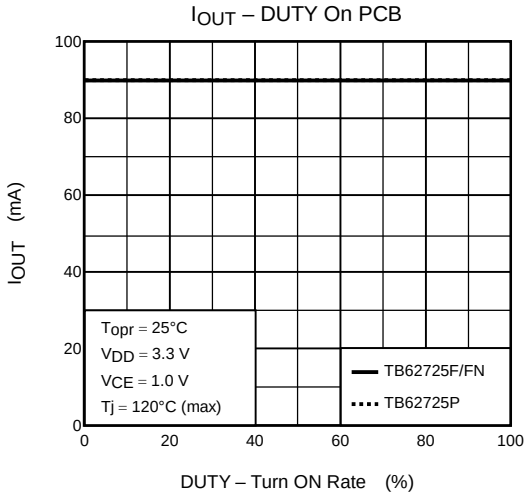
2. CLOCK, SERIAL-IN, $\overline{\text{LATCH}}$, $\overline{\text{ENABLE}}$, $\overline{\text{OUTn}}$

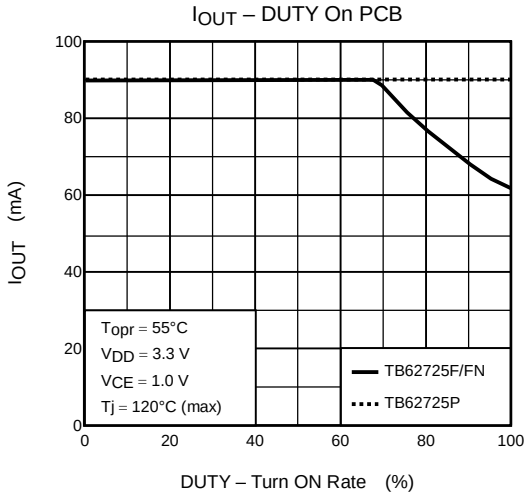


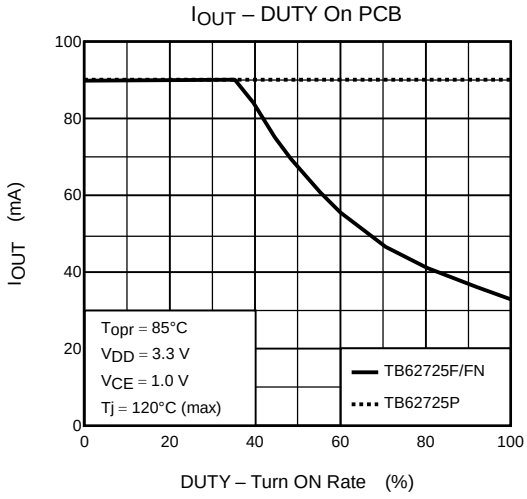
3. $\overline{\text{OUTn}}$

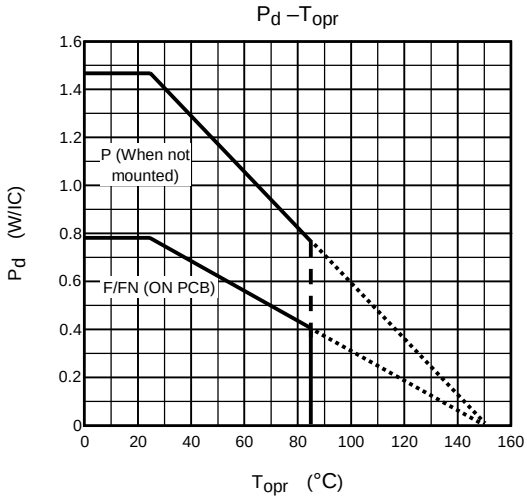


Output Curent – Duty (LED turn-on rate)

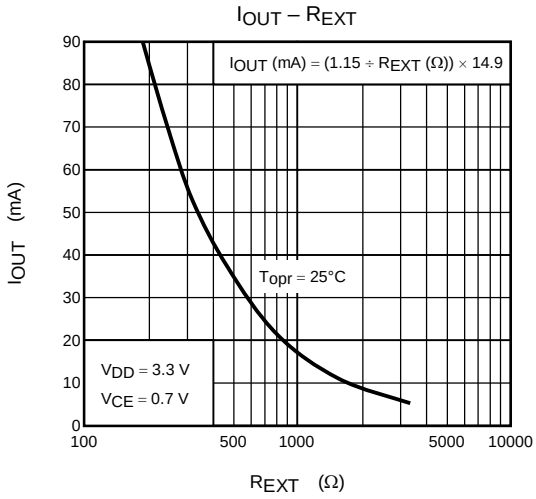








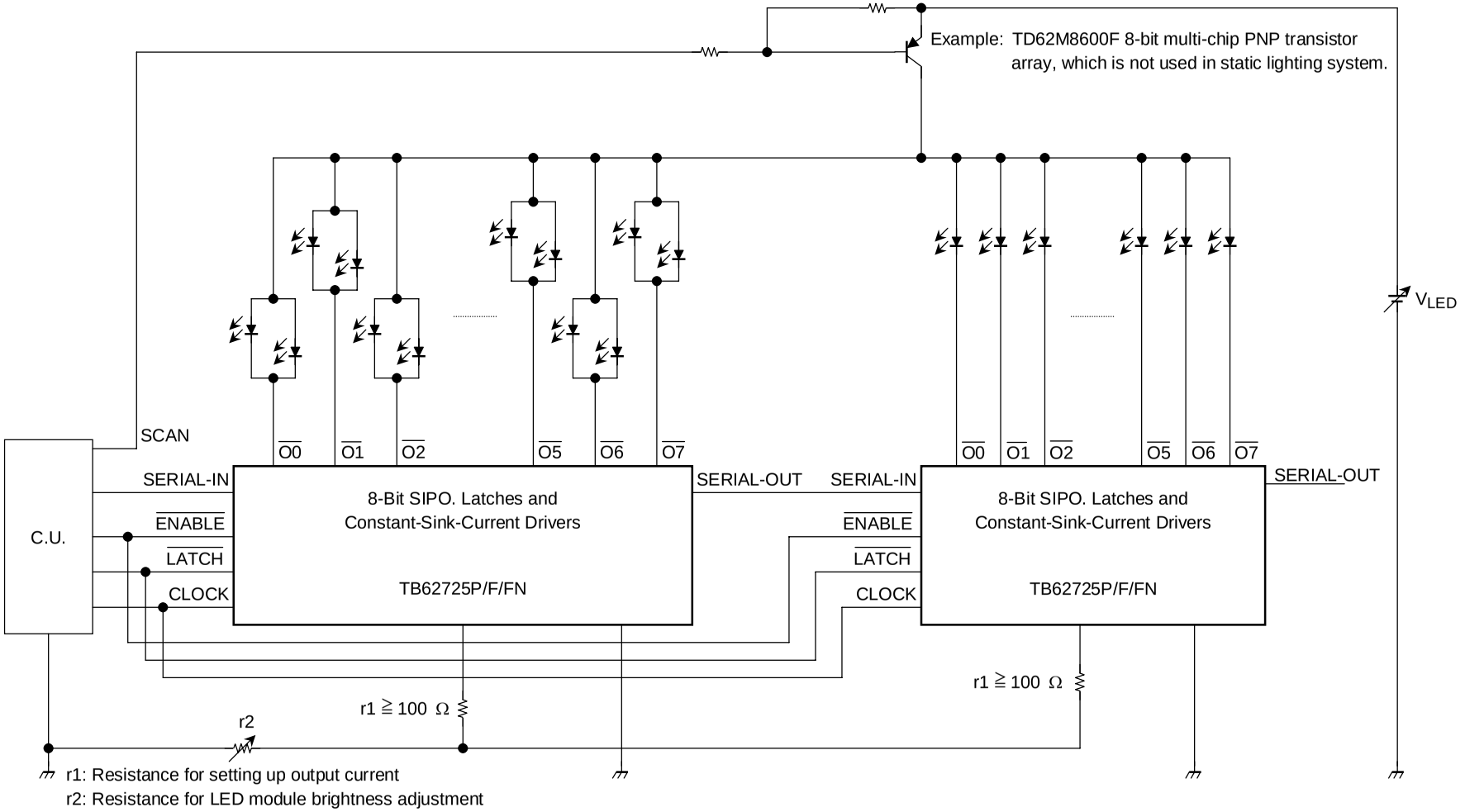
Output Current – R_{EXT} Resistor



Application Notes (example 1)

It is recommended that TB62726 Series recommend device be used in a cascade connection with $V_{LED} = V_{DD} = 3.3$ V and a data transfer rate fclk = 20 (MHz)

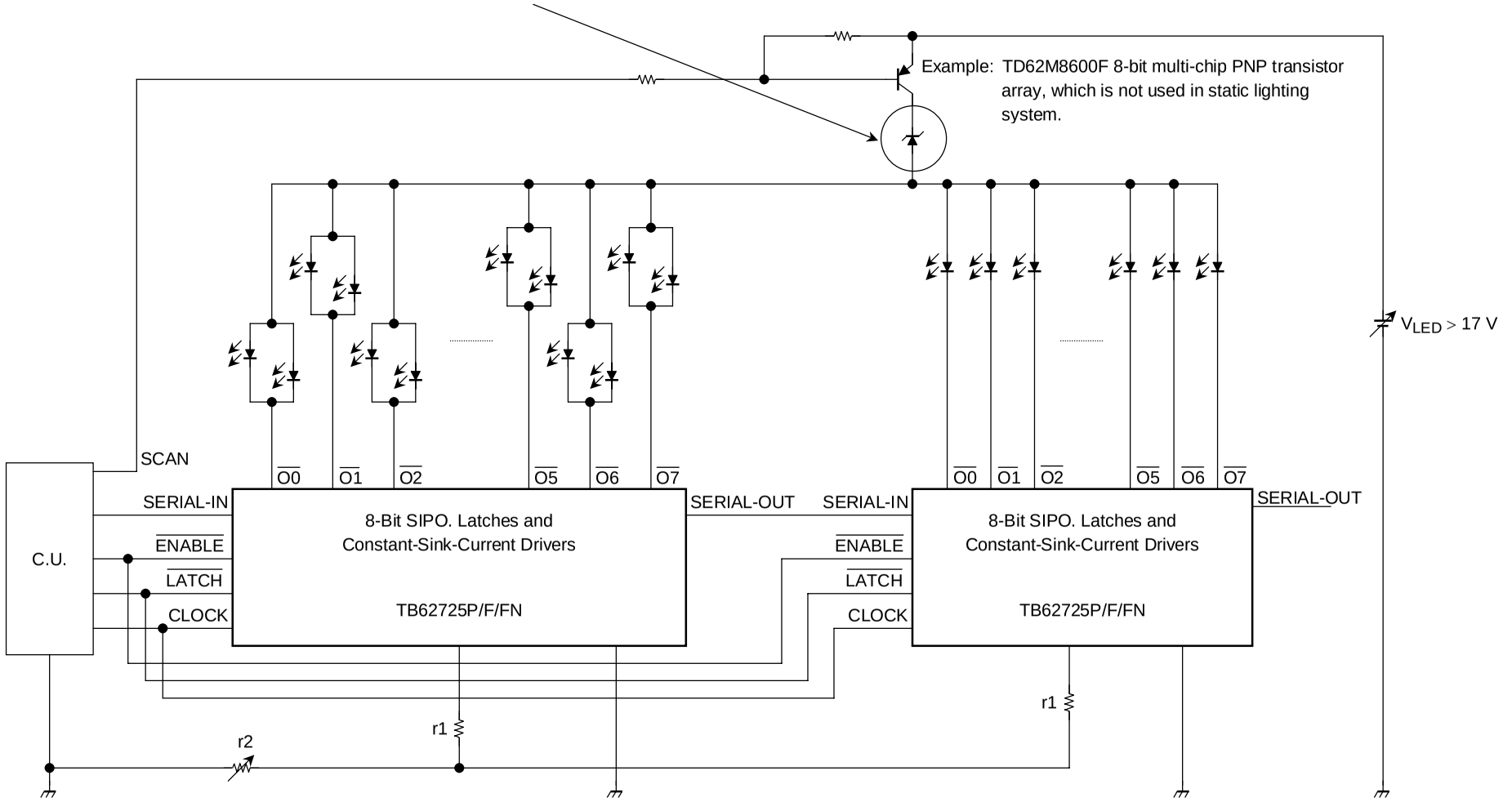
(1) V_f of LED is $V_f = 2.5$ V (max).
(2) Output saturation Vce1 = 0.4 V (min) at TB62726 $I_{out} \leqq 40$ mA
(3) Output saturation Vce2 = 0.25 V (max) at TD62M8600F Ic = −1 A
(4) TB62726 can operate with VDDopr = 3.3 V ±0.3 V



Application Notes (example 2)

TB62725P/F/FN application circuit (for V_{LED} > 17 V)

Example: An unnecessary voltage in the case of V_{LED} > 17 V makes a voltage descend by the Zener diode.



r1: Resistance for setting up output current
r2: Resistance for LED module brightness adjustment

Application Notes (example 3)

TB62725P/F/FN application circuit (with $V_{LED} \leqq 17$ V, the case of the over-saturation)

Example: An over-saturation voltage makes a voltage descend by the resistance with the outside.

Conditions: (1) LED is turned on when I_{OUT} = 20 mA.

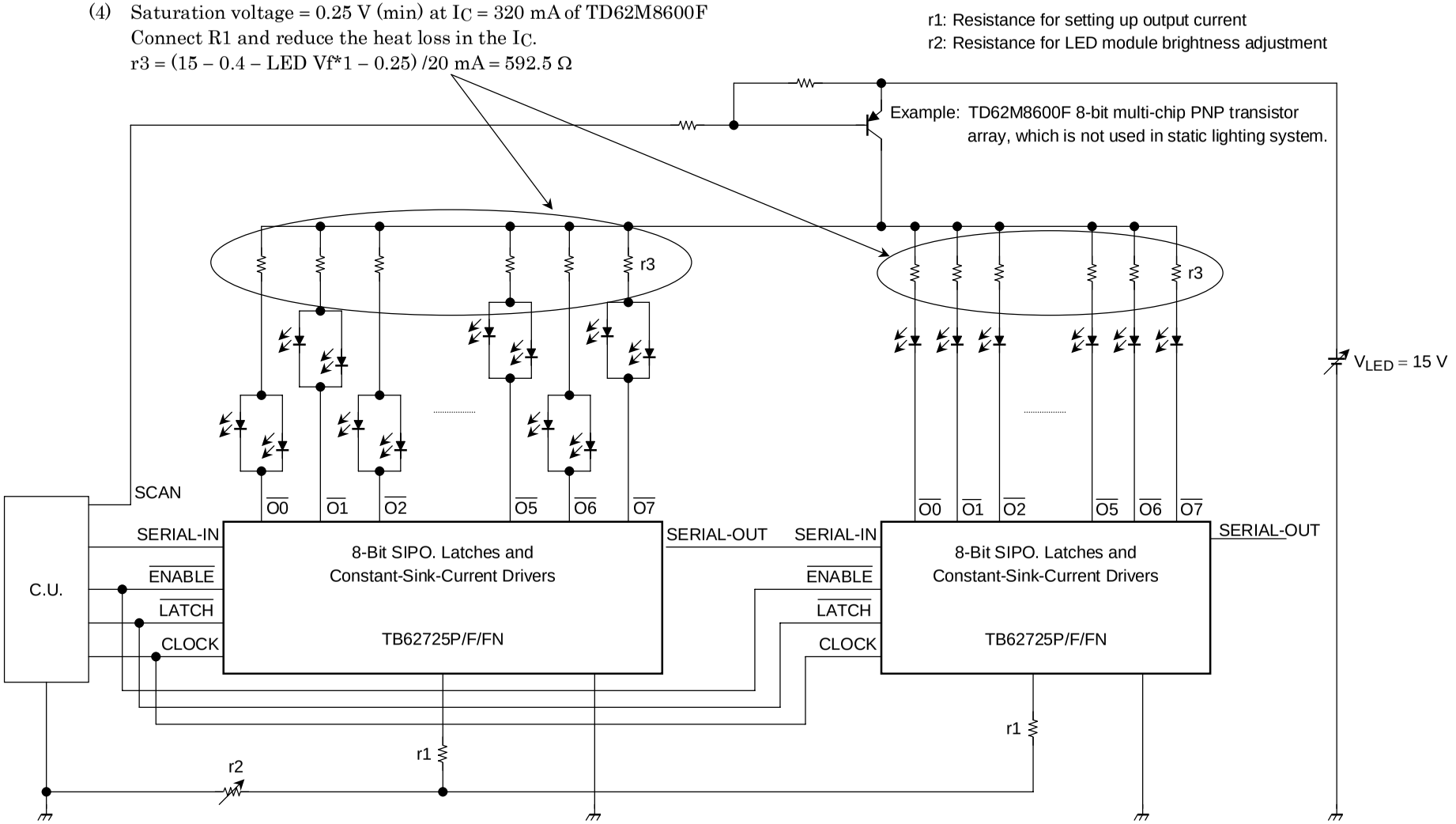
(2) LED of V_f = 2.5 V (max).

(3) Saturation voltage = 0.4 V (min) at I_C = 20 mA of TB62725

(4) Saturation voltage = 0.25 V (min) at I_C = 320 mA of TD62M8600F

Connect R1 and reduce the heat loss in the I_C.

r3 = (15 – 0.4 – LED Vf*1 – 0.25) /20 mA = 592.5 Ω



Notes

- Operation may become unstable due to the electromagnetic interference caused by the wiring and other phenomena.
  To counter this, it is recommended that the IC be situated as close as possible to the LED module.
  If overvoltage is caused by inductance between the LED and the output terminals, both the LED and the terminals may suffer damage as a result.

- There is only one GND terminal on this device when the inductance in the GND line and the resistor are large, the device may malfunction due to the GND noise when output switchings by the circuit board pattern and wiring.
  To achieve stable operation, it is necessary to connect a resistor between the REXT terminal and the GND line.
  Fluctuation in the output waveform is likely to occur when the GND line is unstable or when a capacitor (of more than 50 pF) is used.
  Therefore, take care when designing the circuit board pattern layout and the wiring from the controller.

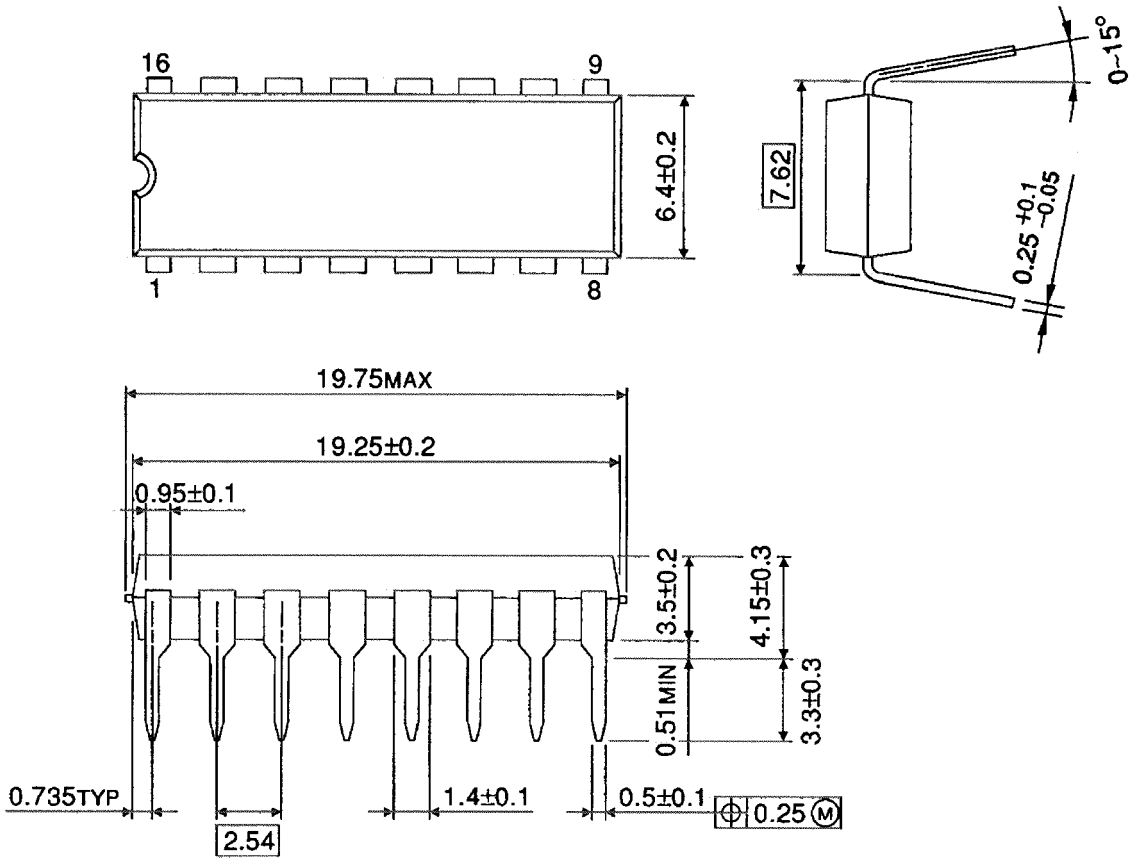
- This application circuit is a reference example and is not guaranteed to work in all conditions.
  Be sure to check the operation of your circuits.

- This device does not include protection circuits for overvoltage, overcurrent or overtemperature.
  If protection is necessary, it must be incorporated into the control circuitry.

- The device is likely to be destroyed if a short-circuit occurs between either of the power supply pins and any of the output terminals when designing circuits, pay special attention to the positions of the output terminals and the power supply terminals (V_{DD} and V_{LED}), and to the design of the GND line.

Package Dimensions

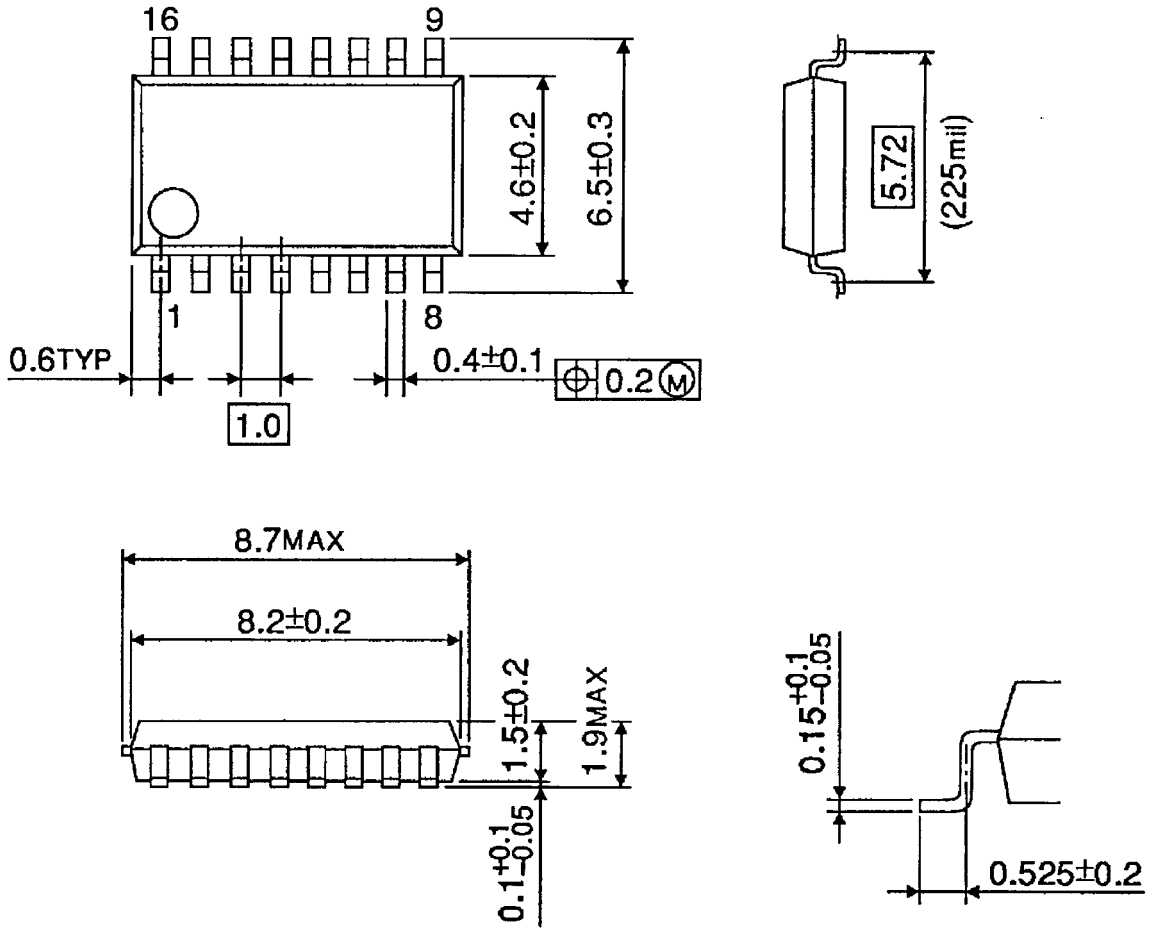
DIP16-P-300-2.54A Unit : mm



Weight: 1.1 g (typ.)

Package Dimensions

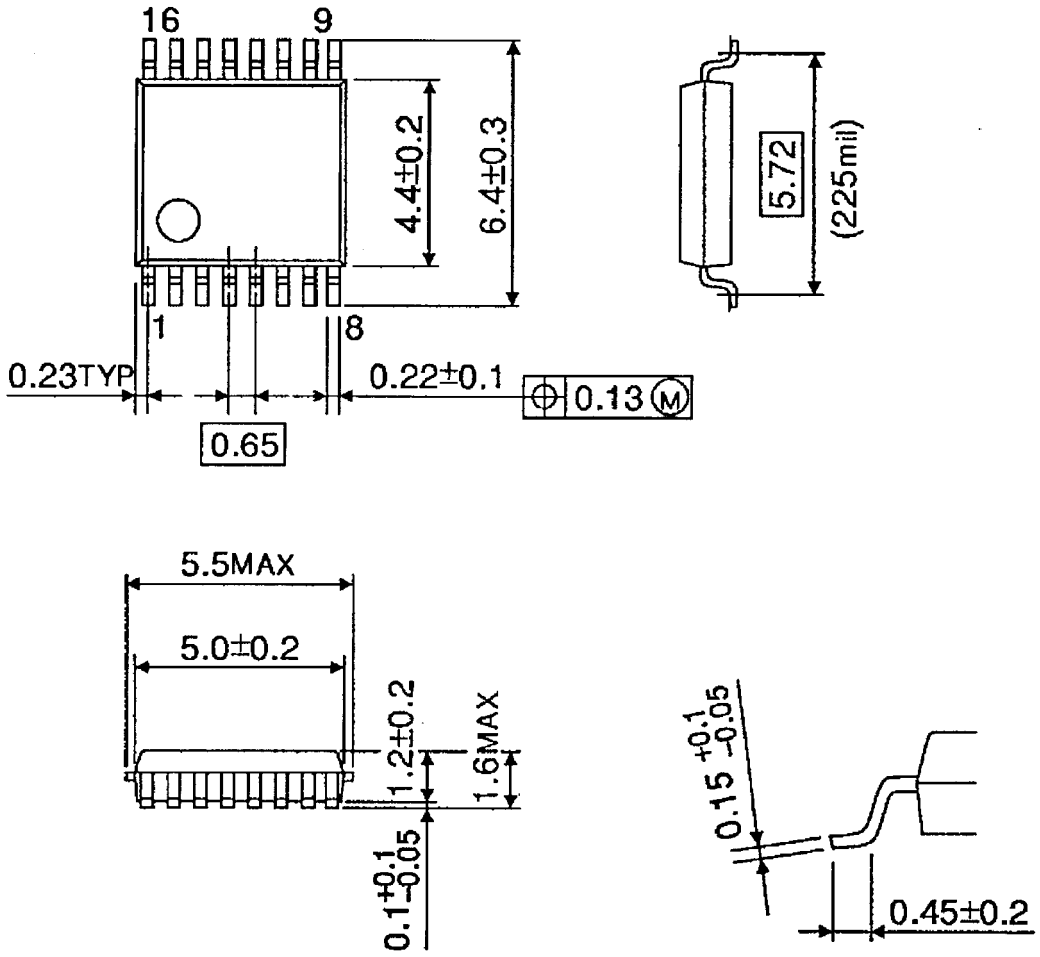
SSOP16-P-225-1.00A Unit : mm



Weight: 0.14 g (typ.)

Package Dimensions

SSOP16-P-225-0.65B Unit : mm



Weight: 0.07 g (typ.)

RESTRICTIONS ON PRODUCT USE

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- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the “Handling Guide for Semiconductor Devices,” or “TOSHIBA Semiconductor Reliability Handbook” etc..
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