MOTOROLA

4-Bit Parallel Access Shift Register

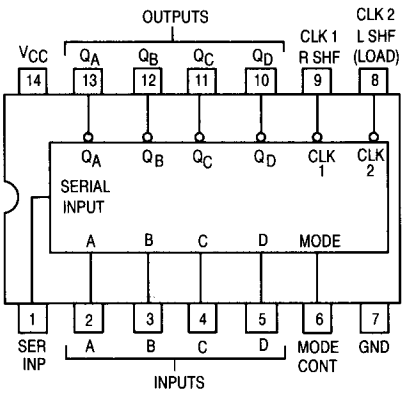
ELECTRICALLY TESTED PER:
MIL-M-38510/30603

The 54LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH to LOW transition of the appropriate clock input.

The 'LS95B is fabricated with the Schottky barrier diode process for high-speed and is completely compatible with all Motorola TTL families.

- Synchronous, Expandable Shift Right
- Synchronous Shift Left Capability
- Synchronous Parallel Load
- Separate Shift and Load Clock Inputs
- Input Clamp Diodes Limit High-Speed Termination Effects

CONNECTION DIAGRAM



Military 54LS95B

AVAILABLE AS:

1) JAN: JM38510/30603BXA
2) SMD: N/A
3) 883: 54LS95B/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
SERIAL	1	1	2	V_{CC}
A IN	2	2	3	V_{CC}
B IN	3	3	4	V_{CC}
C IN	4	4	6	V_{CC}
D IN	5	5	8	V_{CC}
MODE	6	6	9	V_{CC}
GND	7	7	10	GND
CLK_2	8	8	12	CP_1
CLK_1	9	9	13	V_{CC}
Q_D	10	10	14	V_{CC}
Q_C	11	11	16	V_{CC}
Q_B	12	12	18	V_{CC}
Q_A	13	13	19	V_{CC}
V_{CC}	14	14	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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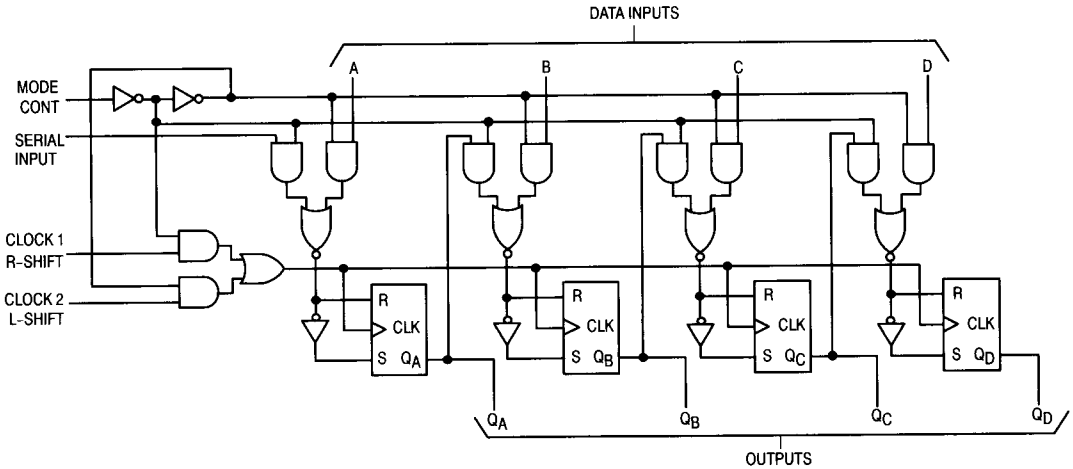
LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The 'LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial (D_S) and four Parallel (P_0-P_3) Data inputs and four Parallel Data outputs (Q_0-Q_3). The serial or parallel mode of operation is controlled by a Mode Control input (S) and two Clock Inputs ($\overline{CP}_1$) and ($\overline{CP}_2$). The serial (right-shift) or parallel data transfers occur synchronous with the HIGH to LOW transition of the selected clock input.

When the Mode Control input (S) is HIGH, $\overline{CP}_2$ is enabled. A HIGH to LOW transition on enabled $\overline{CP}_2$ transfers parallel data from the P_0-P_3 inputs to the Q_0-Q_3 outputs.

When the Mode Control input (S) is LOW, $\overline{CP}_1$ is enabled. A HIGH to LOW transition on enabled $\overline{CP}_1$ transfers the data from Serial input (D_S) to Q_0 and shifts the data in Q_0 to Q_1, Q_1 to Q_2, and Q_2 to Q_3 respectively (right-shift). A left-shift is accomplished by externally connecting Q_3 to P_2, Q_2 to P_1, and Q1 to P_0, and operating the 'LS95B in the parallel mode (S = HIGH).

For normal operation, S should only change states when both Clock inputs are LOW. However, changing S from LOW to HIGH while $\overline{CP}_2$ is HIGH, or changing S from HIGH to LOW while $\overline{CP}_1$ is HIGH and $\overline{CP}_2$ is LOW will not cause any changes on the register outputs.

MODE SELECT — TRUTH TABLE

Operating Mode	Inputs					Outputs			
	S	$\overline{CP}_1$	$\overline{CP}_2$	D_S	P_n	Q_0	Q_1	Q_2	Q_3
Shift	L	↓	X	l	X	L	q_0	q_1	q_2
	L	↓	X	h	X	H	q_0	q_1	q_2
Parallel Load	H	X	↓	X	P_n	P_0	P_1	P_2	P_3
Mode Change	↓	L	L	X	X	No Change			
	↑	L	L	X	X	No Change			
	↓	H	L	X	X	No Change			
	↑	H	L	X	X	Undetermined			
	↓	L	H	X	X	Undetermined			
	↑	L	H	X	X	No Change			
	↓	H	H	X	X	Undetermined			
	↑	H	H	X	X	No Change			

L = LOW Voltage Level
H = HIGH Voltage Level
l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.
P_n = Lower case letters indicates the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

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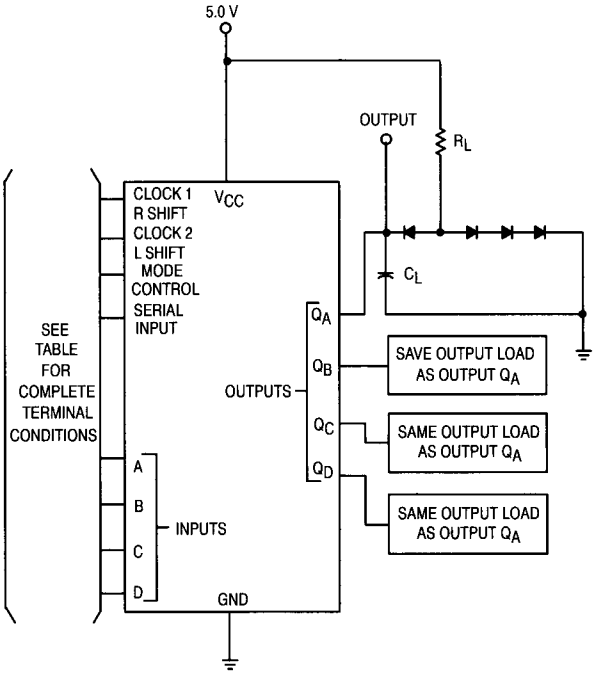
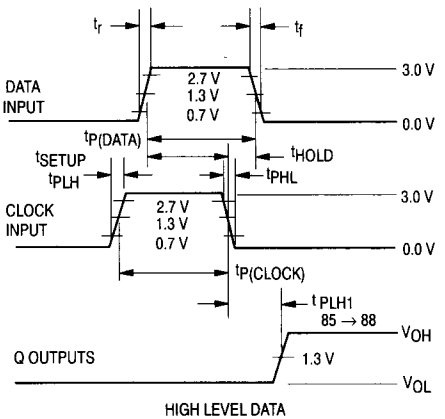
TEST CIRCUIT AND WAVEFORMS

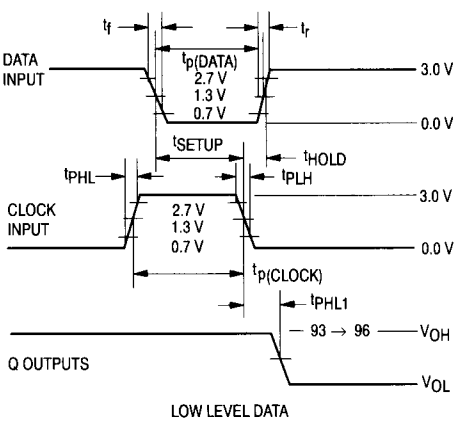


NOTES:

1. The Clock pulse has the following characteristics: $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, $t_p = 0.5$ µs, PRR ≤ 1.0 MHz, $t_{p(clock)} \geq 20$ ns.
2. Serial or data pulse characteristics: $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, $t_{p(SER)}$ or $t_{p(DATA)} = 30$ ns, $t_{setup} = 20$ ns, $t_{HOLD} = 10$ ns.
3. $C_L = 50$ pF ± 10%, including scope probe, wiring and stray capacitance without device in test fixture.
4. $R_L = 2.0$ kΩ ± 5.0%.
5. Voltage measurements are to be made with respect to network ground terminal.
6. All diodes are 1N3064, 1N916 or equivalent.
7. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).
8. Prior to initiating tests, the output shall be placed in the proper state.



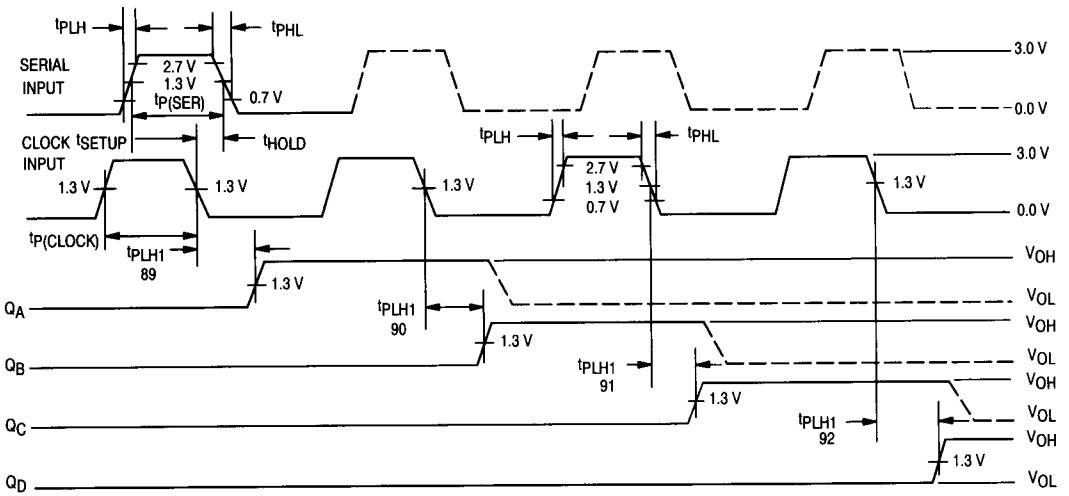
HIGH LEVEL DATA



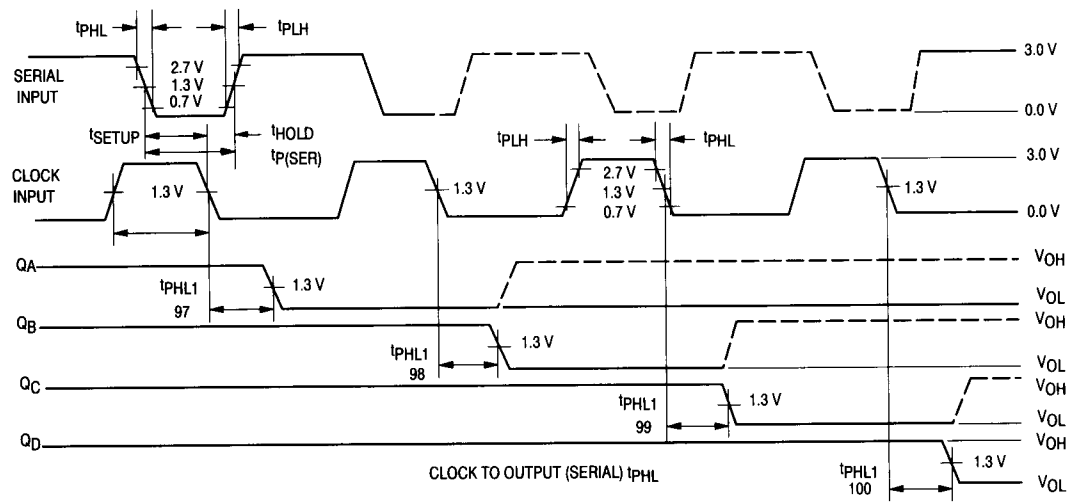
LOW LEVEL DATA

CLOCK TO OUTPUT (PARALLEL)

WAVEFORMS



CLOCK TO OUTPUT (SERIAL) t_{PLH}



CLOCK TO OUTPUT (SERIAL) t_{PHL}

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		− 55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = − 0.4 mA, V_{IN} = GND or 2.0 V, Serial = 2.0 V or open, CLK = GND or (See Note 1), Mode = 0.7 V or 2.0 V.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IN} = 4.5 V or 0.7 V, Mode = 0.7 V or 2.0 V, Serial = GND or open, CLK = GND or (See Note 1).
V_{IC}	Input Clamping Voltage		− 1.5					V	V_{CC} = 4.5 V, I_{IN} = − 18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open, Mode = 4.5 V or GND.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open, Mode = 4.5 V or GND.
I_{IH}	Logical "1" Input Current		40		40		40	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V (Mode), other inputs are open.
I_{IHH}	Logical "1" Input Current		200		200		200	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V (Mode), other inputs are open.
I_{IL}	Logical "0" Input Current	− 0.12	− 0.36	− 0.12	− 0.36	− 0.12	− 0.36	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open, Mode = GND, 4.5 V or 0.4 V.
I_{IL}	Logical "0" Input Current	− 0.12	− 0.36	− 0.12	− 0.36	− 0.12	− 0.36	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V (CLK), other inputs are open, Mode = 4.5 V or GND.
I_{OS}	Short Circuit Output Current	− 15	− 100	− 15	− 100	− 15	− 100	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (Mode), CLK_2 = (See Note 1), CLK_1 = GND, V_{OUT} = GND.
I_{CC}	Power Supply Current Off		21		21		21	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (Mode), other inputs are GND, CLK = (See Note 1).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

NOTE:

1. Apply  2.5 V min/5.5 V max, 0.0 V

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output High-Low	5.0 —	37 32	5.0 —	56 51	5.0 —	56 51	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output Low-High	5.0 —	32 27	5.0 —	48 43	5.0 —	48 43	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
f_{MAX}	Maximum Clock Frequency *See Note 2	22 25		20 25		20 25		MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.

NOTES:

1. The limit specified for C_L = 15 pF is guaranteed but not tested.
2. f_{MAZ} minimum limit specified is the frequency of the clock input pulse. The output frequency shall be one-half of the input frequency. The input frequency on the Serial input shall be one-half of the clock input frequency and the input shall shift such that the input ↑ and ↓ are coincident with the clock ↑. Rise and fall times ≤ 6.0 ns. Input peak voltage 3.0 to 5.0 volts.

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