HARRIS Semiconductor

CD74LCX16652

December 1997

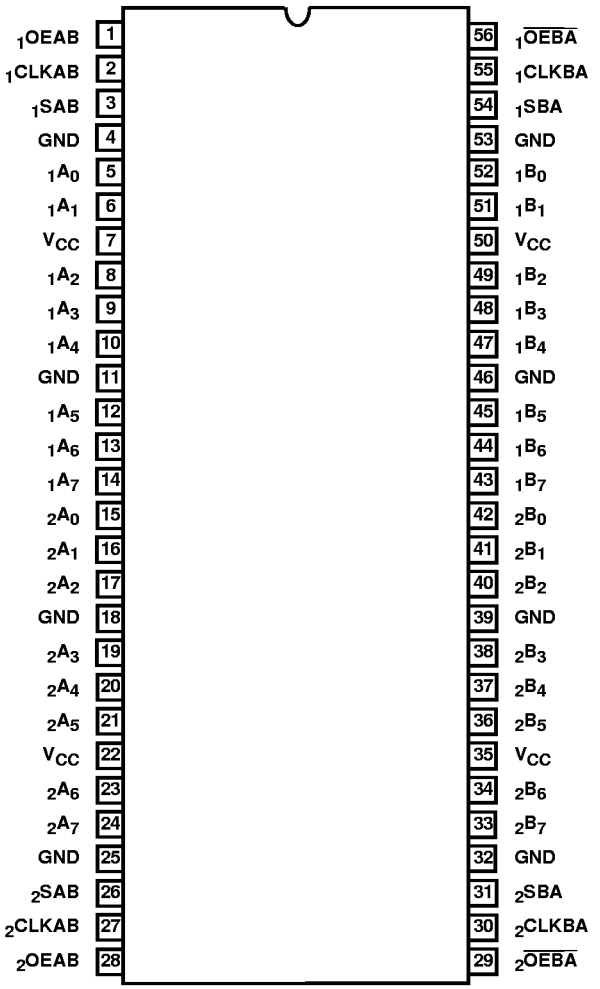
Fast CMOS 16-Bit Registered Transceiver

Features

- **Advanced 0.6 micron CMOS Technology**
- **5V Tolerant Inputs and Outputs**
- **Supports Live Insertion of PCBs**
- **2.0V to 3.6V V_{CC} Supply Range**
- **Balanced 24mA Output Drive**
- **Low Ground Bounce Outputs**
- **ESD Protection Exceeds 2000V, HBM; 200V, MM**
- **Functionally Compatible with FCT3, LVC, LVT, and 74 Series Logic Families**

Pinout

CD74LCX16652 (SSOP, TSSOP)
TOP VIEW



Description

The CD74LCX16652 is a 16-bit registered transceiver organized as two independent 8-bit bus transceivers. It is designed with Three-State D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Each 8-bit transceiver utilizes the enable controls ($_X$OEAB and $_X\overline{OEBA}$) to control the transceiver functions. The Select ($_X$SAB and $_X$SBA) control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The CD74LCX16652 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Ordering Information

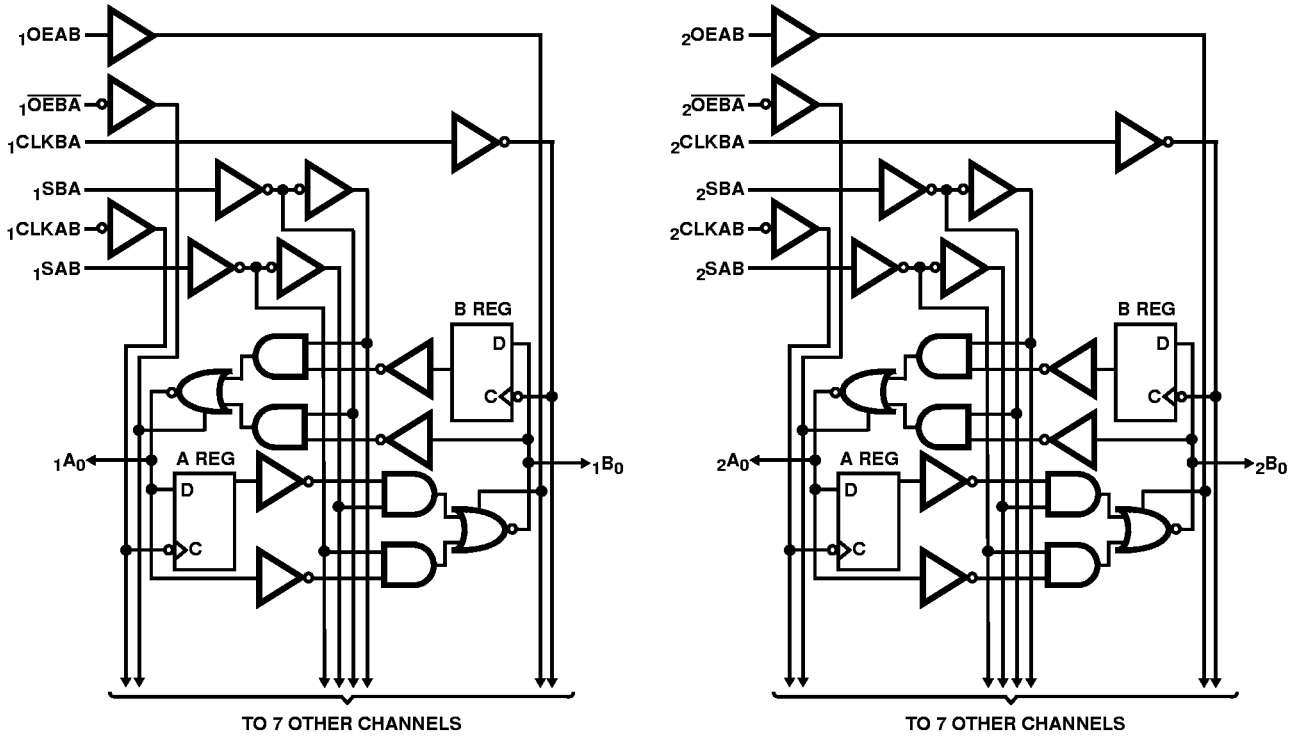
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CD74LCX16652MT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LCX16652SM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4440**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

FUNCTION/OPERATION	INPUTS						DATA I/O	
	$_X$OEAB	$_X\overline{OEBA}$	$_X$CLKAB	$_X$CLKBA	$_X$SAB	$_X$SBA	$_XA_X$	$_XB_X$
Isolation	L	H	H or L	H or L	X	X	Input	Input
Store A and B Data	L	H	↑	↑	X	X		
Store A, Hold B	X	H	↑	H or L	X	X	Input	Unspecified (Note 2)
Store A in Both Registers	H	H	↑	↑	X (Note 3)	X	Input	Output
Hold A, Store B	L	X	H or L	↑	X	X	Unspecified (Note 2)	Input
Store B in Both Registers	L	L	↑	↑	X	X (Note 3)	Output	Input
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	H	H	X	X	L	X	Input	Output
Stored A Data to B Bus	H	H	H or L	X	H	X		
Stored A Data to B Bus and Stored B Data to A Bus	H	L	H or L	H or L	H	H	Output	Output

NOTES:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   ↑= LOW-to-HIGH transition
2. The data output functions may be enabled or disabled by various signals at the xOEAB or $x\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
3. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.

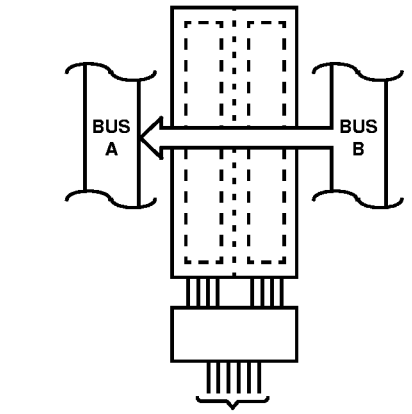


FIGURE 1. REAL-TIME TRANSFER BUS B TO A

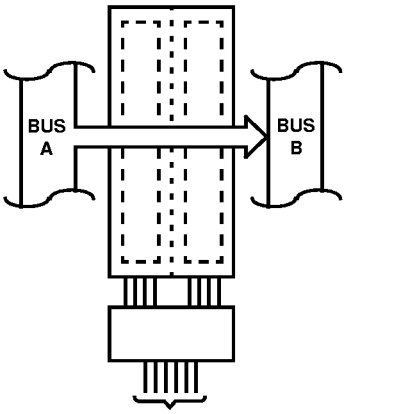


FIGURE 2. REAL-TIME TRANSFER BUS A TO B

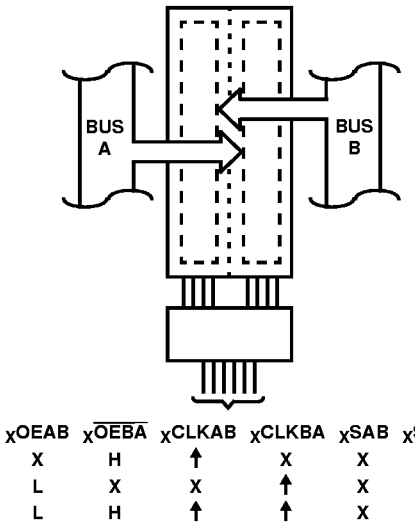


FIGURE 3. STORAGE FROM A AND/OR B

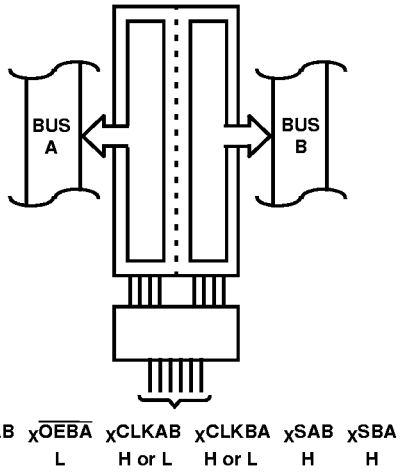


FIGURE 4. TRANSFER STORES DATA TO A AND/OR B

Pin Descriptions

PIN NAME	DESCRIPTION
$_XA_X$	Data Register A Inputs Data Register B Outputs
$_XB_X$	Data Register B Inputs Data Register A Outputs
$_X$CLKAB, $_X$CLKBA	Clock Pulse Inputs
$_X$SAB, $_X$SBA	Output Data Source Select Inputs
$_X$OEAB, $_X\overline{OEBA}$	Output Enable Inputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC
Supply Voltage to Ground Potential
Inputs and V_{CC} Only. . . . . -0.5V to 7.0V
Supply Voltage, V_{CC}
Operating . . . . . 2.0V (Min), 3.6V (Max)
Data Retention . . . . . 1.5V (Min), 3.6V (Max)
Supply Voltage to Ground Potential
Outputs and D/O Only. . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} ($^oC/W$)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, $T_A = -40^oC$ to 85^oC, $V_{CC} = 2.7V$ to $3.6V$							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Output HIGH Voltage	V_{OH}	$V_{CC} = 2.7V$ to $3.6V$	$I_{OH} = -0.1mA$	$V_{CC} - 0.2$	-	-	V
		$V_{CC} = 2.7V$	$I_{OH} = -12mA$	2.2	-	-	V
		$V_{CC} = 3.0V$	$I_{OH} = -18mA$	2.4	-	-	V
			$I_{OH} = -24mA$	2.2	-	-	V
Output LOW Voltage	V_{OL}	$V_{CC} = 2.7V$ to $3.6V$	$I_{OL} = 0.1mA$	-	-	0.2	V
		$V_{CC} = 2.7V$	$I_{OL} = 12mA$	-	-	0.4	V
		$V_{CC} = 3V$	$I_{OL} = 16mA$	-	-	0.4	V
			$I_{OL} = 24mA$	-	-	0.55	V
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, $I_{IN} = -18mA$		-	-0.7	-1.2	V
Input Current	I_I	$V_{CC} = 2.7V$ to $3.6V$	$0 \le V_I \le 5.5V$	-	-	±5	µA
High Impedance Output Current (Three-State)	I_{OZ}	$V_{CC} = 2.7V$ to $3.6V$	$0 \le V_O \le 5.5V$ $V_I = V_{IH}$ or V_{IL}	-	-	±5	µA
Power Down Disable	I_{OFF}	$V_{CC} = 0V$	V_{IN} or $V_{OUT} \le 5.5V$	-	-	10	µA
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	$V_{IN} = V_{CC} - 0.6V$ (Note 7)	-	-	500	µA
CAPACITANCE							
Input Capacitance (Note 8)	C_{IN}	V_{CC} = Open, V_{IN} = 0V or V_{CC}		-	7	-	pF
Output Capacitance (Note 8)	C_{OUT}	$V_{CC} = 3.3V$, V_{IN} = 0V or V_{CC}		-	8	-	pF
Power Dissipation Capacitance (Note 9)	C_{PD}	$V_{CC} = 3.3V$, V_{IN} = 0V or V_{CC}, f = 10MHz		-	20	-	pF

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} = 3.3V ±0.3V		V_{CC} = 2.7V		UNITS
			MIN	MAX	MIN	MAX	
Propagation Delay, Bus to Bus	t_{PHL}, t_{PLH}	C_L = 50pF, R_L = 500Ω	1.5	5.7	1.5	6.2	ns
Output Enable Time, xOEAB or xOEBA to Bus	t_{PZL}, t_{PZH}		1.5	7.0	1.5	8.0	ns
Output Disable Time, xOEAB or xOEBA to Bus	t_{PHZ}, t_{PLZ}		1.5	6.5	1.5	7.0	ns
Propagation Delay, Clock to Bus	t_{PHL}, t_{PLH}		1.5	6.2	1.5	7.0	ns
Propagation Delay, .xSBA to sSAB to Bus	t_{PLH}, t_{PHL}		1.5	6.5	1.5	7.0	ns
Setup Time, HIGH or LOW, Bus to Clock	t_{SU}		2.5	-	2.5	-	ns
Hold Time HIGH or LOW, Bus to Clock	t_H		1.5	-	1.5	-	ns
Clock Pulse Width, HIGH or LOW (Note 12)	t_W		3.0	-	3.0	-	ns
Output Skew (Note 13)	$t_{SK(O)}$		-	1.0	-	-	ns

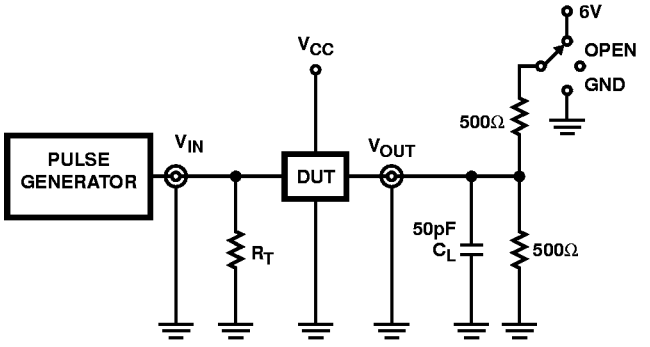
Dynamic Switching Characteristics $T_A = 25^oC$

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	TYP	UNITS
Dynamic LOW Peak Voltage	V_{OLP}	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V	0.8	V
Dynamic LOW Valley Voltage	V_{OLV}	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V	0.8	V

NOTES:

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
6. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
7. Per TTL driven input; all other inputs at V_{CC} or GND.
8. This parameter is determined by device characterization but is not production tested.
9. C_{PD} determines the no-load dynamic power consumption per latch. It is obtained by the following relationship: P_D (total power per latch) = V_{CC}^2 f_i (C_{PD} + C_L) where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply range.
10. See test circuit and waveforms.
11. Minimum limits are guaranteed but not tested on Propagation Delays.
12. This parameter is guaranteed but not production tested.
13. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
14. Measured with n-1 outputs switching from High-to-Low or Low-to-High. The remaining output is measured in the LOW state.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

15. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 5. TEST CIRCUIT

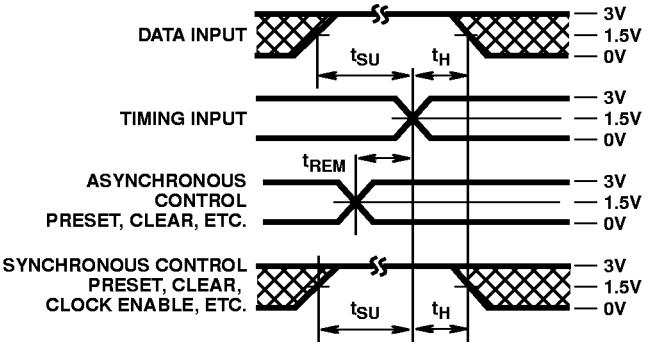


FIGURE 6. SETUP, HOLD, AND RELEASE TIMING

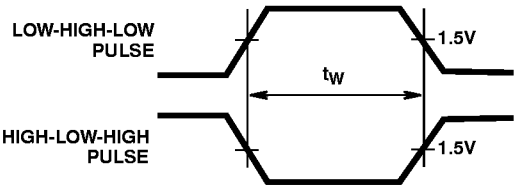


FIGURE 7. PULSE WIDTH

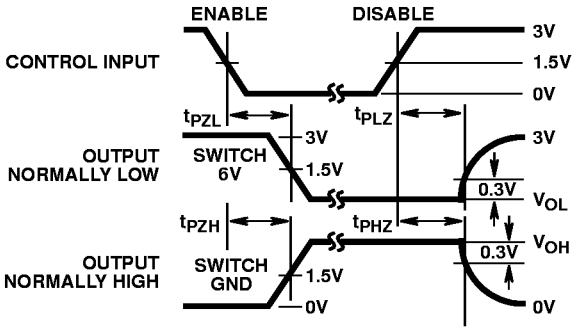


FIGURE 8. ENABLE AND DISABLE TIMING

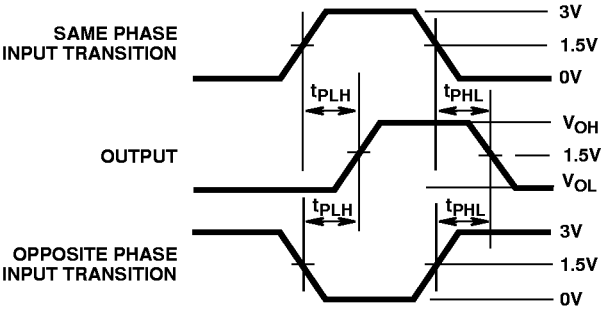
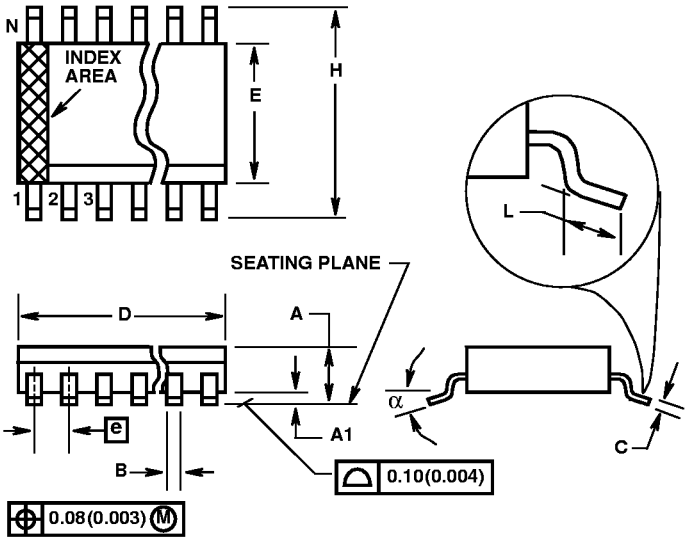


FIGURE 9. PROPAGATION DELAY

Thin Shrink Small Outline Plastic Packages (TSSOP)



M56.240-P

56 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

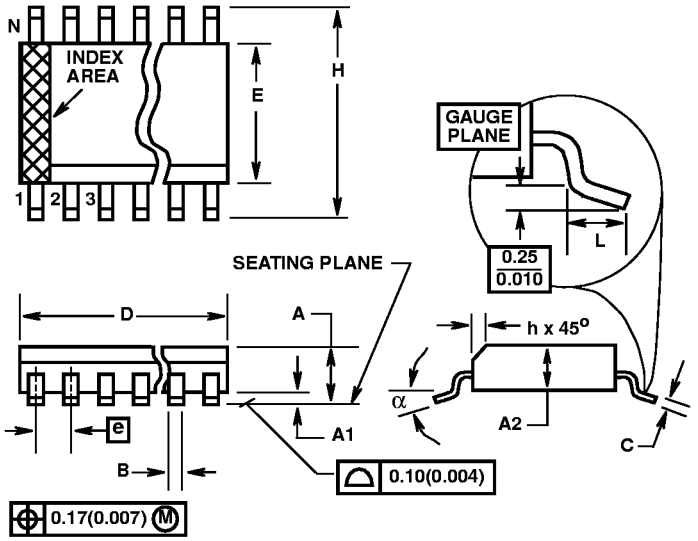
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.041	0.047	1.05	1.20	-
A1	0.002	0.006	0.05	0.15	-
B	0.007	0.010	0.178	0.254	-
C	0.004	0.008	0.102	0.203	-
D	0.547	0.555	13.90	14.09	1
E	0.236	0.244	6.00	6.19	2
e	0.0197 BSC		0.50 BSC		-
H	0.307	0.330	7.80	8.38	-
L	0.020	0.030	0.51	0.76	3
N	56		56		4
α	0^o	8^o	0^o	8^o	-

Rev. 0 6/96

NOTES:

1. Dimension “D” does not include mold flash, protrusions or gate burrs.
2. Dimension “E” does not include interlead flash or protrusions.
3. “L” is the length of terminal for soldering to a substrate.
4. “N” is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

Shrink Small Outline Plastic Packages (SSOP)



M56.300-P

56 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.096	0.108	2.44	2.74	-
A1	0.008	0.016	0.20	0.41	-
A2	0.088	0.092	2.24	2.34	-
B	0.008	0.0135	0.20	0.34	-
C	0.005	0.010	0.13	0.25	-
D	0.720	0.730	18.29	18.54	2
E	0.291	0.299	7.39	7.59	3
e	0.025 BSC		0.635 BSC		-
H	0.395	0.415	10.03	10.54	-
h	0.015	0.025	0.381	0.635	-
L	0.020	0.040	0.51	1.01	4
N	56		56		5
α	0^o	8^o	0^o	8^o	-

Rev. 0 5/96

NOTES:

1. These package dimensions are within allowable dimensions of JECEC MO-118-AB, Issue B.
2. Dimension “D” does not include mold flash, protrusions or gate burrs.
3. Dimension “E” does not include interlead flash or protrusions.
4. “L” is the length of terminal for soldering to a substrate.
5. “N” is the number of terminal positions.
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