# Presettable synchronous 4-bit binary counter; asynchronous reset

# 74LV161

## FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between $V_{CC}$ = 2.7 V and $V_{CC}$ = 3.6 V
- Typical $V_{OLP}$ (output ground bounce) < 0.8 V at $V_{CC}$ = 3.3 V, $T_{amb}$ = 25°C
- Typical $V_{OHV}$ (output $V_{OH}$ undershoot) > 2 V at $V_{CC}$ = 3.3 V, $T_{amb}$ = 25°C
- Asynchronous reset
- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Output capability: standard
- $I_{CC}$ category: MSI

## DESCRIPTION

The 74LV161 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT161.

The 74LV161 is a synchronous presettable binary counter which features an internal look-head carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP). The outputs ($Q_0$ to $Q_3$) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs ($D_0$ to $D_3$) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET). A low level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops ($Q_0$ to $Q_3$) to LOW level regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of $Q_0$. This pulse can be used to enable the next cascading stage. The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{max} = \frac{1}{t_{p(max)}\ (CP\ to\ TC) + t_{su}(CEP\ to\ CP)}$$

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25°C; $t_r = t_f \leq 2.5$ ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation delay<br>CP to $Q_n$<br>CP to TC<br>$\overline{MR}$ to $Q_n$<br>$\overline{MR}$ to TC<br>CET to TC | $C_L$ = 15 pF;<br>$V_{CC}$ = 3.3 V | <br>15<br>18<br>15<br>17<br>9 | ns |
| $f_{max}$ | Maximum clock frequency | | 77 | MHz |
| $C_I$ | Input capacitance | | 3.5 | pF |
| $C_{PD}$ | Power dissipation capacitance per gate | $V_I$ = GND to $V_{CC}$[1] | 25 | pF |

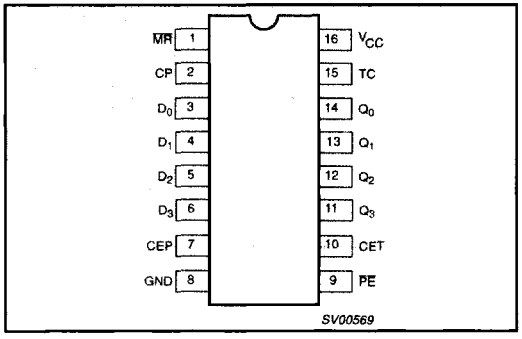
**NOTES:**

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   $f_i$ = input frequency in MHz; $C_L$ = output load capacitance in pF;
   $f_o$ = output frequency in MHz; $V_{CC}$ = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

## ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | PKG. DWG. # |
|---|---|---|---|---|
| 16-Pin Plastic DIL | −40°C to +125°C | 74LV161 N | 74LV161 N | SOT38-4 |
| 16-Pin Plastic SO | −40°C to +125°C | 74LV161 D | 74LV161 D | SOT109-1 |
| 16-Pin Plastic SSOP Type II | −40°C to +125°C | 74LV161 DB | 74LV161 DB | SOT338-1 |
| 16-Pin Plastic TSSOP Type I | −40°C to +125°C | 74LV161 PW | 74LV161PW DH | SOT403-1 |

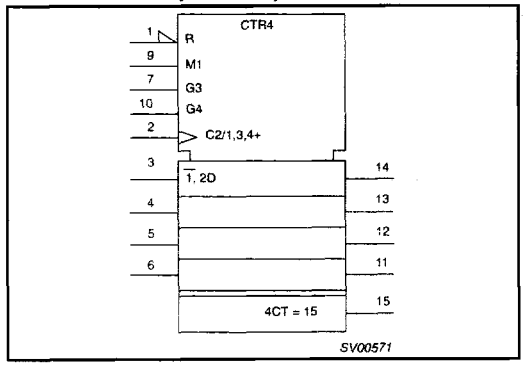
## PIN CONFIGURATION



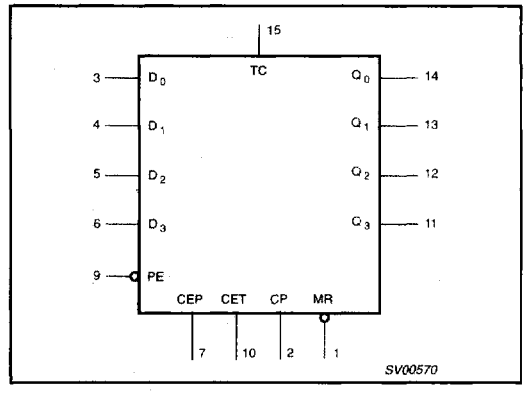

## PIN DESCRIPTION

| PIN NUMBER | SYMBOL | FUNCTION |
|---|---|---|
| 1 | $\overline{MR}$ | Asynchronous master reset (active LOW) |
| 2 | CP | Clock input (LOW-to-HIGH, edge-triggered) |
| 3, 4, 5, 6 | $D_0$ to $D_3$ | Data inputs |
| 7 | CEP | Count enable inputs |
| 8 | GND | Ground (0 V) |
| 9 | $\overline{PE}$ | Parallel enable input (active LOW) |
| 10 | CET | Count enable carry input |
| 14, 13, 12, 11 | $Q_0$ to $Q_3$ | Flip-flop outputs |
| 15 | TC | Terminal count output |
| 16 | $V_{CC}$ | Positive supply voltage |

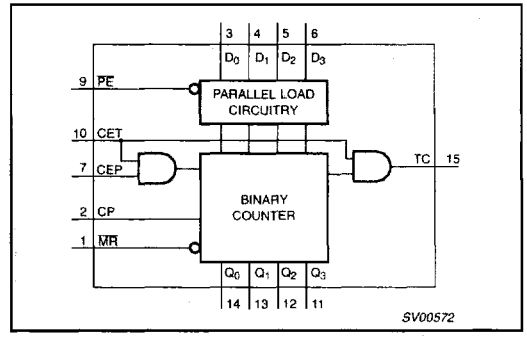
## LOGIC SYMBOL (IEEE/IEC)




## LOGIC SYMBOL




## FUNCTIONAL DIAGRAM



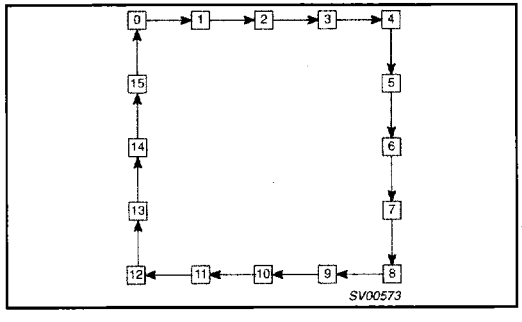
## FUNCTION TABLE

| OPERATING MODES | INPUTS | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|
| | $\overline{MR}$ | CP | CEP | CET | $\overline{PE}$ | $D_n$ | $Q_n$ | TC |
| Reset (clear) | L | X | X | X | X | X | L | L |
| Parallel load | H | ↑ | X | X | l | l | L | L |
| | H | ↑ | X | X | l | h | H | * |
| Count | H | ↑ | h | h | h | X | Count | * |
| Hold (do nothing) | H | X | l | X | h | X | $q_n$ | * |
| | H | X | X | l | h | X | $q_n$ | L |

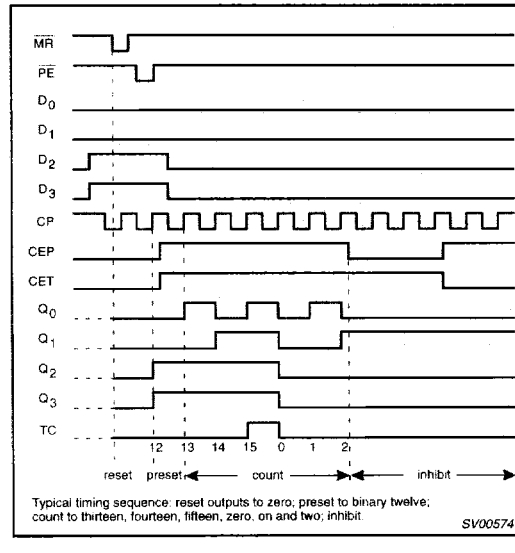
**NOTES:**

* = The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH)
H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level level one set-up time prior to the LOW-to-HIGH clock transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition
X = don't care
↑ = LOW-to-HIGH clock transition

## STATE DIAGRAM

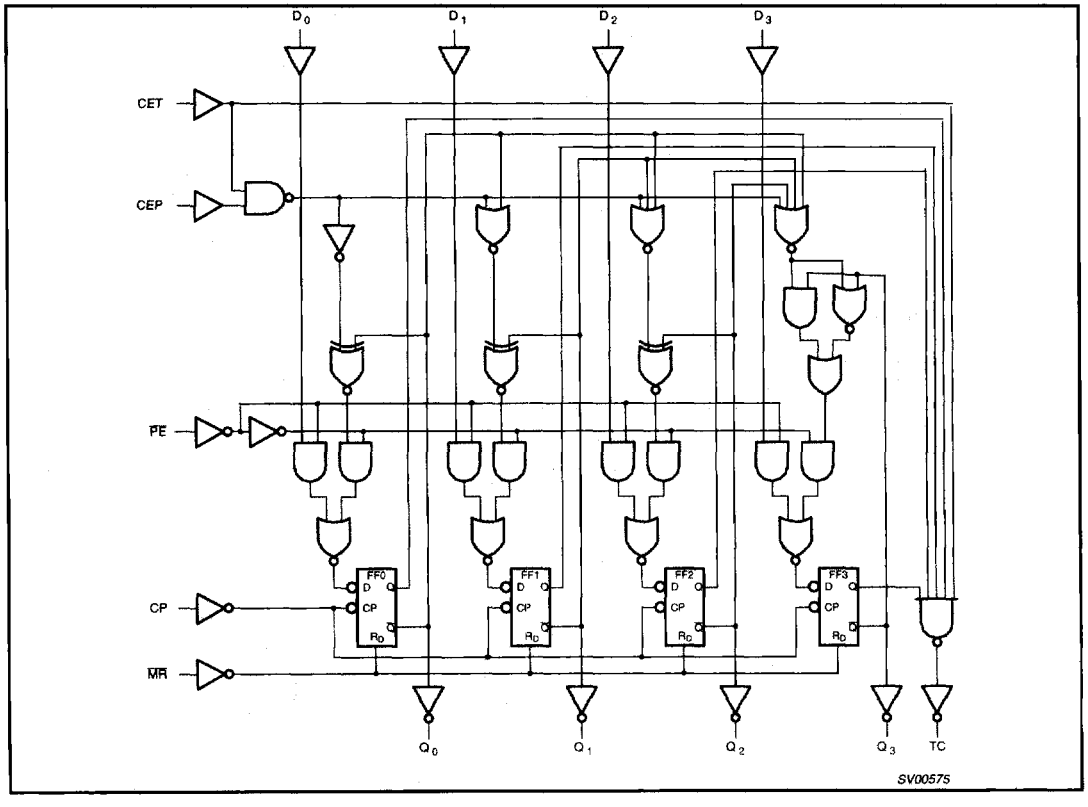



## TYPICAL TIMING SEQUENCE




Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, on and two; inhibit.

## LOGIC DIAGRAM



## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | See Note 1 | 1.0 | 3.3 | 3.6 | V |
| $V_I$ | Input voltage | | 0 | – | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | – | $V_{CC}$ | V |
| $T_{amb}$ | Operating ambient temperature range in free air | See DC and AC characteristics | –40<br>–40 | | +85<br>+125 | °C |
| $t_r$, $t_f$ | Input rise and fall times | $V_{CC}$ = 1.0V to 2.0V<br>$V_{CC}$ = 2.0V to 2.7V<br>$V_{CC}$ = 2.7V to 3.6V | –<br>–<br>– | –<br>–<br>– | 500<br>200<br>100 | ns/V |

**NOTE:**
1. The LV is guaranteed to function down to $V_{CC}$ = 1.0V (input levels GND or $V_{CC}$); DC characteristics are guaranteed from $V_{CC}$ = 1.2V to $V_{CC}$ = 3.6V.

## ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | | –0.5 to +4.6 | V |
| $\pm I_{IK}$ | DC input diode current | $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$ | 20 | mA |
| $\pm I_{OK}$ | DC output diode current | $V_O < -0.5$ or $V_O > V_{CC} + 0.5V$ | 50 | mA |
| $\pm I_O$ | DC output source or sink current<br>– standard outputs | $-0.5V < V_O < V_{CC} + 0.5V$ | 25 | mA |
| $\pm I_{GND}$,<br>$\pm I_{CC}$ | DC $V_{CC}$ or GND current for types with<br>– standard outputs | | 50 | mA |
| $T_{stg}$ | Storage temperature range | | –65 to +150 | °C |
| $P_{TOT}$ | Power dissipation per package<br>– plastic DIL<br>– plastic mini-pack (SO)<br>– plastic shrink mini-pack (SSOP and TSSOP) | for temperature range: –40 to +125°C<br>above +70°C derate linearly with 12 mW/K<br>above +70°C derate linearly with 8 mW/K<br>above +60°C derate linearly with 5.5 mW/K | <br>750<br>500<br>400 | mW |

**NOTES:**
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | -40°C to +85°C | | | -40°C to +125°C | | |
| | | | MIN | TYP[1] | MAX | MIN | MAX | |
| $V_{IH}$ | HIGH level input voltage | $V_{CC}$ = 1.2 V | 0.9 | | | 0.9 | | V |
| | | $V_{CC}$ = 2.0 V | 1.4 | | | 1.4 | | |
| | | $V_{CC}$ = 2.7 to 3.6 V | 2.0 | | | 2.0 | | |
| $V_{IL}$ | LOW level input voltage | $V_{CC}$ = 1.2 V | | | 0.3 | | 0.3 | V |
| | | $V_{CC}$ = 2.0 V | | | 0.6 | | 0.6 | |
| | | $V_{CC}$ = 2.7 to 3.6 V | | | 0.8 | | 0.8 | |
| $V_{OH}$ | HIGH level output voltage; all outputs | $V_{CC}$ = 1.2 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $-I_O$ = 100μA | | 1.2 | | | | V |
| | | $V_{CC}$ = 2.0 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $-I_O$ = 100μA | 1.8 | 2.0 | | 1.8 | | |
| | | $V_{CC}$ = 2.7 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $-I_O$ = 100μA | 2.5 | 2.7 | | 2.5 | | |
| | | $V_{CC}$ = 3.0 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $-I_O$ = 100μA | 2.8 | 3.0 | | 2.8 | | |
| $V_{OH}$ | HIGH level output voltage; STANDARD outputs | $V_{CC}$ = 3.0 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $-I_O$ = 6mA | 2.40 | 2.82 | | 2.20 | | V |
| $V_{OL}$ | LOW level output voltage; all outputs | $V_{CC}$ = 1.2 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = 100μA | | 0 | | | | V |
| | | $V_{CC}$ = 2.0 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = 100μA | | 0 | 0.2 | | 0.2 | |
| | | $V_{CC}$ = 2.7 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = 100μA | | 0 | 0.2 | | 0.2 | |
| | | $V_{CC}$ = 3.0 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = 100μA | | 0 | 0.2 | | 0.2 | |
| $V_{OL}$ | LOW level output voltage; STANDARD outputs | $V_{CC}$ = 3.0 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = 6mA | | 0.25 | 0.40 | | 0.50 | V |
| $I_I$ | Input leakage current | $V_{CC}$ = 3.6 V; $V_I$ = $V_{CC}$ or GND | | | 1.0 | | 1.0 | μA |
| $I_{CC}$ | Quiescent supply current; MSI | $V_{CC}$ = 3.6 V; $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 | | | 20.0 | | 160 | μA |
| $\Delta I_{CC}$ | Additional quiescent supply current per input | $V_{CC}$ = 2.7 V to 3.6 V; $V_I$ = $V_{CC}$ – 0.6 V | | | 500 | | 850 | μA |

**NOTE:**

1. All typical values are measured at $T_{amb}$ = 25°C.

## AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

| SYMBOL | PARAMETER | WAVEFORM | CONDITION | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | −40 to +85 °C | | | −40 to +125 °C | | |
| | | | $V_{CC}$(V) | MIN | TYP[1] | MAX | MIN | MAX | |
| $t_{PHL}/t_{PLH}$ | Propagation delay CP to $Q_n$ | Figures 1, 6 | 1.2 | | 95 | | | | ns |
| | | | 2.0 | | 32 | 61 | | 75 | |
| | | | 2.7 | | 24 | 45 | | 55 | |
| | | | 3.0 to 3.6 | | 18[2] | 36 | | 44 | |
| $t_{PHL}/t_{PLH}$ | Propagation delay CP to TC | Figures 1, 6 | 1.2 | | 115 | | | | ns |
| | | | 2.0 | | 39 | 75 | | 90 | |
| | | | 2.7 | | 29 | 55 | | 66 | |
| | | | 3.0 to 3.6 | | 22[2] | 44 | | 53 | |
| $t_{PHL}/t_{PLH}$ | Propagation delay $\overline{MR}$ to $Q_n$ | Figures 2, 6 | 1.2 | | 95 | | | | ns |
| | | | 2.0 | | 32 | 61 | | 75 | |
| | | | 2.7 | | 24 | 45 | | 55 | |
| | | | 3.0 to 3.6 | | 18[2] | 36 | | 44 | |
| $t_{PHL}/t_{PLH}$ | Propagation delay $\overline{MR}$ to TC | Figures 2, 6 | 1.2 | | 105 | | | | ns |
| | | | 2.0 | | 36 | 68 | | 82 | |
| | | | 2.7 | | 26 | 50 | | 60 | |
| | | | 3.0 to 3.6 | | 20[2] | 40 | | 48 | |
| $t_{PHL}/t_{PLH}$ | Propagation delay CET to TC | Figures 3, 6 | 1.2 | | 55 | | | | ns |
| | | | 2.0 | | 19 | 36 | | 44 | |
| | | | 2.7 | | 14 | 26 | | 33 | |
| | | | 3.0 to 3.6 | | 10[2] | 21 | | 26 | |
| $t_w$ | Clock pulse width HIGH or LOW | Figures 1, 6 | 2.0 | 34 | 10 | | 41 | | ns |
| | | | 2.7 | 25 | 8 | | 30 | | |
| | | | 3.0 to 3.6 | 20 | 6[2] | | 24 | | |
| $t_w$ | Master reset width; LOW | Figures 2, 6 | 2.0 | 34 | 14 | | 41 | | ns |
| | | | 2.7 | 25 | 10 | | 30 | | |
| | | | 3.0 to 3.6 | 20 | 8[2] | | 24 | | |
| $t_{rem}$ | Removal time $\overline{MR}$ to CP | Figures 2, 6 | 1.2 | | 25 | | | | ns |
| | | | 2.0 | 22 | 9 | | 26 | | |
| | | | 2.7 | 16 | 6 | | 19 | | |
| | | | 3.0 to 3.6 | 13 | 5[2] | | 15 | | |
| $t_{su}$ | Set-up time $D_n$ to CP | Figures 4, 6 | 1.2 | | 25 | | | | ns |
| | | | 2.0 | 22 | 9 | | 26 | | |
| | | | 2.7 | 16 | 6 | | 19 | | |
| | | | 3.0 to 3.6 | 13 | 5[2] | | 15 | | |
| $t_{su}$ | Set-up time $\overline{PE}$ to CP | Figures 4, 6 | 1.2 | | 30 | | | | ns |
| | | | 2.0 | 22 | 10 | | 26 | | |
| | | | 2.7 | 16 | 8 | | 19 | | |
| | | | 3.0 to 3.6 | 13 | 6[2] | | 15 | | |
| $t_{su}$ | Set-up time CEP, CET to CP | Figures 5, 6 | 1.2 | | 30 | | | | ns |
| | | | 2.0 | 22 | 10 | | 26 | | |
| | | | 2.7 | 16 | 8 | | 19 | | |
| | | | 3.0 to 3.6 | 13 | 6[2] | | 15 | | |

## AC ELECTRICAL CHARACTERISTICS (Continued)

| SYMBOL | PARAMETER | WAVEFORM | CONDITION | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | −40 to +85 °C | | | −40 to +125 °C | | |
| | | | $V_{CC}$(V) | MIN | TYP[1] | MAX | MIN | MAX | |
| $t_h$ | Hold time $D_n$, $\overline{PE}$, CEP, CET to CP | Figures 4 – 6 | 1.2 | | −35 | | | | ns |
| | | | 2.0 | 0 | −12 | | 0 | | |
| | | | 2.7 | 0 | −9 | | 0 | | |
| | | | 3.0 to 3.6 | 0 | −7[2] | | 0 | | |
| $f_{max}$ | Maximum clock pulse frequency | Figures 1, 6 | 2.0 | 14 | 40 | | 12 | | MHz |
| | | | 2.7 | 19 | 58 | | 16 | | |
| | | | 3.0 to 3.6 | 24 | 70 | | 20 | | |

**NOTES:**
1. Unless otherwise stated, all typical values are measured at $T_{amb}$ = 25°C
2. Typical values are measured at $V_{CC}$ = 3.3 V.

## AC WAVEFORMS

$V_M$ = 1.5 V at $V_{CC} \geq$ 2.7 V;
$V_M$ = 0.5 × $V_{CC}$ at $V_{CC}$ < 2.7 V;
$V_{OL}$ and $V_{OH}$ are the typical output voltage drop that occur with the output load.

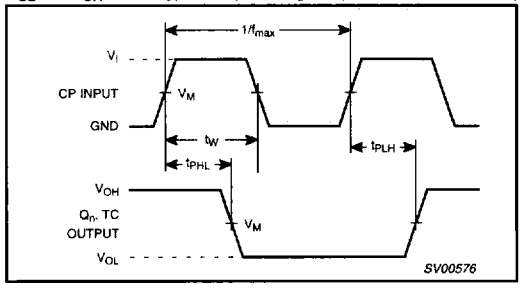



**Figure 1. Clock (CP) to outputs ($Q_n$, TC) propagation delays, the clock pulse width and the maximum clock frequency.**

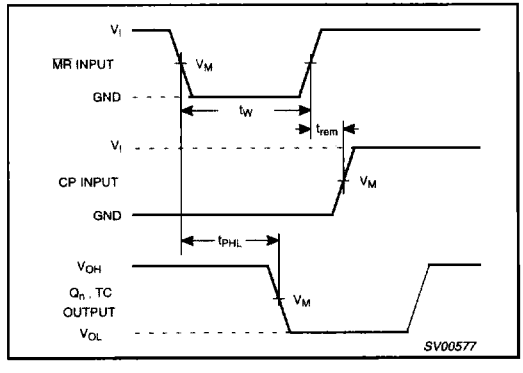



**Figure 2. Master reset ($\overline{MR}$) pulse width, the master reset to output ($Q_n$, TC) propagation delays and the master reset to clock (CP) removal times.**

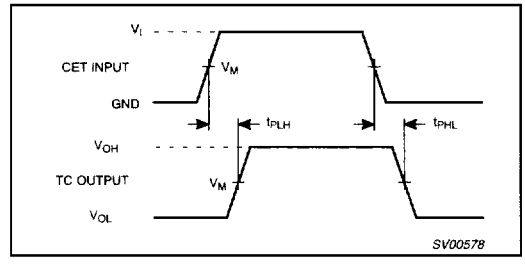



**Figure 3. Input (CET) to output (TC) propagation delays.**

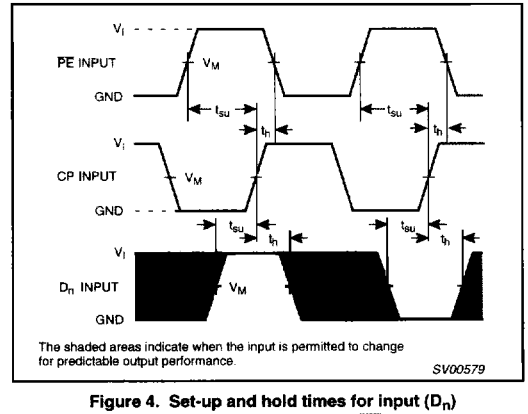



**Figure 4. Set-up and hold times for input ($D_n$) and parallel enable input ($\overline{PE}$).**

## AC WAVEFORMS (Continued)

$V_M$ = 1.5 V at $V_{CC} \geq$ 2.7 V;
$V_M = 0.5 \times V_{CC}$ at $V_{CC} <$ 2.7 V;
$V_{OL}$ and $V_{OH}$ are the typical output voltage drop that occur with the output load.

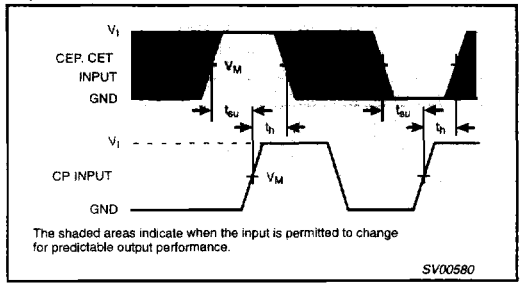



**Figure 5. CEP and CET set-up and hold times.**

## TEST CIRCUIT

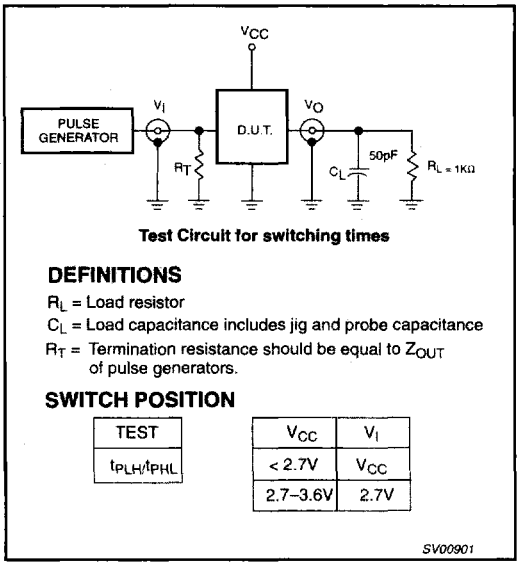



**Figure 6. Load circuitry for switching times.**