



HIGH PERFORMANCE CMOS BUS INTERFACE REGISTER

IDT54/74FCT823A/B/C

FEATURES:

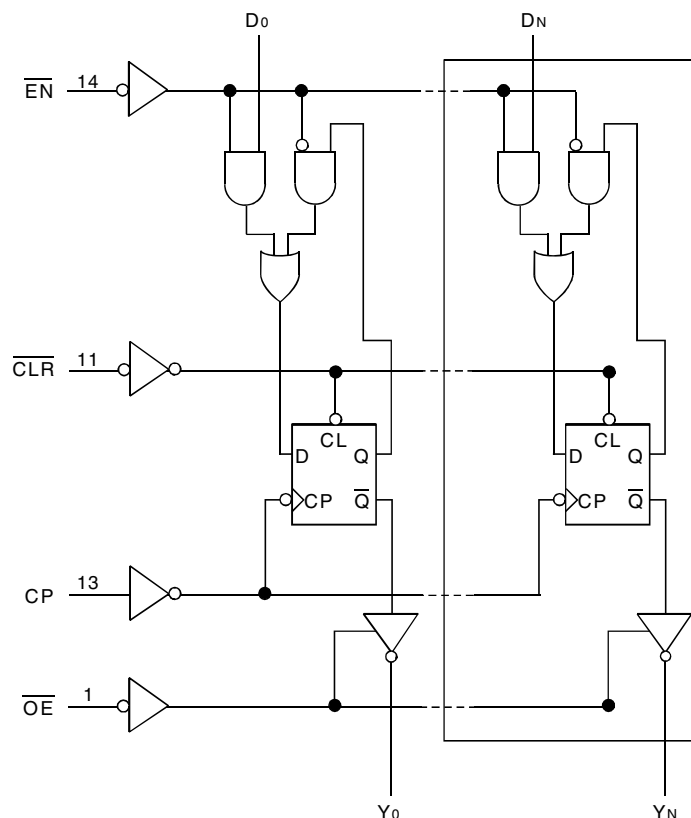
- Equivalent to AMD's Am29823 bipolar registers in pinout/ function, speed, and output drive over full temperature and voltage supply extremes
- IDT54/74FCT823A equivalent to FAST™ speed
- IDT54FCT823B 25% faster than FAST
- IDT74FCT823C 40% faster than FAST
- Buffered common Clock Enable (\overline{EN}) and Asynchronous Clear Input (\overline{CLR})
- IOL = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output compatibility
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5 μ A max.)
- Military product compliant to MIL-STD-883, Class B
- Available in the following packages:
 - Commercial: SOIC
 - Military: CERDIP, LCC

DESCRIPTION:

The FCT823 series is built using an advanced dual metal CMOS technology. The FCT823 bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The FCT823 is a 9-bit wide buffered register with Clock Enable (\overline{EN}) and Clear (\overline{CLR}) – ideal for parity bus interfacing in high-performance microprogrammed systems.

The FCT823 high-performance interface family is designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

FUNCTIONAL BLOCK DIAGRAM

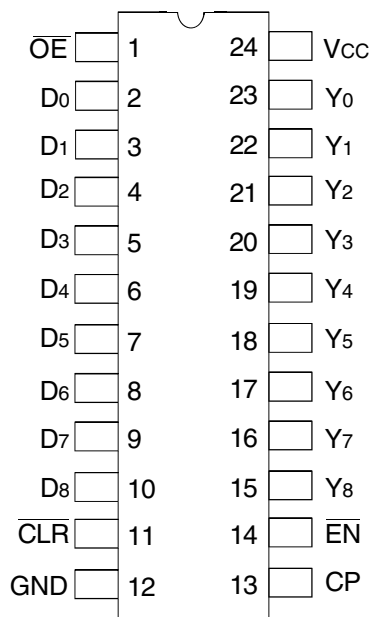


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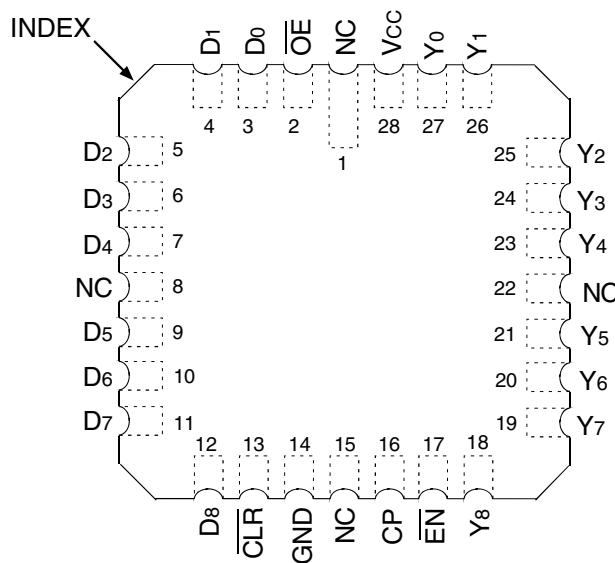
MILITARY AND COMMERCIAL TEMPERATURE RANGES

JUNE 2002

PIN CONFIGURATION



CERDIP/ SOIC
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Rating | Commercial | Military | Unit |
|----------------------------------|--------------------------------------|-------------------------|-------------------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +7 | -0.5 to +7 | V |
| V _{TERM} ⁽³⁾ | Terminal Voltage with Respect to GND | -0.5 to V _{CC} | -0.5 to V _{CC} | V |
| T _A | Operating Temperature | 0 to +70 | -55 to +125 | °C |
| T _{BIAS} | Temperature under BIAS | -55 to +125 | -65 to +135 | °C |
| T _{STG} | Storage Temperature | -55 to +125 | -65 to +150 | °C |
| P _T | Power Dissipation | 0.5 | 0.5 | W |
| I _{OUT} | DC Output Current | 120 | 120 | mA |

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Input and V_{CC} terminals only.
- Output and I/O terminals only.

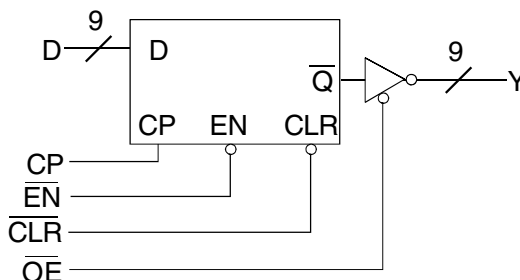
CAPACITANCE (T_A = +25°C, F = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 6 | 10 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 8 | 12 | pF |

NOTE:

- This parameter is measured at characterization but not tested.

LOGIC SYMBOL



PIN DESCRIPTION

| Pin Name | I/O | Description |
|----------------|-----|---|
| D _x | I | D flip-flop data inputs |
| CLR | I | For both inverting and non-inverting registers, when the clear input is LOW and OE is LOW, the Q _x outputs are LOW. When the clear input is HIGH, data can be entered into the register. |
| CP | I | Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition. |
| Y _x | O | Register 3-state outputs |
| EN | I | Clock Enable. When the clock enable is LOW, data on the D _i input is transferred to the Q _i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q _i outputs do not change state, regardless of the data or clock input transitions. |
| OE | I | Output Control. When the OE input is HIGH, the Y _x outputs are in the high impedance state. When the OE input is LOW, the TRUE register data is present at the Y _x outputs. |

FUNCTION TABLE⁽¹⁾

| Inputs | | | | | Internal/Outputs | | Function |
|--------|-----|----|----|----|------------------|----|----------|
| OE | CLR | EN | Dx | CP | Qx | Yx | |
| H | H | L | L | ↑ | L | Z | High Z |
| H | H | L | H | ↑ | H | Z | |
| H | L | X | X | X | L | Z | Clear |
| L | L | X | X | X | L | L | |
| H | H | H | X | X | NC | Z | Hold |
| L | H | H | X | X | NC | NC | |
| H | H | L | L | ↑ | L | Z | Load |
| H | H | L | H | ↑ | H | Z | |
| L | H | L | L | ↑ | L | L | |
| L | H | L | H | ↑ | H | H | |

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH Transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Commercial: $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = 5.0V \pm 5\%$, Military: $T_A = -55^\circ C$ to $+125^\circ C$, $V_{CC} = 5.0V \pm 10\%$

| Symbol | Parameter | Test Conditions ⁽¹⁾ | Min. | Typ. ⁽²⁾ | Max. | Unit | |
|-----------|--|---|------------------------|---------------------|----------|--------------------|-------------------------|
| V_{IH} | Input HIGH Level | Guaranteed Logic HIGH Level | 2 | — | — | V | |
| V_{IL} | Input LOW Level | Guaranteed Logic LOW Level | — | — | 0.8 | V | |
| I_{IH} | Input HIGH Current | $V_{CC} = \text{Max.}$ | $V_I = V_{CC}$ | — | — | 5 | μA |
| I_{IL} | Input LOW Current | | $V_I = 2.7V$ | — | — | 5 ⁽⁴⁾ | |
| | | | $V_I = 0.5V$ | — | — | -5 ⁽⁴⁾ | |
| I_{OZH} | Off State (High Impedance) Output Current | $V_{CC} = \text{Max.}$ | $V_O = V_{CC}$ | — | — | 10 | μA |
| | | | $V_O = 2.7V$ | — | — | 10 ⁽⁴⁾ | |
| | | | $V_O = 0.5V$ | — | — | -10 ⁽⁴⁾ | |
| | | | $V_O = GND$ | — | — | -10 | |
| V_{IK} | Clamp Diode Voltage | $V_{CC} = \text{Min.}, I_{IN} = -18mA$ | — | -0.7 | -1.2 | V | |
| I_{OS} | Short Circuit Current | $V_{CC} = \text{Max.}, V_O = GND$ ⁽³⁾ | -75 | -120 | — | mA | |
| V_{OH} | Output HIGH Voltage | $V_{CC} = 3V, V_{IN} = V_{LC}$ or $V_{HC}, I_{OH} = -32\mu A$ | V_{HC} | V_{CC} | — | V | |
| | | $V_{CC} = \text{Min}$ | $I_{OH} = -300\mu A$ | V_{HC} | V_{CC} | | |
| | | $V_{IN} = V_{IH}$ or V_{IL} | $I_{OH} = -15mA$ MIL | 2.4 | 4.3 | | — |
| | | | $I_{OH} = -24mA$ COM'L | 2.4 | 4.3 | | — |
| V_{OL} | Output LOW Voltage | $V_{CC} = 3V, V_{IN} = V_{LC}$ or $V_{HC}, I_{OL} = 300\mu A$ | — | GND | V_{LC} | V | |
| | | $V_{CC} = \text{Min}$ | $I_{OL} = 300\mu A$ | — | GND | | V_{LC} ⁽⁴⁾ |
| | | $V_{IN} = V_{IH}$ or V_{IL} | $I_{OL} = 32mA$ MIL | — | 0.3 | | 0.5 |
| | | | $I_{OL} = 48mA$ COM'L | — | 0.3 | | 0.5 |

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient and maximum loading.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|------------------|---|--|---|------|---------------------|---------------------|------------|
| I _{CC} | Quiescent Power Supply Current | V _{CC} = Max. V _{IN} ≥ V _{HC} ; V _{IN} ≤ V _{LC} | | — | 0.2 | 1.5 | mA |
| ΔI _{CC} | Quiescent Power Supply Current TTL Inputs HIGH | V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾ | | — | 0.5 | 2 | mA |
| I _{CCD} | Dynamic Power Supply Current ⁽⁴⁾ | V _{CC} = Max. Outputs Open $\overline{OE} = \overline{EN} = GND$ One Input Toggling 50% Duty Cycle | V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} | — | 0.15 | 0.25 | mA/ MHz |
| I _C | Total Power Supply Current ⁽⁶⁾ | V _{CC} = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle $\overline{OE} = \overline{EN} = GND$ One Bit Toggling at f _i = 5MHz 50% Duty Cycle | V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT) | — | 1.7 | 4 | mA |
| | | | V _{IN} = 3.4V V _{IN} = GND | — | 2.2 | 6 | |
| | | V _{CC} = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle $\overline{OE} = \overline{EN} = GND$ at f _i = 2.5MHz Eight Bits Toggling | V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT) | — | 4 | 7.8 ⁽⁵⁾ | |
| | | | V _{IN} = 3.4V V _{IN} = GND | — | 6.2 | 16.8 ⁽⁵⁾ | |

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at V_{CC} = 5.0V, +25°C ambient.

3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.

6. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for register devices (zero for non-register devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

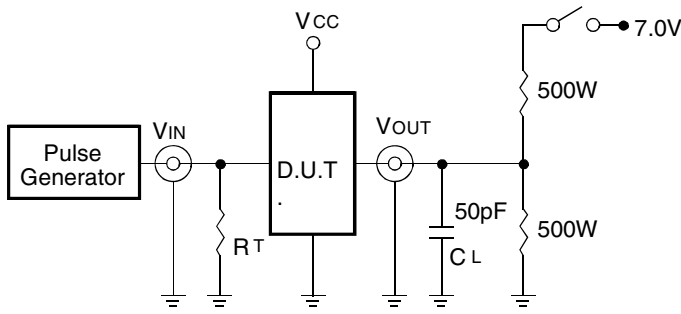
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol | Parameter | Condition ⁽¹⁾ | 54/74FCT823A | | | | 54FCT823B | | 74FCT823C | | Unit |
|--------------------------------------|---|--|---------------------|------|---------------------|------|---------------------|------|---------------------|------|------|
| | | | Com'l. | | Mil. | | Mil. | | Com'l. | | |
| | | | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | |
| t _{PLH} t _{PHL} | Propagation Delay CP to Yx ($\overline{OE} = \text{LOW}$) | CL = 50pF RL = 500Ω | — | 10 | — | 11.5 | — | 8.5 | — | 6 | ns |
| | | CL = 300pF ⁽³⁾ RL = 500Ω | — | 20 | — | 20 | — | 16 | — | 12.5 | |
| t _{PZH} t _{PZL} | Output Enable Time, \overline{OE} to Yx | CL = 50pF RL = 500Ω | — | 12 | — | 13 | — | 9 | — | 7 | ns |
| | | CL = 300pF ⁽³⁾ RL = 500Ω | — | 23 | — | 25 | — | 16 | — | 12.5 | |
| t _{PHZ} t _{PLZ} | Output Disable Time, \overline{OE} to Yx | CL = 5pF ⁽³⁾ RL = 500Ω | — | 7 | — | 8 | — | 7 | — | 6.2 | ns |
| | | CL = 50pF RL = 500Ω | — | 8 | — | 9 | — | 8 | — | 6.5 | |
| t _{SU} | Set-up Time HIGH or LOW, Dx to CP Set-up Time HIGH or LOW, \overline{EN} to CP | CL = 50pF RL = 500Ω | 4 | — | 4 | — | 3 | — | 3 | — | ns |
| t _H | Hold Time HIGH or LOW, Dx to CP | | 2 | — | 2 | — | 1.5 | — | 1.5 | — | |
| t _H | Hold Time HIGH or LOW, \overline{EN} to CP | | 2 | — | 2 | — | 0 | — | 0 | — | |
| t _{PHL} | Propagation Delay, \overline{CLR} to Yx | | — | 14 | — | 15 | — | 9.5 | — | 8 | |
| t _{REM} | Recovery Time, \overline{CLR} to CP | | 6 | — | 7 | — | 6 | — | 6 | — | |
| t _W | CP Pulse Width HIGH or LOW | | 7 | — | 7 | — | 6 | — | 6 | — | |
| t _W | \overline{CLR} Pulse Width HIGH or LOW | | 6 | — | 7 | — | 6 | — | 6 | — | |

NOTES:

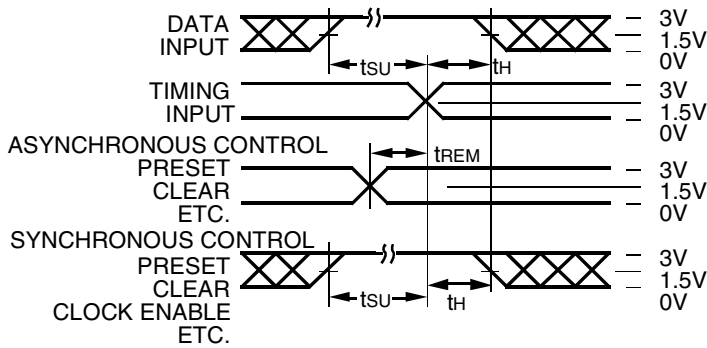
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS



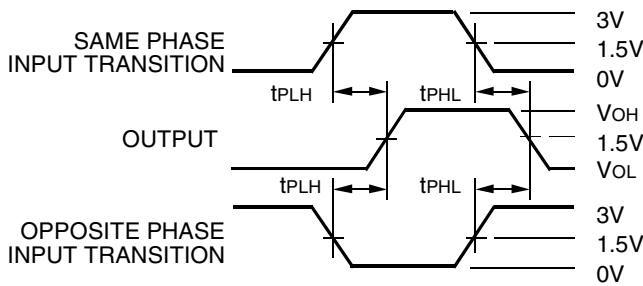
Octal Link

Test Circuits for All Outputs



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Set-Up, Hold, and Release Times



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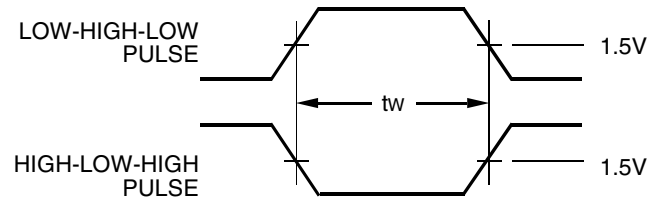
Propagation Delay

SWITCH POSITION

| Test | Switch |
|---|--------|
| Open Drain Disable Low Enable Low | Closed |
| All Other Tests | Open |

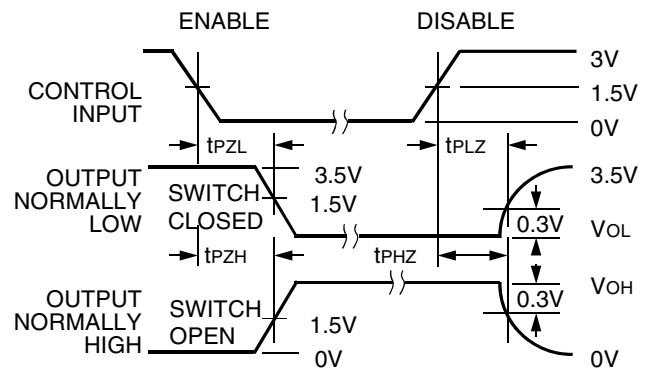
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

Octal Link



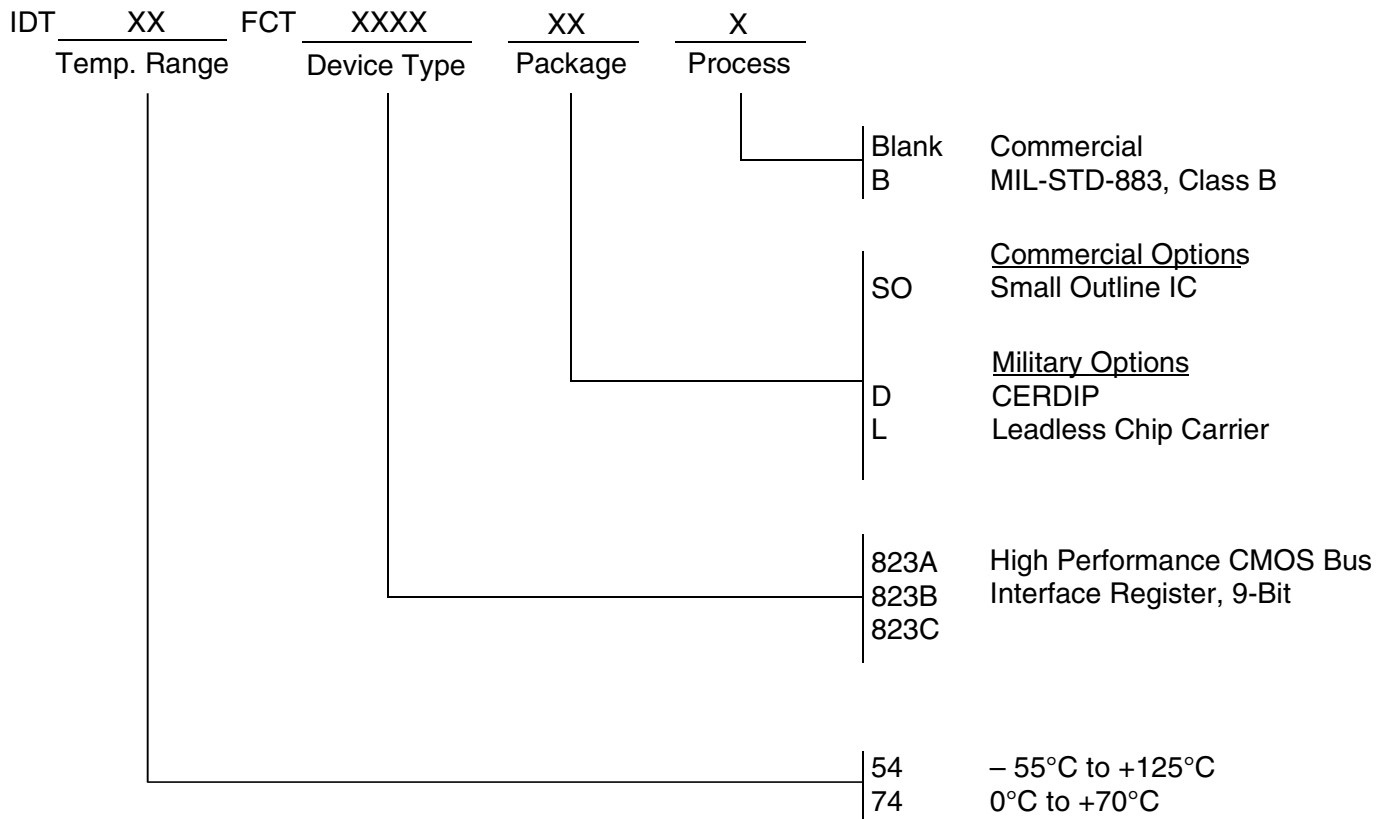
Octal Link

Enable and Disable Times

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Zo ≤ 50Ω; tr ≤ 2.5ns; tr ≤ 2.5ns.

ORDERING INFORMATION



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