

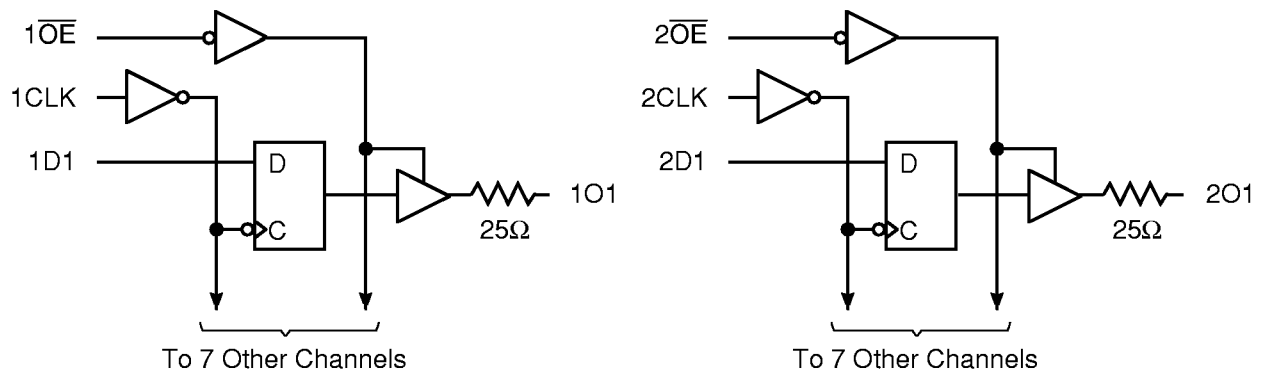
## FEATURES/BENEFITS

- 5V tolerant inputs and outputs
- Bus Hold feature holds last active state during 3-state operation
- 25Ω series resistor for low switching noise
- 10μA I<sub>CCQ</sub> quiescent power supply current
- Hot insertable
- 2.0V-3.6V V<sub>CC</sub> supply operation
- ±12mA balanced output drive
- t<sub>PD</sub> = 6.2ns
- Input hysteresis for noise immunity
- Multiple power and ground pins for low noise
- Operating temperature range:  
-40°C to 85°C
- Latch-up performance exceeds 500mA
- ESD performance:  
Human body model > 2000V  
Machine model > 200V
- Packages available:  
48-pin TSSOP  
48-pin SSOP

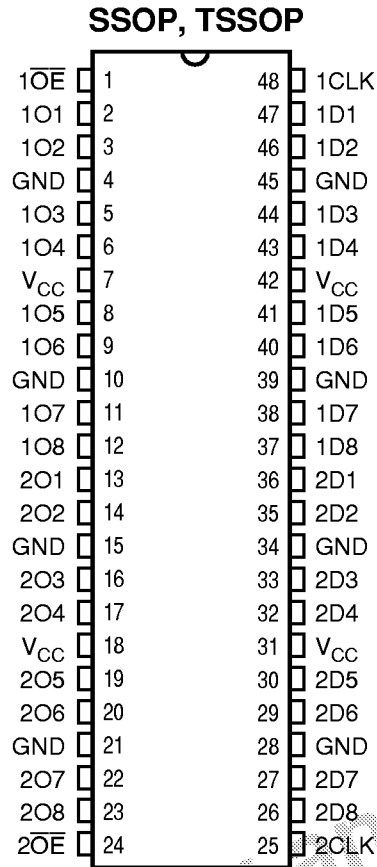
## DESCRIPTION

The LCX162H374 is a 16-bit buffered register with three-state outputs that is ideal for driving address and data buses. The output enable ( $\overline{xOE}$ ) and clock ( $xCLK$ ) controls are organized to operate each device as two 8-bit registers, or one 16-bit register with common clock. Easy board layout is facilitated by the use of flow-through pinouts and byte enable controls provide architectural flexibility for systems designers. The QS74LCX162H374 with integrated output resistor is ideally suited for low noise environments where reduced output overshoot and undershoot are critical requirements. Bus Hold circuitry on the data inputs retains the last active state during 3-state operation, eliminating the need for external pull-up resistors. The 3.3V LCXPlus family features low power, low switching noise, and fast switching speeds for low power portable applications as well as high-end advanced workstation applications. 5V tolerant inputs and outputs allow this LCXPlus product to be used in mixed 5V and 3.3V applications. To accommodate hot-plug or live insertion applications, this product is designed not to load an active bus when V<sub>CC</sub> is removed.

**Figure 1. Functional Block Diagram**



**Figure 2. Pin Configuration**  
(All Pins Top View)



**Table 1. Pin Description**

Name	I/O	Description
xDx	I	Data Inputs (Bus Hold Inputs)
xOx	O	Data Outputs
xCLK	I	Clock Input
xOE	I	Output Enable

**Table 2. Function Table**

Inputs			Internal Q Value	Outputs xOx	Function
xOE	xCLK	xDx			
H	X	X	X	Hi-Z	Disable Outputs
L	↑	L	L	L	Load Input Data
L	↑	H	H	H	Enable Outputs
H	↑	L	L	Hi-Z	Load Input Data
H	↑	H	H	Hi-Z	Disable Outputs

**Table 3. Capacitance**

Symbol	Pins	Typ	Unit	Conditions
$C_{IN}$	Input Capacitance	7.0	pF	$V_{IN} = 0V, V_{OUT} = 0V, f = 1MHz$
$C_{I/O}$	I/O Capacitance	8.0	pF	$V_{IN} = 0V, V_{OUT} = 0V, f = 1MHz$
$C_{PD}$	Power Dissipation Capacitance	20	pF	$V_{CC} = 3.3V, V_{IN} = 0 \text{ or } V_{CC}, f = 10MHz$

**Note:** Capacitance is characterized but not production tested.

**Table 4. Absolute Maximum Ratings**

Supply Voltage to Ground .....	-0.5V to 7.0V
DC Output Voltage $V_{OUT}$	
Outputs HIGH-Z .....	-0.5V to 7.0V
Outputs Active .....	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage $V_{IN}$ .....	-0.5V to 7.0V
DC Input Diode Current with $V_{IN} < 0$ .....	-50mA
DC Output Diode Current	
$V_O < 0$ .....	-50mA
$V_O > V_{CC}$ .....	50mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ ) .....	$\pm 50mA$
DC Supply Current per Supply Pin .....	$\pm 100mA$
DC Ground Current per Ground Pin .....	$\pm 100mA$
$T_{STG}$ Storage Temperature .....	-65° to 150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

**Table 5. Recommended Operating Conditions**

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	Supply Voltage, Operating	2.0	3.6	V	
	Supply Voltage, Data Retention Only	1.5	3.6		
$V_{IN}$	Input Voltage	0	5.5	V	
$V_{OUT}$	Output Voltage in Active State	0	$V_{CC}$	V	
$V_{OUT}$	Output Voltage in "OFF" State	0	5.5	V	
$I_{OH}/I_{OL}$	Output Current	$V_{CC} = 3.0 - 3.6V$	—	$\pm 12$	mA
		$V_{CC} = 2.7V$	—	$\pm 6$	
$\Delta t/\Delta v$	Input Transition Slew Rate	—	10	ns/V	
$T_A$	Operating Free Air Temperature	-40	85	°C	

**Table 6. DC Electrical Characteristics Over Operating Range**

Industrial Temperature Range,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Typ <sup>(2)</sup>	Max	Unit
$V_{IH}$	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
$V_{IL}$	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = 2.7\text{V}, I_{OH} = -100\mu\text{A}$ $V_{CC} = 3.0\text{V}, I_{OH} = -12\text{mA}$ $V_{CC} = 3.0\text{V}, I_{OH} = -18\text{mA}$	$V_{CC}-0.2$ 2.4 2.2	—	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = 2.7\text{V}, I_{OL} = 100\mu\text{A}$ $V_{CC} = 3.0\text{V}, I_{OL} = 12\text{mA}$ $V_{CC} = 3.0\text{V}, I_{OL} = 18\text{mA}$	— — —	—	0.2 0.55 0.8	V
$R_{OUT}$	Output Resistance	$V_{CC} = 3.0\text{V}, I_{OL} = 12\text{mA}$	—	28	—	$\Omega$
$\Delta V_T$	Input Hysteresis <sup>(3)</sup>	$V_{TLH} - V_{THL}$ for All Inputs	—	150	—	mV
$ I_{BH} $	Input Current Input High or Low Bus Hold Inputs <sup>(3,4)</sup>	$V_{CC} = 3.6\text{V}, V_{IN} = 0\text{V}$ or $V_{IN} = V_{CC}$	—	—	50	$\mu\text{A}$
		$V_{CC} = 3.6\text{V}, 0.8\text{V} < V_{IN} < 2.0\text{V}$	—	—	500 <sup>(5)</sup>	$\mu\text{A}$
$I_{BHH}$	Bus Hold Sustaining Current	$V_{CC} = 3\text{V}$	$V_{IN} = 2.0\text{V}$	-75	—	$\mu\text{A}$
$I_{BHL}$	Bus Hold Inputs		$V_{IN} = 0.8\text{V}$	75	—	$\mu\text{A}$
$I_I$	Input Leakage Current	$V_I = 0\text{V}, V_I = 5.5\text{V}, V_{CC} = 3.6\text{V}$	—	—	$\pm 1.0$	$\mu\text{A}$
$I_{OZ}$	High-Z I/O Leakage	$V_O = 0\text{V}, V_O = 5.5\text{V}$ $V_I = V_{IH}$ or $V_{IL}, V_{CC} = 3.6\text{V}$	—	—	$\pm 1.0$	$\mu\text{A}$
$I_{OS}$	Short Circuit Current <sup>(3,6)</sup>	$V_{CC} = 3.6\text{V}, V_{OUT} = \text{GND}$	-60	—	-200	mA
$I_{OR}$	Current Drive <sup>(3)</sup>	$V_{CC} = 3.6\text{V}, V_{OUT} = 2.0\text{V}$	40	—	—	mA
$I_{OFF}$	Power Off Leakage	$V_{CC} = 0\text{V}, V_I$ or $V_O = 5.5\text{V}$	—	—	10	$\mu\text{A}$
$V_{IK}$	Input Clamp Voltage	$V_{CC} = 2.7\text{V}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V

**Notes:**

1. For conditions shown as Min. or Max. use appropriate value specified under Recommended Operating Conditions for the applicable device type.
2. Typical values are at  $V_{CC} = 3.3\text{V}$  and  $T_A = 25^{\circ}\text{C}$ .
3. These parameters are guaranteed by characterization, but not production tested.
4. Pins with Bus Hold are identified in the Pin Description.
5. An external driver must provide at least  $|I_{BH}|$  during transition to guarantee that the Bus Hold input will change state.
6. Not more than one output should be tested at one time. Duration of test should not exceed one second.

**Table 7. Power Supply Characteristics**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Typ <sup>(2)</sup>	Max	Unit	
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = 3.6V$ , Freq = 0 $V_{IN} = GND$ or $V_{CC}$	0.1	10	$\mu A$	
$\Delta I_{CC}$	Supply Current per Input @ TTL HIGH <sup>(3)</sup>	$V_{CC} = 3.6V$ , $V_{IN} = V_{CC} - 0.6V$ , Freq = 0	Control Inputs	2.0	30	$\mu A$
			Bus Hold Inputs	—	500	$\mu A$
$I_{CCD}$	Supply Current per Input per MHz <sup>(4)</sup>	$V_{CC} = 3.6V$ , Outputs Open One Bit Toggling @ 50% Duty Cycle $\overline{xOE} = GND$	50	75	$\mu A / MHz$	
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = 3.6V$ , Outputs Open One Bit Toggling @ 50% Duty Cycle $\overline{xOE} = GND$ , $f = 5MHz$ $f_{CP} = 10MHz$	$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = GND$	0.5 <sup>(5)</sup>	1.0 <sup>(5)</sup>	mA
		$V_{CC} = 3.6V$ , Outputs Open Sixteen Bits Toggling @ 50% Duty Cycle $\overline{xOE} = GND$ , $f = 2.5MHz$ $f_{CP} = 10MHz$	$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = GND$	2.0 <sup>(5)</sup>	7.0 <sup>(5)</sup>	mA

**Notes:**

- For conditions shown as Min. or Max., use the appropriate values specified under Recommended Operating Conditions for applicable device type.
- Typical values are at  $V_{CC} = 3.3V$ , 25°C ambient.
- Per TTL driven input. All other inputs at  $V_{CC}$  or GND.
- This parameter is not directly testable, but is derived for use in total power supply calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed by design but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CCQ} + \Delta I_{CC} D_H N_T + I_{CCD} f N_O$   
 $I_{CCQ} =$  Quiescent Current ( $I_{CCL}$ ,  $I_{CCH}$ , and  $I_{CCZ}$ ).  
 $\Delta I_{CC} =$  Power Supply Current for a TTL-High Input ( $V_{IN} = V_{CC} - 0.6V$ ).  
 $D_H =$  Duty Cycle for TTL High Inputs.  
 $N_T =$  Number of TTL High Inputs.  
 $I_{CCD} =$  Dynamic Current Caused by an Input Transition Pair (HLH or LHL).  
 $f =$  Average Switching Frequency per Output.  
 $N_O =$  Number of Outputs Switching.

**Table 8. Dynamic Switching Characteristics <sup>(1)</sup>**

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = 25^\circ C$	Units
				Typical	
$V_{OLP}$	Quiet Output Dynamic Peak $V_{OL}$	$C_L = 30pF$ , $V_{IH} = 3.3$ , $V_{IL} = 0V$	3.3	0.8	V
$V_{OLV}$	Quiet Output Dynamic Peak $V_{OL}$	$C_L = 30pF$ , $V_{IH} = 3.3$ , $V_{IL} = 0V$	3.3	0.8	V

**Note:**

- Characterized but not production tested.

**Table 9. Switching Characteristics Over Operating Range**

Industrial Temperature Range,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}$

$C_{\text{LOAD}} = 30\text{pF}$ ,  $R_{\text{LOAD}} = 500\Omega$  unless otherwise noted.

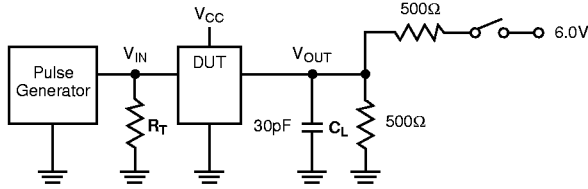
Symbol	Description <sup>(1)</sup>	$V_{\text{CC}} = 3.3 \pm 0.3\text{V}$		$V_{\text{CC}} = 2.7\text{V}^{(2)}$		Unit
		Min	Max	Min	Max	
$f_{\text{MAX}}$	Clock Pulse Frequency <sup>(2)</sup>	170	—	—	—	MHz
$t_{\text{PHL}}$ $t_{\text{PLH}}$	Propagation Delay xCLK to xOx	2.0	6.2	2.0	6.5	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output Enable Time xOE to xOx	1.5	6.1	1.5	6.3	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output Disable Time <sup>(2)</sup> $\overline{\text{xOE}}$ to xOx	1.5	6.0	1.5	6.2	ns
$t_{\text{S}}$	Data Setup Time xDx to xCLK	2.5	—	2.5	—	ns
$t_{\text{H}}$	Data Hold Time xDx to xCLK	1.5	—	1.5	—	ns
$t_{\text{W}}$	Clock Pulse Width HIGH or LOW <sup>(2)</sup>	3.0	—	3.0	—	ns
$t_{\text{SK(o)}}$	Output Skew <sup>(3)</sup>	—	0.5	—	—	ns

Notes:

1. Minimums guaranteed but not tested on propagation delays. See Test Circuit and Waveforms.
2. Guaranteed by characterization.
3. Skew between any two outputs of the same package switching in the same direction.  
This parameter is guaranteed by characterization but not production tested.

TEST CIRCUIT AND WAVEFORMS

Figure 3. Test Circuit



SWITCH POSITION	
Test	Switch
Open Drain	
Disable LOW	6V
Enable LOW	
Disable HIGH	GND
Enable HIGH	
All Other Inputs	Open

DEFINITIONS:  
 $C_L$  = Load capacitance: includes jig and probe capacitance.  
 $R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse generator.

Figure 4. Setup, Hold, and Release Timing

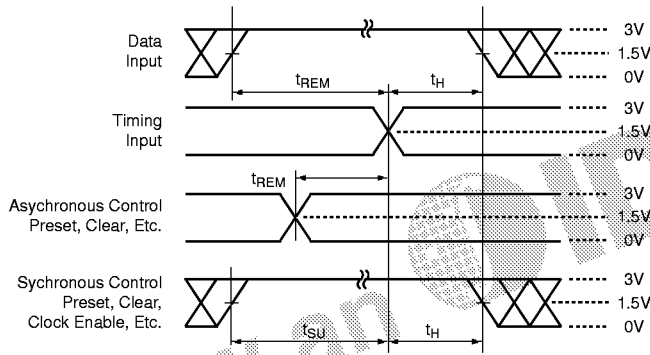


Figure 6. Pulse Width

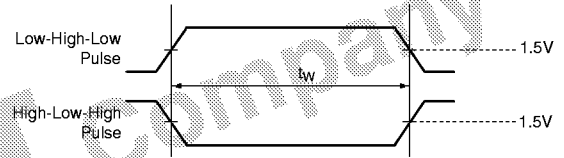
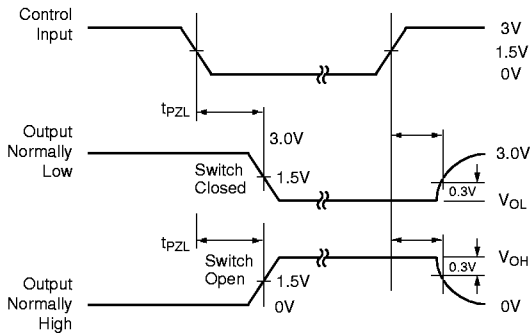


Figure 5. Enable and Disable Timing



Notes:

1. Input Control Enable = LOW and Input Control Disable = HIGH.
2. Pulse Generator for All Pulses: Rate  $\leq$  1.0MHz;  
 $Z_{OUT} \leq 50\Omega$ ;  $t_F, t_R \leq 2.5ns$ .

Figure 7. Propagation Delay

