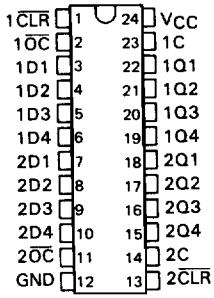
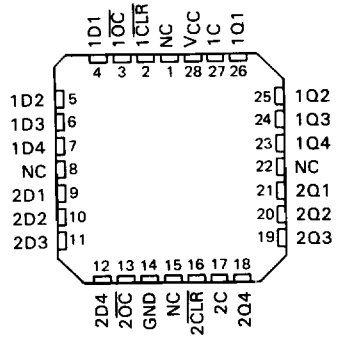
D2661, APRIL 1982—REVISED DECEMBER 1983

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **'ALS880 and 'AS880 Are Alternative Versions with Inverting Outputs**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS873, SN54AS873 . . . JT PACKAGE
SN74ALS873, SN74AS873 . . . NT PACKAGE
(TOP VIEW)



SN54ALS873, SN54AS873 . . . FH PACKAGE
SN74ALS873, SN74AS873 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These dual 4-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

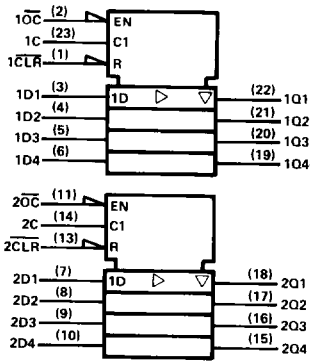
The dual 4-bit latches are transparent D-type. While the latch enable input (1C or 2C) is high, the Q outputs will follow the data (D) inputs in true form, according to the function table. When the latch enable input is taken low, the outputs will be latched. When $\overline{CLR}$ goes low, the Q outputs go low independently of enable C. The outputs are in a high-impedance state when $\overline{OC}$ (output control) is at a high logic level.

The SN54ALS873 and SN54AS873 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS873 and SN74AS873 are characterized for operation from 0 °C to 70 °C.

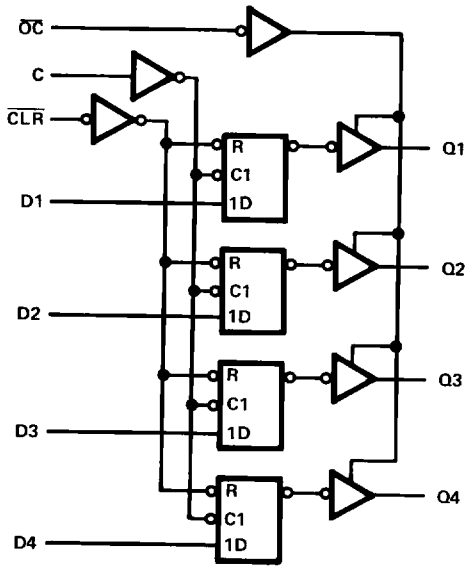
FUNCTION TABLE (EACH LATCH)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	ENABLE C	D	Q
L	L	X	X	L
L	H	H	H	H
L	H	H	L	L
L	H	L	X	Q_0
H	X	X	X	Z

logic symbol



functional block diagram (each quad latch, positive logic)



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS873, SN54AS873 . . . . . −55 °C to 125 °C
SN74ALS873, SN74AS873 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS873			SN74ALS873			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration	$\overline{CLR}$ low	15			15			ns
		Enable C high	10			10			
t_{su}	Setup time, data before enable C↓		10			10			ns
t_h	Hold time, data after enable C↓		7			7			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS873			SN74ALS873			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		10	21		10	21	mA
		Outputs low		15	29		15	29	
		Outputs disabled		16	31		16	31	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

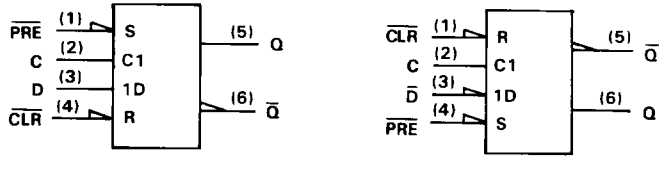
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS873		SN74ALS873		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2	15	2	14	ns
t_{PHL}			2	15	2	14	
t_{PLH}	C	Q	8	29	8	22	ns
t_{PHL}			8	22	8	21	
t_{PHL}	$\overline{CLR}$	Q	6	24	6	24	ns
t_{PZH}	$\overline{OC}$	Q	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OC}$	Q	2	10	2	8	ns
t_{PLZ}			2	15	2	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D latch signal conventions

It is TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (⊵) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

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recommended operating conditions

			SN54AS873			SN74AS873			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{CLR}$ low	4.5			3.5			ns
		Enable C high	5.5			4.5			
t_{su}	Setup time, data before enable C↓		2			2			ns
t_h	Hold time, data after enable C↓		3			3			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS873			SN74AS873			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	$V_{CC}-2$			$V_{CC}-2$			V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		68	110		68	110	mA
		Outputs low		67	109		67	109	
		Outputs disabled		80	129		80	129	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS873		SN74AS873		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3	9	3	6	ns
t_{PHL}			3	7	3	6	
t_{PLH}	C	Q	6	14	6	11.5	ns
t_{PHL}			4	9	4	7.5	
t_{PHL}	$\overline{CLR}$	Q	3	8.5	3	7.5	ns
t_{PZH}	$\overline{OC}$	Q	2	8	2	6.5	ns
t_{PZL}			4	11	4	9.5	
t_{PHZ}	$\overline{OC}$	Q	2	8	2	6.5	ns
t_{PLZ}			2	8.5	2	7.5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.