



Single Wide Bandwidth Analog Switch

Features

- Single-Supply Operation (+2V to +6V)
- · Rail-to-Rail Analog Signal Dynamic Range
- Low On-Resistance (6Ω typ with 5V supply) Minimizes Distortion and Error Voltages
- On-Resistance Flatness, 3Ω typical
- Low Charge Injection Reduces Glitch Errors. Q = 4pC (typical)
- Replaces Mechanical Relays
- High Speed: t_{ON} = 10ns typical
- Wide -3dB Bandwidth: 300 MHz (typical)
- High-Current Channel Capability: >100mA
- TTL/CMOS Logic Compatible
- Low Power Consumption (0.5µW typical)
- Small outline transistor package minimizes board area
 - 65 mil wide SOT23-5 (T5)

Applications

- · Audio, Video Switching and Routing
- Battery-Powered Communication Systems
- · Computer Peripherals
- Telecommunications
- · Portable Instrumentation
- · Mechanical Relay Replacement
- · Cell Phones
- PDAs

Truth Table

ŌĒ	PI5A125		
0	ON		
1	OFF		

Switch shown for Logic "0" input

Ordering Information

P/N	Package			
PI5A125T	SOT23-5			

Description

The PI5A125 is a single analog switch designed for single-supply operation. This high-precision device is ideal for low-distortion audio, video, signal switching and routing.

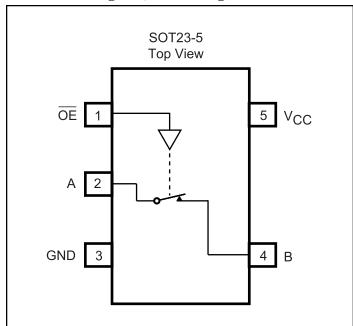
The PI5A125 is a single-pole single-throw (SPST), normally closed (NC) switch. The switch is open when \overline{OE} is HIGH.

This switch conducts current equally well in either direction when on. When off, it blocks voltages up to V_{CC} .

The PI5A125 is fully specified with +5V, and +3.3V supplies. With +5V, it guarantees <10W on-resistance. On-resistance flatness is less than 5Ω over the specified range. The switch also guarantees fast switching speeds (t_{ON} <20ns).

This product is available in a 5-pin SOT23 plastic package for operation over the industrial (-40°C to +85°C) temperature range.

Functional Diagram, Pin Configuration





Electrical Specifications - Single +5V Supply $(V_{CC} = +5V \pm 10\%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)$

Description	Parameter	Conditions	Temp. (°C)	Min. ⁽²⁾	Typ. ⁽¹⁾	Max. ⁽²⁾	Units
Analog Switch							
Analog Signal Range (3)	V _{ANALOG}		Full	0		V _{CC}	
On-Resistance	ъ	$V_{CC} = 4.5V, I_{B} = -30 \text{ mA},$ $V_{A} = +2.5V$	25		8	10	V
	R_{ON}		Full			12	1
(5)	D.	$V_{CC} = 5V, I_B = -30 \text{ mA},$	25		2.5	3.5	Ω
On-Resistance Flatness ⁽⁵⁾	R _{FL} AT(ON)	$V_A = 1V, 2.5V, 4V$	Full			4	
G (6)	I _{A(OFF)} or	$V_{CC} = 5.5V, V_B = 0V,$	25		0.20		
Off Leakage Current ⁽⁶⁾	I _{B(OFF)}	$V_A = 4.5V$	Full	-80		80	
On Leakage Current ⁽⁶⁾	I _{A(ON)} or	V+ = 5.5V,	25		0.20		nA
On Leakage Current	$I_{B(ON)}$	$V_B = V_A = +4.5V$	Full	-80		80	
Logic Input				•			
Input High Voltage	V _{IH}	Guaranteed Logic High Level	Full	2			**7
Input Low Voltage	V _{IL}	Guaranteed Logic Low Level				0.8	V
Input Current with Input Voltage High	I _{INH}	V_{IN} =2.4V, all others = 0.8V		- 1	0.005	1	μА
Input Current with Input Voltage Low	I _{INL}	V_{IN} =0.8V, all others = 2.4V					
Dynamic				-		•	•
T. O. T.		V CV E 1	25		7	15	nc
Turn-On Time	ton	$V_{CC} = 5V$, see Figure 1	Full			20	
T. Off T.	,		25		1	7	
Turn-Off Time	toff	$V_{COM} = \pm 3V$, see Figure 2	Full		2	5	
Charge Injection (3)	Q	$C_L = 1 \text{nF}, V_{GEN} = 0 \text{V},$ $R_{GEN} = 0 \Omega, \text{ see Figure 2}$				10	pC
Off Isolation	OIRR	$R_L = 50\Omega$, $C_L = 5pF$, f = 10 MHz, see Figure 3	25				dB
A or B Off Capacitance	C _(OFF)	f = 1kHz, see Figure 4			5.5		pF
On Capacitance	C _(ON)	f = 1kHz, see Figure 5			5.5		
-3dB Bandwidth	BW	$R_L = 50\Omega$, see Figure 6			300		MHz
Supply		•	1			1	
Power-Supply Range	V _{CC}			2		6	V
Positive Supply Current	I_{CC}	$V+=5.5V,V_{IN}=0V$ or $V_{CC},$ All channels on or off	Full			1	μА

PS8199B 03/25/99 2



Absolute Maximum Ratings

Voltages Referenced to GND	
V _{CC}	-0.5V to +7V
V _{OE} , V _A , V _B ⁽¹⁾	-0.5V to V _{CC} +2V
	or 30mA, whichever occurs first
Current (any terminal except A	A, B) 30mA
Current: A,B (pulsed at 1ms,	10% duty cycle) 120mA

Thermal Information

Continuous Power Dissipation	
SOT23-5 (derate 7mW/°C above +70°C)	550mW
Storage Temperature65°	C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1:

Signals on \overline{OE} , A, B exceeding Vcc or Gnd are clamped by internal diodes. Limit forward diode current to 30mA.

Caution: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

Electrical Specifications-Single +3.3V Supply $(V_{CC} = +3.3V \pm 10\%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)$

Parameter	Symbol	Conditions	Temp(°C)	Min. ⁽¹⁾	Typ. ⁽²⁾	Max. ⁽¹⁾	Units
Analog Switch	•						
Analog Signal Range ⁽³⁾	V _{ANALOG}			0		V _{CC}	V
On-Resistance	Pov	$V_{CC} = 3V$, $I_B = -30$ mA, $V_A = 1.5V$	25		12	18	
	R _{ON}		Full			22	Ω
On-Resistance Flatness ^(3,5)	R _F LAT(ON)	$V_{CC} = 3.3V, I_B = -30mA,$ $V_A = 0.8V, 2.5V$	25		0.5	4	
			Full			5	
Dynamic							
Turn-On Time	ton	V_{CC} =3.3V to VNO or VNC = 1.5V, Fig.1	25		15	25	
			Full			40	
Turn-Off Time	tOFF		25		1.5	12	ns
			Full			20	
Charge Injection ⁽³⁾	Q	$C_L = 1$ nf, $V_{GEN} = 0$ V, $R_{GEN} = 0$ V, Fig.2	25		1.3	10	pC
Supply							
I _{CC}	Positive Supply Current	$V_{CC} = 3.6V$, $V_{IN} = 0V$ or V_{CC} All channels on or off	Full			1	μA

Notes:

1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.

3

- 2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
- 3. Guaranteed by design
- 4. $\Delta R_{ON} = R_{ON} \max R_{ON} \min$
- 5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.
- 6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25°C.
- 7. Off Isolation = $20log_{10} V_B / V_A$. See figure 3.

PS8199B 03/25/99



Test Circuits/Timing Diagrams

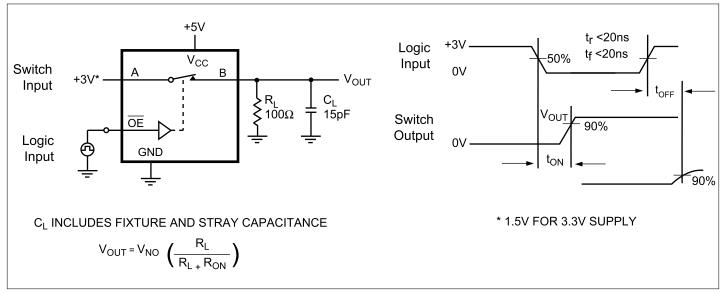


Figure 1. Switching Time

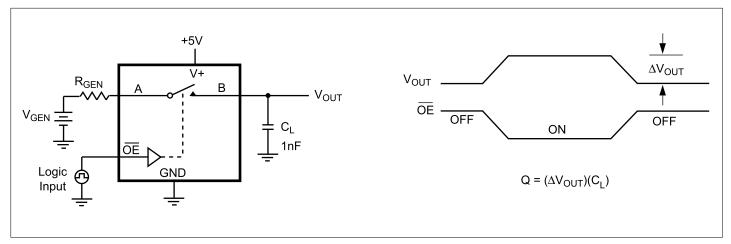


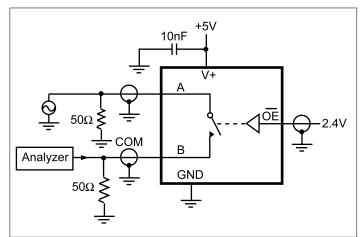
Figure 2. Charge Injection

4

PS8199B 03/25/99



Test Circuits/Timing Diagrams (continued)



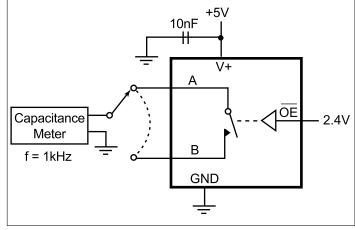


Figure 3. Off Isolation

Figure 4. Channel-Off Capacitance

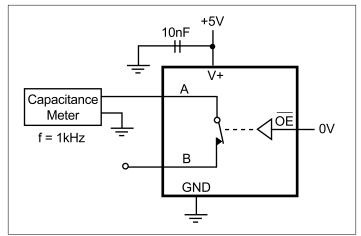


Figure 5. Channel-On Capacitance

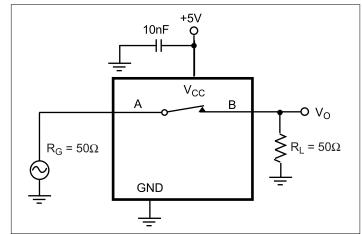


Figure 6. Bandwidth

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5

PS8199B 03/25/99