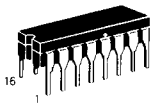
MC54/74HC4543

BCD-to-Seven-Segment Latch/ Decoder/Display Driver for LCDs

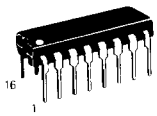
High-Performance Silicon-Gate CMOS

The MC54/74HC4543 is compatible in both function and pinout with the MC14543B metal-gate CMOS decoder/driver. This device is designed for use with liquid-crystal display (LCD) readouts. The HC4543 provides a 4-bit storage latch, a BCD-to-seven-segment decoder, and an LCD driver. The blanking input (BI) and latch enable (LE, active low) are used to blank the display and store the BCD code, respectively. A square wave is applied to the phase input (Ph) of the HC4543 and electrically common backplane of the LCD.

- Latch Storage of BCD Inputs
- Blanking Input
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 252 FETs or 63 Equivalent Gates



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-06

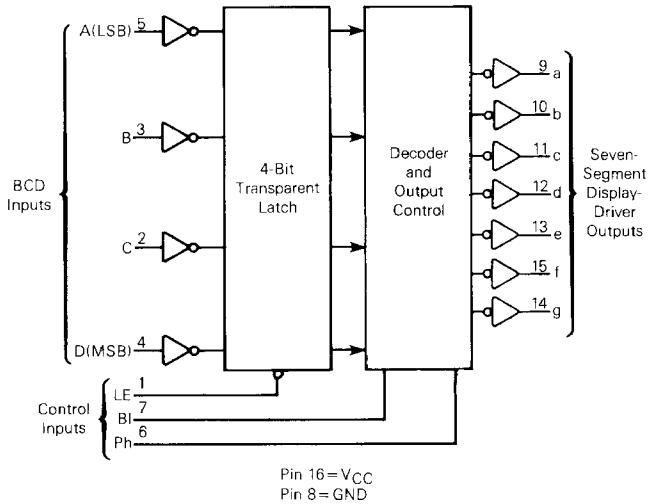
D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

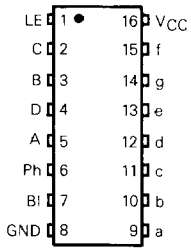
$T_A = -55°$ to 125°C for all packages.
Dimensions in Chapter 7.

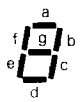
BLOCK DIAGRAM



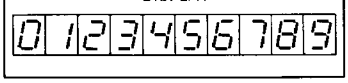
Pin 16 = V_{CC}
Pin 8 = GND

PIN ASSIGNMENT





DISPLAY



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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(Plastic DIP or SOIC Package)	260	
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C
Ceramic DIP: −10 mW/°C from 100° to 125°C
SOIC Package: −7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0 V	0	1000	ns
	(Figure 3)	V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to −55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20\ \mu A$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20\ \mu A$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\ \mu A$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 4.0$ mA	4.5	3.98	3.84	3.70	
		$\|I_{out}\| \le 5.0$ mA	6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\ \mu A$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 4.0$ mA	4.5	0.26	0.33	0.40	
		$\|I_{out}\| \le 5.0$ mA	6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A, B, C, or D to Output (Figures 1 and 5)	2.0 4.5 6.0	600 120 102	750 150 130	900 180 153	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, LE to Output (Figures 2 and 5)	2.0 4.5 6.0	600 120 102	750 150 130	900 180 153	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, BI or Ph to Output (Figures 3 and 5)	2.0 4.5 6.0	600 120 102	750 150 130	900 180 153	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 5)	2.0 4.5 6.0	600 120 102	750 150 130	900 180 153	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V_{CC} = 5.0 V 40	pF

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Input A, B, C, or D to LE (Figure 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_h	Minimum Hold Time, LE to Input A, B, C, or D (Figure 4)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t_w	Minimum Pulse Width, LE (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 3)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4.

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SWITCHING WAVEFORMS

FIGURE 1

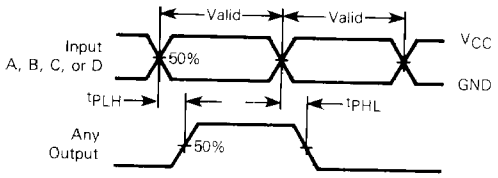


FIGURE 2

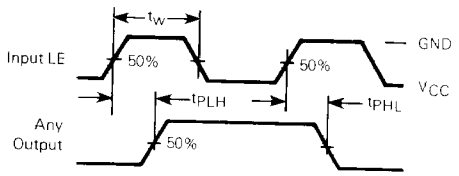


FIGURE 3

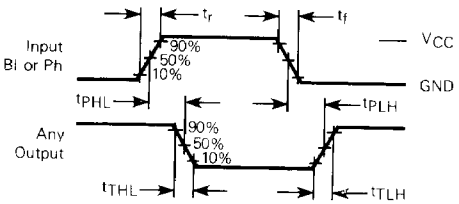


FIGURE 4

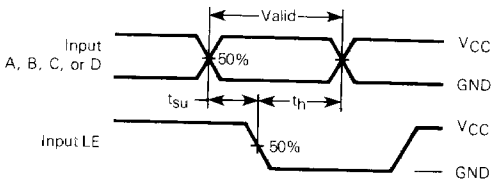
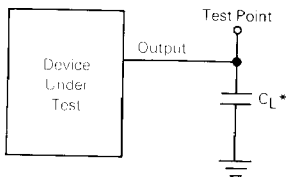


FIGURE 5 — TEST CIRCUIT



*Includes all probe and jig capacitance.

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FUNCTION TABLE

Inputs							Outputs							
LE	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	H	L	X	X	X	X	L	L	L	L	L	L	L	Blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	Blank
L	L	L	X	X	X	X	**							**
†	†	H	†				Inverse of Output Combinations Above							Display as above

X = Don't care

† = Above Combinations

* = For liquid crystal readouts, apply a square wave to Ph.

** = Depends upon the code previously applied when LE = H

PIN DESCRIPTIONS

INPUTS

A, B, C, D (PINS 5, 3, 2, 4) — BCD inputs. These are the inputs to be decoded. The data on these pins is decoded to a seven-segment output when the LE pin is high and is latched when LE is low. For inputs greater than hexadecimal 9 or for BI input high, the output is blanked. A (pin 5) is the least-significant data bit and D (pin 4) is the most-significant data bit.

OUTPUTS

a, b, c, d, e, f, g (PINS 9, 10, 11, 12, 13, 15, 14) — Decoded seven-segment display-driver outputs. For liquid-crystal displays (LCD's), these outputs are tied directly to the LCD segment pins. For other type displays, see Figure 6.

CONTROL INPUTS

LE (PIN 1) — Latch Enable input (active-low). A falling-edge signal on this pin latches the code on the A, B, C, and D pins. The code remains latched until a rising-edge signal is applied to this pin. A high level on this pin allows the code to be transferred thru the latch to the decoder.

Ph (PIN 6) — Phase input. This input is used to invert the output level. For liquid-crystal displays (LCD), a square wave is applied to this input (typically 100 Hz) and to the common backplane of the LCD. For light-emitting diode (LED), incandescent, or gas-discharge displays, the phase input is tied to the appropriate level as shown in Figure 6.

BI (PIN 7) — Blanking input pin. A high level on this pin causes the outputs to follow the phase input, thereby blanking the display (no voltage drop across LCD segments).

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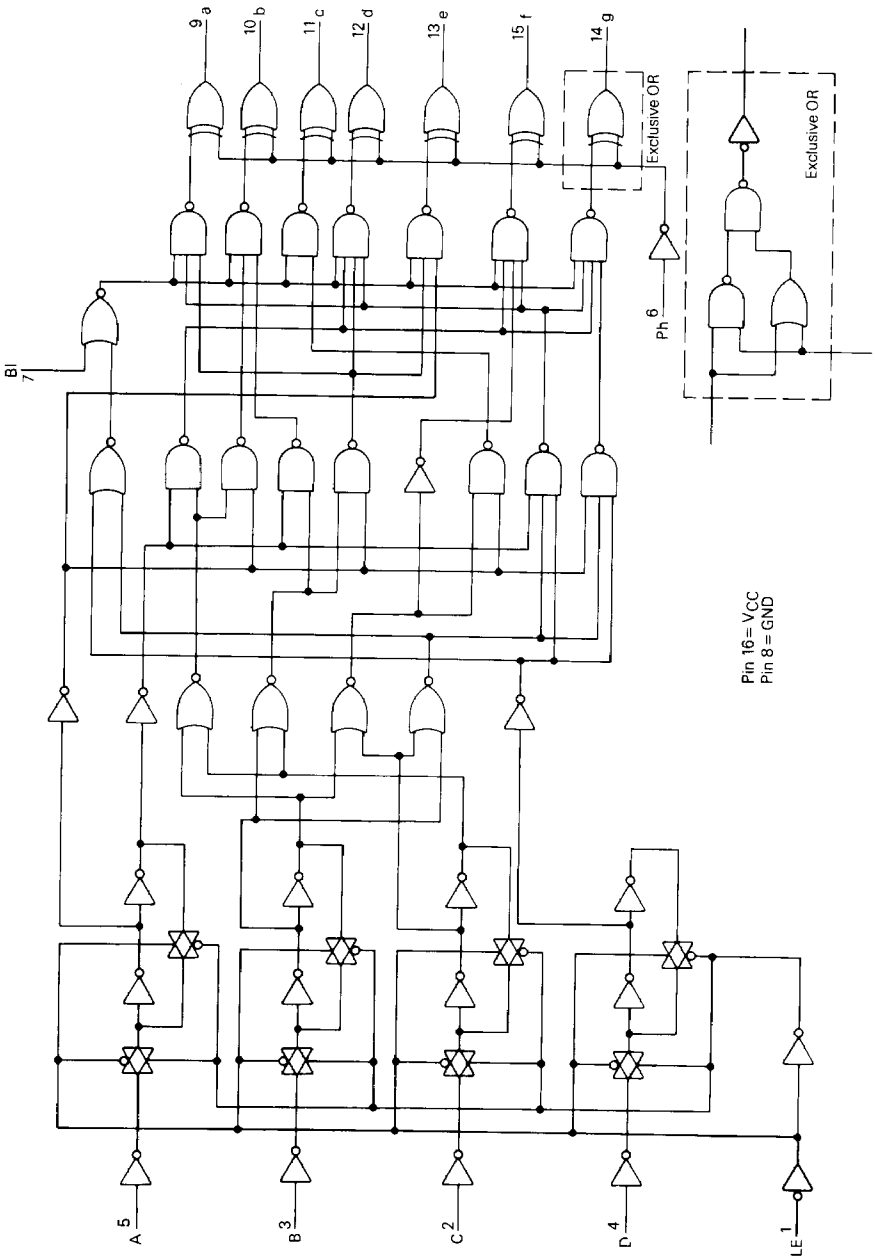
EXPANDED LOGIC DIAGRAM



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TIMING DIAGRAM

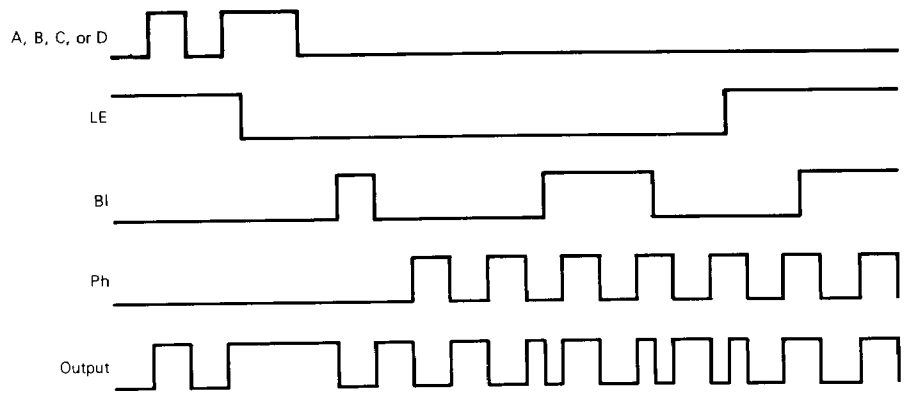
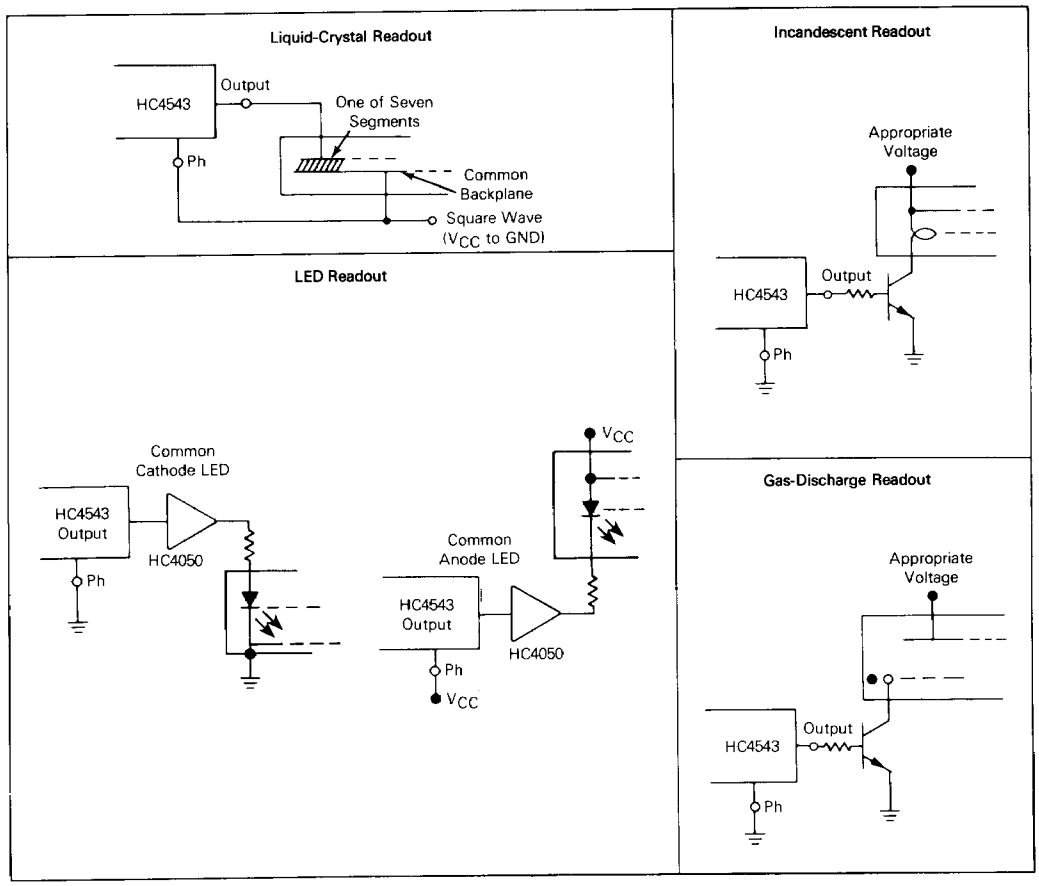


FIGURE 6 — CONNECTIONS TO VARIOUS DISPLAY READOUTS



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