FAIRCHILD SEMICONDUCTOR™

May 2001
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74LCXZR164245
16-Bit Dual Supply Translating Transceiver with 3-STATE Outputs and 26Ω Series Resistors in the Outputs (Preliminary)

General Description

The 74LCXZR164245 is a dual supply, 16-bit, translating transceiver that is designed for two-way asynchronous communication between busses at different supply voltages. This device is suited for PCMCIA and other real-time configurable I/O applications that utilize mixed power supplies.

The 74LCXZR164245 is designed to Power-Up and Power-Down into a High Impedance state (outputs disabled). The feature eliminates the need to power-up in a specific sequence to avoid drawing excessive current.

The A Port interfaces with the lower voltage bus (2.3V to 2.6V), and the B Port interfaces with the higher voltage bus (2.0V to 5.5V). This dual supply design allows for translation from low voltage busses (2.3V to 3.6V) to busses at a higher potential, up to 5.5V. The 74LCXZR164245 is intended to be used in applications where the A Port is connected to the 3.0V host system, and the B Port is connected to the PCMCIA card slots.

Furthermore, when both $\overline{OE}$'s are HIGH, the B Port I/O pins are disabled, and both B Port I/O connections and B Port V_{CC} are allowed to float. This feature permits PCMCIA cards to be inserted and removed during normal operation.

All A and B I/O include nominal 26Ω series resistors to reduce overshoot and undershoot.

The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow. Transmit (active-HIGH) enables data from A Ports to B Ports; Receive (active-LOW) enables data from B Ports to A Ports. The Output Enable ($\overline{OE}_1$, $\overline{OE}_2$) inputs, when HIGH, disable their associated ports by placing the I/Os in HIGH-Z condition. The 74LCXZR164245 is designed so that the control pins ($T/\overline{R}_n$, $\overline{OE}_n$) are powered by V_{CCA}, so that V_{CCB} may be removed when the I/Os are disabled.

The 74LCXZR164245 is suitable for mixed voltage applications such as notebook computers using a 3.3V CPU and 5.0V peripheral components. It is fabricated with an Advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- Bidirectional interface between 3V busses and 5V busses
- Supports live insertion and withdrawal (Note 1)
- Outputs source/sink up to 12 mA
- All outputs include nominal 26Ω series resistors
- Uses patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16245
- Port B I/O may be disabled by use of $\overline{OE}_n$ or removal of B Port V_{CC}
- Port B V_{CC} may be removed when $\overline{OE}_n$ is used to disable I/O's
- Port B V_{CC} removal may occur coincident with rising edge of $\overline{OE}_n$
- Configurable as one 16-bit or two 8-bit transceivers
- Unrestricted power-up sequencing

Note 1: To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value or the resistor is determined by the current-sourcing capability of the driver.

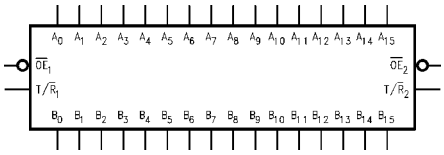
Ordering Code:

Order Number	Package Number	Package Description
74LCXZR164245MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

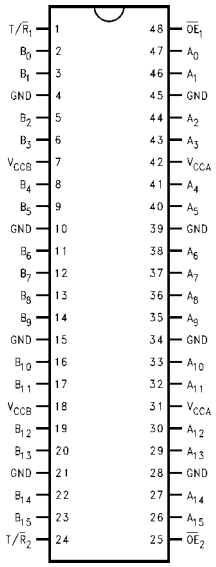
Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Quiet Series™ is a trademark of Fairchild Semiconductor Corporation.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs or 3-STATE Outputs
B_0–B_{15}	Side B Inputs or 3-STATE Outputs

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH-Z State on A_8–A_{15}, B_8–B_{15}

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance

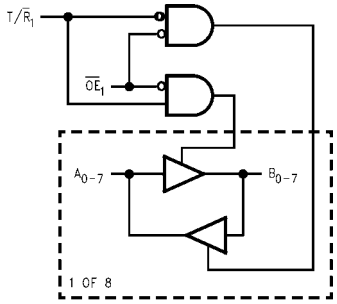
LCXZR164245 Translator Power Up Note

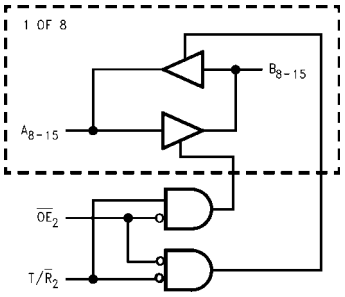
The LCXZR164245 Translator is designed with two separate V_{CC} power rails. V_{CCB} is the higher potential rail, operating at 3.0 to 5.5 volts, and V_{CCA} is the lower potential rail, operating at 2.3 to 3.6 volts. The control pins of the device ($\overline{OE}_n$, $T/\overline{R}_n$) are supplied by the V_{CCA} rail.

The LCXZR164245 will remain in high impedance mode (outputs are disabled) when V_{CCA} and/or V_{CCB} is between 0 volts and 1.5 volts during power up. Placing the outputs in a high impedance (Z) state prevents intermittent low impedance loading or glitching in bus oriented applications.

To ensure the high impedance state during power up beyond a V_{CC} of 1.5V and also during power down, the $\overline{OE}_n$ pin should be tied to V_{CCA} through a pull up resistor. The minimum value of this resistor is determined by the current-sourcing capability of the device driving the $\overline{OE}_n$ pin.

Logic Diagrams





Note: Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

Symbol	Parameter	Value	Conditions	Units
V_{CCA}, V_{CCB}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0	$\overline{OE}$, T/$\overline{R}$ Control Pins	V
$V_{I/O}$	DC Output Voltage	−0.5 to +7.0	Outputs 3-STATE	V
		−0.5 to V_{CCA} +0.5	A Outputs in HIGH or LOW State (Note 3)	
		−0.5 to V_{CCB} +0.5	B Outputs in HIGH or LOW State (Note 3)	
I_{IK}	DC Input Diode Current	−50	V_I < GND ($\overline{OE}$, T/$\overline{R}$)	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		±50	V_O > V_{CC}	
I_O	DC Output Source or Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 4)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	V_{CCA}	2.3	3.6	V
		V_{CCB}	3.0	5.5	
V_I	Input Voltage @ $\overline{OE}$, T/$\overline{R}$		0	5.5	V
$V_{I/O}$	Output Voltage	A_n HIGH or LOW State	0	V_{CCA}	V
		B_n HIGH or LOW State	0	V_{CCB}	
		3-STATE	0	5.5	
T_A	Free Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V - 2.0V, V_{CCB} = 2.3V - 3.6V, V_{CCA} = 4.5V - 5.5V		0	10	ns/V

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Unused inputs or I/O's must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter		V_{CCA} (V)	V_{CCB} (V)	T_A = −40°C to +85°C		Units	Conditions
					Min	Max		
V_{IHA}	Minimum HIGH	A_n	2.3	3.0	2.0		V	
	Level Input		3.0	3.6	2.0			
	Voltage		3.6	5.5	2.0			
V_{IHB}		B_n	2.3	3.0	1.7			
		$\overline{OE}$	3.0	3.6	2.0			
		T/$\overline{R}$	3.6	5.5	2.0			
V_{ILA}	Maximum LOW	A_n	2.7	3.0		0.8	V	
	Level Input		3.0	3.6		0.8		
	Voltage		3.6	5.5		0.8		
V_{ILB}		B_n	2.7	3.0		0.7		
		OE	3.0	3.6		0.8		
		T/$\overline{R}$	3.6	5.5		0.8		

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CCA} (V)	V_{CCB} (V)	$T_A = -40°C$ to $+85°C$ Min	Max	Units	Conditions
V_{OHA}	Minimum HIGH Level Output Voltage		2.3	3.0	V_{CCA}–0.2		V	$I_{OUT} = -100\ \mu A$
			2.3	3.0	2.4			$I_{OH} = -4$ mA
			2.3	3.0	2.0			$I_{OH} = -12$ mA
			2.7	3.0	2.4			$I_{OH} = -4$ mA
			2.7	4.5	3.7			$I_{OH} = -12$ mA
V_{OHB}			2.3	3.0	V_{CCB}–0.2			$I_{OUT} = -100\ \mu A$
			2.3	3.0	1.8			$I_{OH} = -4$ mA
			2.3	4.5	2.2			$I_{OH} = -12$ mA
			3.0	4.5	2.2			$I_{OH} = -12$ mA
V_{OLA}	Maximum LOW Level Output Voltage		2.3	3.0		0.2	V	$I_{OUT} = 100\ \mu A$
			2.3	3.0		0.8		$I_{OL} = 12$ mA
			2.3	3.0		0.6		$I_{OL} = 4$ mA
			3.6	4.5		0.7		$I_{OL} = 12$ mA
V_{OLB}			3.0	3.0		0.2		$I_{OUT} = 100\ \mu A$
			2.3	3.0		0.6		$I_{OL} = 4$ mA
			3.0	4.5		0.8		$I_{OL} = 12$ mA
I_{IN}	Maximum Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$		3.6	3.6		±5.0	μA	$V_I = V_{CCB}$ or GND
			3.6	5.5				
I_{OZA}	Maximum 3-STATE Output Leakage @ A_n		3.6	3.6		±5.0	μA	$V_I = V_{IL}$, V_{IH}, $\overline{OE} = V_{CCB}$ $V_O = V_{CCA}$, GND
			3.6	5.5		±5.0		
I_{OZB}	Maximum 3-STATE Output Leakage @ B_n		3.6	3.6		±5.0	μA	$V_I = V_{IL}$, V_{IH}, $\overline{OE} = V_{CCB}$ $V_O = V_{CCB}$, GND
			3.6	5.5		±5.0		
ΔI_{CC}	Maximum I_{CC}/Input	B_n, $\overline{OE}$, T/$\overline{R}$	3.6	5.5		500	μA	$V_I = V_{CCB}$–0.6V
		A_n	3.6	5.5		2.0	mA	$V_I = V_{CCA}$–2.1V
I_{CCB1}	Quiescent V_{CCB} Supply Current as B Port Floats		3.6	Open		50	μA	$A_n = V_{CCA}$ or GND B_n = Open, $\overline{OE} = V_{CCA}$, T/$\overline{R} = V_{CCA}$, V_{CCB} = Open
I_{CCA2}	Quiescent V_{CCA} Supply Current		3.6	3.6		50	μA	$A_n = V_{CCA}$ or GND, $B_n = V_{CCB}$ or GND, $\overline{OE}$ = GND, T/$\overline{R}$ = GND
			3.6	5.5		80		
I_{CCB}	Quiescent V_{CCB} Supply Current		3.6	3.6		50	μA	$A_n = V_{CCA}$ or GND, $B_n = V_{CCB}$ or GND, $\overline{OE}$ = GND, T/$\overline{R} = V_{CCB}$
			3.6	5.5		50		
$I_{PU/PD}$	Power Up 3-STATE Output Current		0-1.5	0-1.5		±5.0	μA	V_O = 5V to V_{CC} V_I = GND or V_{CC}

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CCB} (V)	V_{CCA} (V)	$T_A = +25°C$ Typical	Units
V_{OLPB}	Quiet Output Dynamic Peak V_{OL}, A to B	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0$V	3.3	2.5	0.4	V
			5.0	3.3	0.4	
V_{OLPA}	Quiet Output Dynamic Peak V_{OL}, B to A	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0$V	3.3	2.5	0.4	V
			5.0	3.3	0.8	
V_{OLVB}	Quiet Output Dynamic Valley V_{OL}, A to B	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0$V	3.3	2.5	–0.4	V
			5.0	3.3	–0.4	
V_{OLVA}	Quiet Output Dynamic Valley V_{OL}, B to A	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0$V	3.3	2.5	–0.4	V
			5.0	3.3	–0.8	

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $V_{CCB} = 3.3V \pm 0.3V$, $V_{CCA} = 5.0V \pm 0.5V$		$T_A = -40°C$ to $+85°C$, $C_L = 30$ pF, $V_{CCB} = 2.5V \pm 0.2V$, $V_{CCA} = 5.0V \pm 0.5V$		Units
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay A to B	1.0	7.5	1.0	7.0	ns
t_{PHL} t_{PLH}	Propagation Delay B to A	1.0	7.5	1.0	7.0	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}$ to B	1.0	10.0	1.0	11.5	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}$ to A	1.0	10.0	1.0	11.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to B	1.0	10.5	1.0	11.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A	1.0	10.5	1.0	11.5	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 5) Data to Output		1.0		1.0	ns

Note 5: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Note: Typical values at $V_{CCA} = 3.3V$, $V_{CCB} = 5.0V$ @ 25°C.

Note: Typical values at $V_{CCA} = 3.3V$, $V_{CCB} = 3.3V$ @ 25°C.

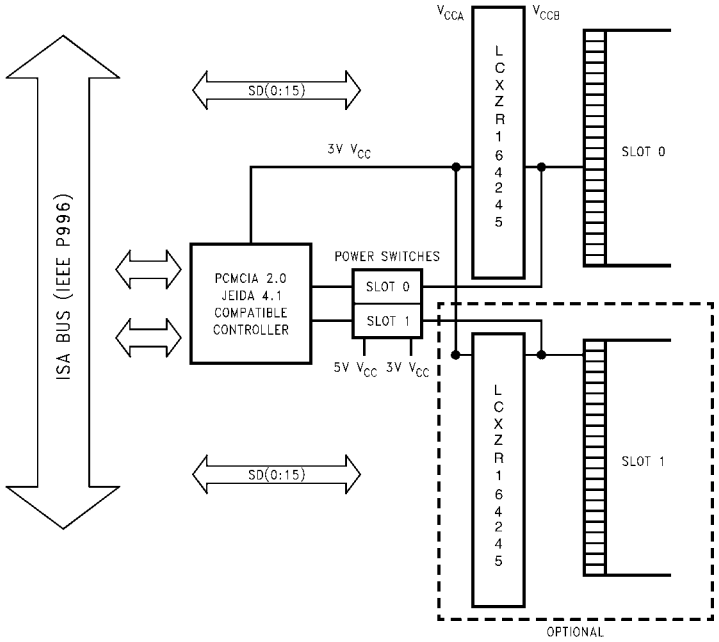
Capacitance

Symbol	Parameter		Typ	Units	Conditions
C_{IN}	Input Capacitance		4.5	pF	V_{CC} = Open
$C_{I/O}$	Input/Output Capacitance		10	pF	$V_{CCA} = 2.5V, 3.3V$ $V_{CCB} = 5.0V$
C_{PD}	Power Dissipation	A→B	40	pF	$V_{CCA} = 2.5V, 3.3V$
	Capacitance (Note 6)	B→A	65	pF	$V_{CCB} = 5.0V$

Note 6: C_{PD} is measured at 10 MHz.

I/O Application for PCMCIA Cards

Block Diagram

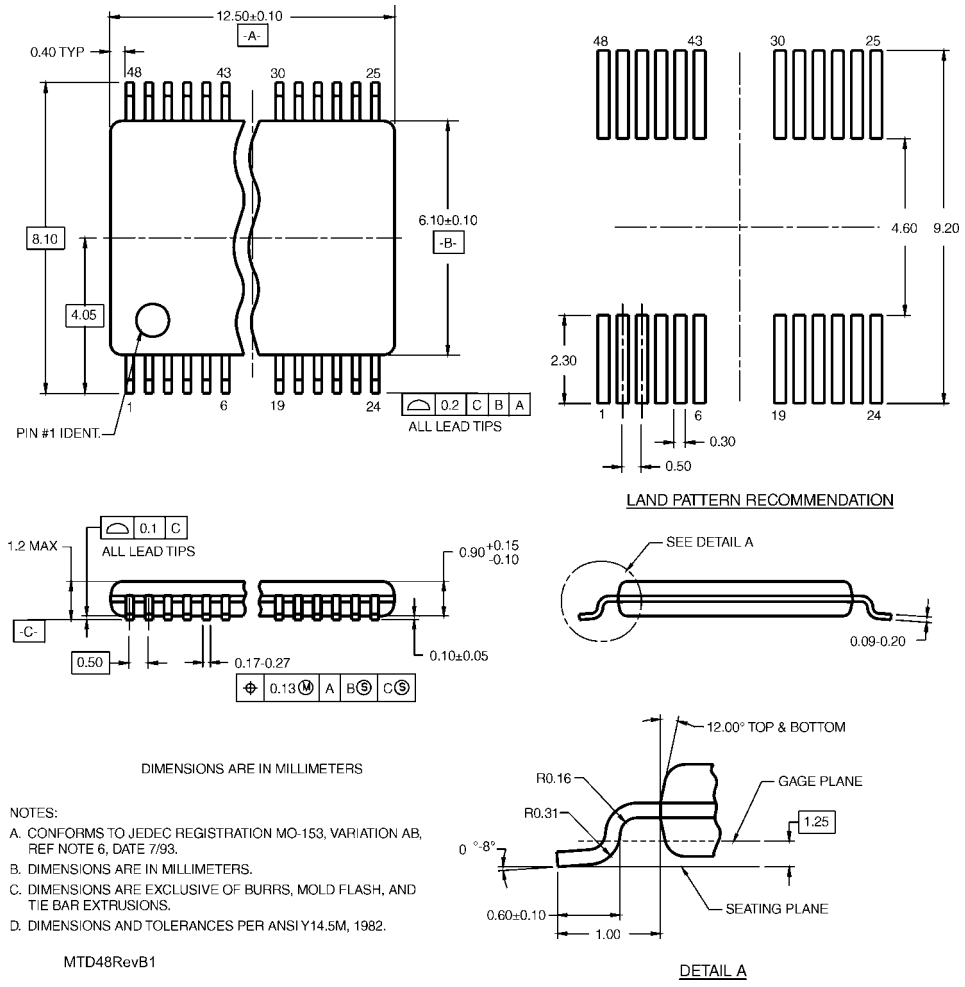


The LCXZR164245 is a 48-pin dual supply device well suited for PCMCIA I/O applications. Ideal for low power notebook designs, the LCXZR164245 consumes less than 1 mW of quiescent power in all modes of operation. The LCXZR164245 meets all PCMCIA I/O voltage requirements at 5V and 3.3V operation. By tying V_{CCA} of the LCXZR164245 to the card voltage supply, the PCMCIA card will always experience rail to rail output swings, maximizing the reliability of the interface.

The V_{CCA} pin on the LCXZR164245 must always be tied to a 3V power supply. This voltage connection provides internal references needed to account for variations in V_{CCB}. When connected as in the figure above, the LCXZR164245 meets all the voltage and current requirements of the ISA bus standard (IEEE P996).

Please reference Application Note AN-5001 for more detailed information on using Fairchild's LVX Low Voltage Dual Supply CMOS Translating Transceivers.

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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