ADVANCED

CY2DP814

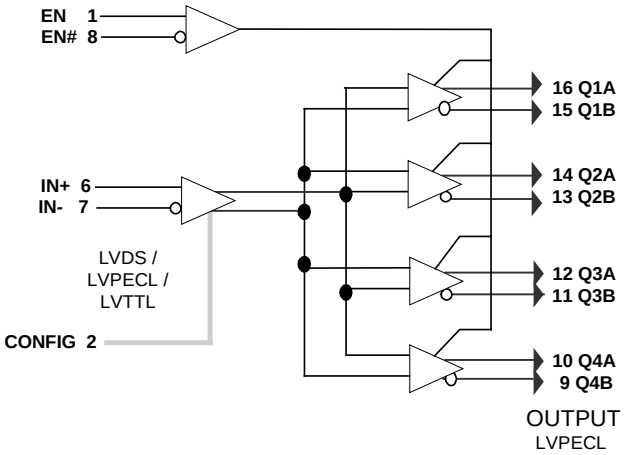
1:4 Clock Fanout Buffer

ComL™ SERIES

Product Features

- Low Voltage Operation
  V_{DD} = 3.3V
- 1:4 Fanout
- Single input configurable for
  LVDS, LVPECL or LVTTL
- 4 Differential pairs of LVPECL outputs.
- Drives 50 or 100 ohm load (Selectable)
- Low input capacitance
- Low output skew
- Low propagation delay
  Typical (tpd<4ns)
- Fmax=>400MHz
- Industrial Operation at 0°C to +85°C
- Packages available include: TSSOP / SSOP

Block Diagram



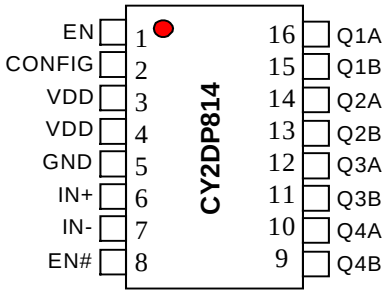
Product Description

The CYPRESS series of network circuits are produced using advanced 0.35-micron CMOS technology, achieving the industries fastest logic.

The CYPRESS CY2DP814 fanout buffer features a single LVDS or a single LVPECL compatible input and four LVPECL output pairs.

Designed for Data Communications clock management applications, the fanout from a single input reduces loading on the input clock.
The DP814 is ideal for both level translations from single ended to LVPECL and / or for the distribution of LVDS-based clock signals. The CYPRESS CY2DP814 has configurable input between logic families. The input can be selectable for LVPECL / LVTTL or LVDS signal. While the output driver's support LVPECL capable of driving 100 ohm lines.

Pin Configuration



16 pin TSSOP / SSOP

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http://www.cypress.com

Pin Description

Pin Number	Pin Name	Pin Interface Standard	Description
6,7	IN+,IN-	Configurable	Differential input pair or single line. LVPECL default. See CONFIG below.
3	V_{DD}	POWER	Positive Supply Voltage
2	CONFIG	LVTTL / LVCMOS	Converts inputs from the default LVPECL (logic = 0) to LDVS (logic = 1)
1,8	EN, EN#	LVPECL	Differential Output Enable Pair
16,15,14,13,12,11,10,9	Q1A, Q1B, Q2A, Q2B, Q3A, Q3B, Q4A, Q4B	LVPECL	Differential outputs.
4	V_{DD}	POWER	Positive Supply Voltage
5	GND	POWER	Ground

Absolute Maximum Ratings:

Storage Temperature	-65°C to 150°C
Ambient Temperature	0°C to +85°C
Supply Voltage to Ground Potential (Inputs and V_{DD} only)	-0.3V to 4.6V
Supply Voltage to Ground Potential (outputs only)	-0.3V to V_{DD}+0.3V
DC Input Voltage	-0.3V to V_{DD} +0.3V
DC Output Voltage	-0.3V to V_{DD} +3.9V
Power Dissipation	0.75W

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ	Max	Unit
I_{CCD}	Dynamic Power Supply Current	V_{DD} = Max Input toggling 50% Duty Cycle, Outputs Open	-	0.4	0.5	mA/MHz
I_C	Total Power Supply Current	V_{DD} = Max Input toggling 50% Duty Cycle, Outputs Open fL=100MHz	-	20	50	mA

LVDS Input D.C. Electrical Characteristics: @ 3.3V

D.C. Electrical Characteristics (Over the Operating Range , TA =0°C to +85°C, VDD=3.3V +/-5%							
Parameter	**Description**	**Test Conditions**		**Min.**	**Typ.**	**Max**	**Units**
$\lvert V_{ID} \rvert$	Magnitude of Differential Input Voltage			100		600	mV
$\lvert V_{IC} \rvert$	Common-Mode of Differential Input Voltage $\lvert V_{ID} \rvert$ (min&max)			$\lvert V_{ID} \rvert$ /2	2.4-($\lvert V_{ID} \rvert$ /2)		V
V_{IH}	Input High Voltage	Guaranteed Logic High Level	Config / Cntrl Pins	2			V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level				0.8	V
I_{IH}	Input High Current	V_{DD}=Max	$V_{IN}=V_{DD}$		+/-10	+/-20	uA
I_{IL}	Input Low Current	V_{DD}=Max	$V_{IN}=V_{SS}$		+/-10	+/-20	uA
I_I	Input High Current	V_{DD}=Max, $V_{IN}=V_{DD}$(max)				+/-20	uA

LVPECL Input D.C. Electrical Characteristics: @ 3.3V

D.C. Electrical Characteristics (Over the Operating Range , TA =0°C to +85°C, VDD=3.3V +/-5%							
Parameter	**Description**	**Test Conditions**		**Min.**	**Typ**	**Max**	**Units**
$\lvert V_{ID} \rvert$	Differential input voltage p-p	Guaranteed Logic High Level		400		2600	mV
V_{IH}	Input High Voltage	Guaranteed Logic High Level		2.15		2.4	V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level		1.5		1.8	V
I_{IH}	Input High Current	V_{DD}=Max	$V_{IN}=V_{DD}$		+/-10	+/-20	uA
I_{IL}	Input Low Current	V_{DD}=Max	$V_{IN}=V_{SS}$		+/-10	+/-20	uA
I_I	Input High Current	V_{DD}=Max., $V_{IN}=V_{DD}$(Max)				+/-20	uA

LVPECL OUTPUT D.C. Electrical Characteristics: @ 3.3V

D.C. Electrical Characteristics (Over the Operating Range , TA =0°C to +85°C, VDD=3.3V +/-5%							
Parameter	**Description**	**Test Conditions**		**Min.**	**Typ**	**Max**	**Units**
$\lvert V_{OD} \rvert$	Driver Differential Output voltage p-p	V_{DD}=Min., $V_{IN}=V_{IH}$ or V_{IL}	RL=75 ohm	1100		2200	mV
			RL=50 ohm	1100		2200	mV
$\lvert V_{OC} \rvert$	Driver common-mode p-p	V_{DD}=Min., $V_{IN}=V_{IH}$ or V_{IL}	RL=75 ohm		2100		mV
V_{OH}	Output High Voltage	V_{DD}=Min., $V_{IN}=V_{IH}$ or V_{IL}	I_{OH} = -12mA	1.8		2.4	V
V_{OL}	Output Low Voltage	V_{DD}=Min., $V_{IN}=V_{IH}$ or V_{IL}		1.2		1.7	V
I_{OS}	Short Circuit Current	V_{DD}=Max, V_{OUT} = GND				-50	mA

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AC Parameters @ 3.3V (DP814)

D.C. Electrical Characteristics (Over the Operating Range , TA =0°C to +85°C, VDD=3.3V +/-5%

Parameter	Description	Test Conditions		Min.	Typ	Max	Units
Risetime	Pin Control (pin 3) logic is "FALSE" defaulting to 100 ohm output drivers. Differential 20% to 80%	CL-10pF	RL=100 ohm	-	350	600	pS
Falltime		RL & CL to GND 3 CL=$C_{intrinsic}$ & $C_{external}$		-	350	600	pS

AC Parameters @ 3.3V (DP814B)

D.C. Electrical Characteristics (Over the Operating Range , TA =0°C to +85°C, VDD=3.3V +/-5%

Parameter	Description	Test Conditions		Min.	Typ	Max	Units
Risetime	Pin Control (pin 3) logic is "True" defaulting to 50 ohm output drivers. Differential 20% to 80%	CL-10pF	RL=50 ohm	-	350	600	pS
Falltime		RL & CL to GND 3 CL=$C_{intrinsic}$ & $C_{external}$	Output boost	-	350	600	pS

AC Switching Characteristics @ 3.3

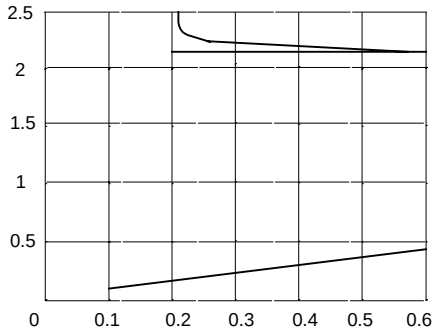
AC Switching Characteristics Over Operating Range TA =0°C to +85°C, VDD=3.3V +/-5%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TPLH	Propagation Delay – Low to High	VOD=100mV Figure 5	1.0	2.5	3.5	nS
TPHL	Propagation Delay – High to Low		1.0	2.5	3.5	nS
TPe	Enable (EN) to functional operation				6	nS
Tpd	Functional operation to Disable				5	nS
TSK(0)	Output Skew: Skew between outputs of the same package (in phase)		-	-	0.2	nS
TSK(p)	Pulse Skew: Skew between opposite transitions of the same output (TPHL – TPLH)		-	-	0.3	nS
TSK(t)	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type. Same input signal level and output load.	VID=100mV	-	-	1.6	nS

High Frequency Parametrics :

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Fmax	Maximum frequency VDD = 3.3V	50% duty cycle tW(50-50) Standard Load Circuit.	-	-	400	MHz
		50% duty cycle tW(50-50) The "point to point load circuit"	-	-	400	
Fmax(20)	Maximum frequency VDD = 3.3 V	20% duty cycle tW(20-80) The "point to point load circuit" Vin = 3.0V / 0.0V Vout = 2.3V / 0.4V	-	-	TBD	MHz
tW	Minimum pulse VDD = 3.3 V	The "point to point load circuit" Vin = 3.0V / 0.0V F= 100MHz Vout = 2.0V / 0.8V	TBD	-	-	nS

Common - Mode Input Voltage vs. DIfferential Voltage



Test Circuit & Voltage Definitions for the Differential Output Signal

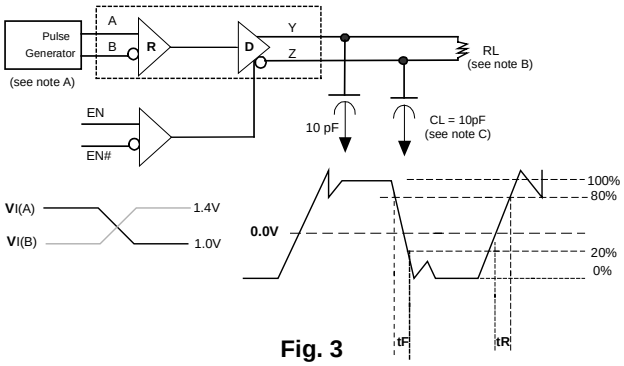


Fig. 3

Test Circuit & Voltage Definitions for the Driver Common-Mode Output Voltage

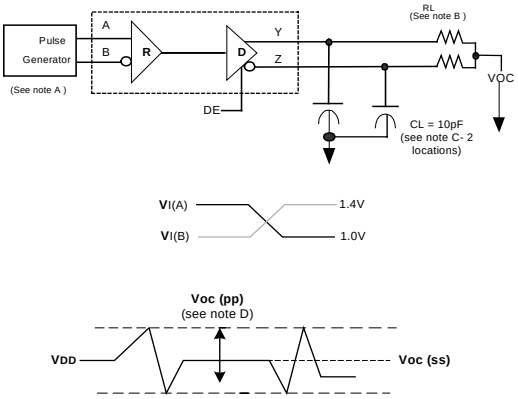


Fig. 4

Differential Receiver to Driver Propagation Delay and Driver Transition Time

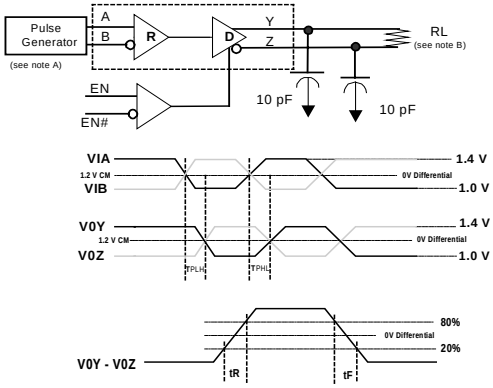


Fig.5

Test Circuit & Voltage Definitions for the Driver Common-Mode Output Voltage

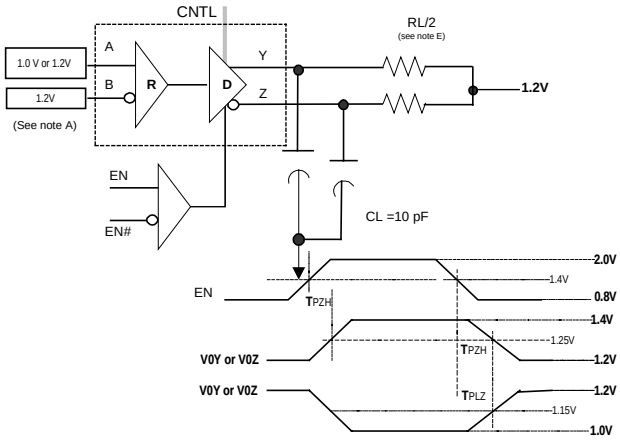


Fig. 6

Notes:

A: All input pulses are supplied by a frequency Generator
With the following characteristics:
t_R & $t_F \leq$ 1nS
Pulse rep rate = 50 MppS
Pulse width = 10 ± 0.2nS

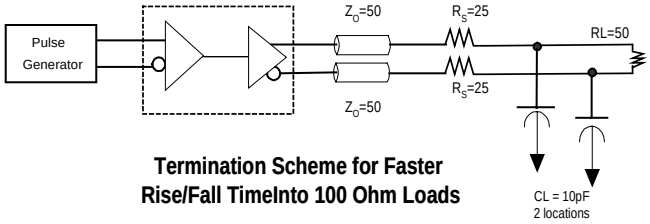
B: RL-100 ohm/50 ohm ±1%

C: CL includes instrumentation and fixture capacitance within 6mm of the DUT

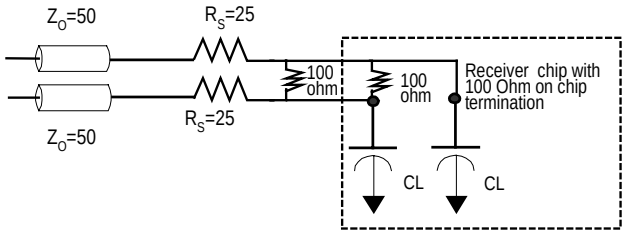
D: VOC measurement requires equipment with a 3dB Bandwidth of at least 300MHz.

E: RL-100 ohm/50 ohm ±1% via CNTL

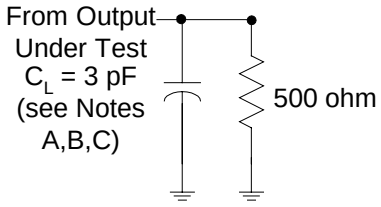
Application Engineering



Termination Scheme for Faster Rise/Fall TimeInto 100 Ohm Loads



Termination Scheme for100 ohm Self Terminating Interface Chip

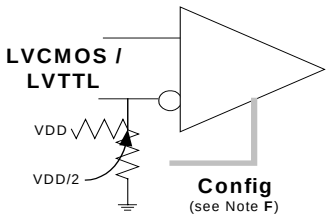


Point to Point Load Circuit

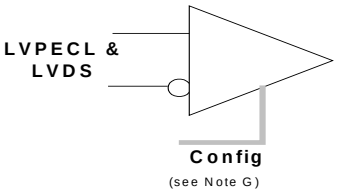
I/O Configuration Options

Input Configurations:

F. LVCMOS / LVTTL single ended input.
G. LVPECL or LVDS differential input.



0	LVPECL



0	LVPECL
1	LVDS

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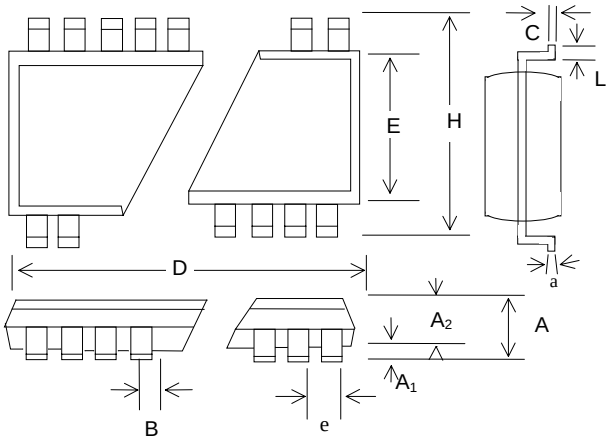
Package Drawing and Dimensions



16 Pin TSSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
B	0.007	-	0.012	0.19	-	0.30
C	0.004	-	0.008	0.09	-	0.20
D	0.193	0.197	0.201	4.90	5.00	5.10
E	0.169	0.173	0.177	4.30	4.40	4.50
e	0.02559 BSC			0.65 BSC		
H	0.244	0.252	0.260	6.20	6.40	6.60
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0º	-	8º	0º	-	8º

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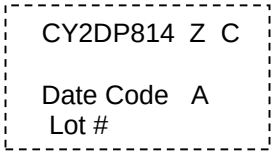
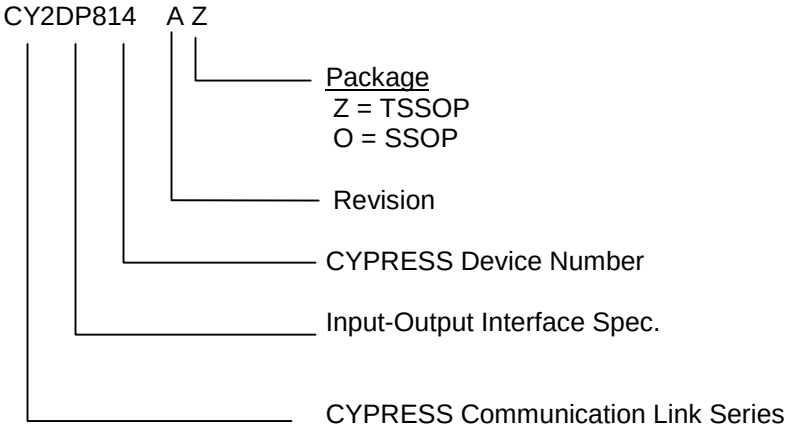
Ordering Information

Part Number	Package Type
CY2DP814Z	16 Pin TSSOP
CY2DP814O	16 Pin SSOP

Note: the ordering part number is formed by a combination of device number, package and screening as shown below.

Marking: Example:





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Document Title: CY2DP814 1:4 Clock Fanout Buffer **Document Number**: 38-07060				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107085	06/07/01	IKA	Convert from IMI to Cypress