



Integrated Device Technology, Inc.

FAST CMOS 8-INPUT MULTIPLEXER

IDT54/74FCT151T/AT/CT
IDT54/74FCT251T/AT/CT

FEATURES:

- IDT54/74FCT151T/251T equivalent to FAST™ speed and drive
- IDT54/74FCT151AT/251AT 25% faster than FAST
- IDT54/74FCT151CT/251CT 50% faster than FAST
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- TTL input and output level compatible
 - $V_{OH} = 3.3V$ (typ.)
 - $V_{OL} = 0.3V$ (typ.)
- $I_{OL} = 48mA$ (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

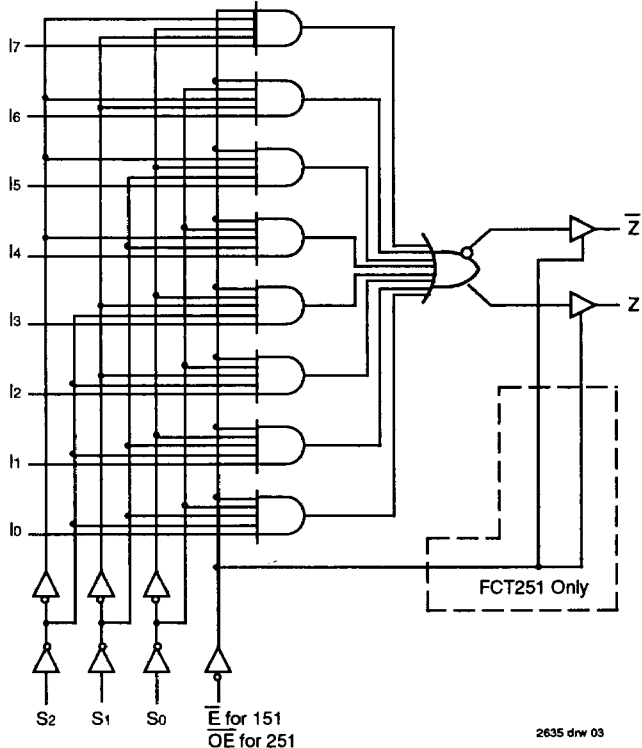
DESCRIPTION:

The IDT54/74FCT151T/AT/CT and IDT54/74FCT251T/AT/CT are high-speed 8-input multiplexers built using advanced CEMOS™, a dual metal CMOS technology. They select one bit of data from up to eight sources under the control of three select inputs. Both assertion and negation outputs are provided.

The IDT54/74FCT151T/AT/CT has a common Active-LOW enable (\bar{E}) input. When \bar{E} is LOW, data from one of eight inputs is routed to the complementary outputs according to the 3-bit code applied to the Select (S_0 - S_2) inputs. A common application of the 'FCT151 is data routing from one of eight sources.

The IDT54/74FCT251T/AT/CT has a common Active-LOW Output Enable (\bar{OE}) input. When \bar{OE} is LOW, data from one of eight inputs is routed to the complementary outputs. When \bar{OE} is HIGH, both outputs are in the high-impedance state. This feature allows multiplexer expansion by tying several outputs together.

FUNCTIONAL BLOCK DIAGRAM



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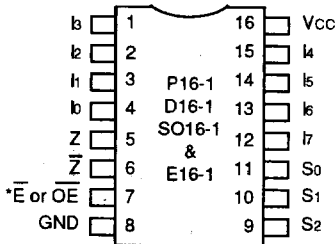
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FAST is a trademark of National Semiconductor Co.

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

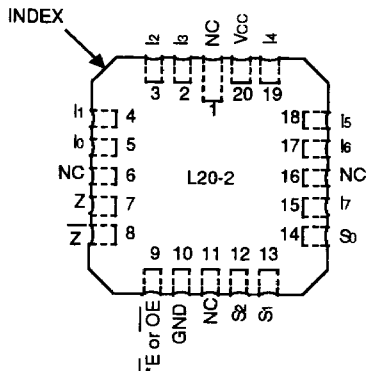
MAY 1992

PIN CONFIGURATIONS



**DIP/SOIC/CERPACK
TOP VIEW**

2635 drw 01



**LCC
TOP VIEW**

2635 drw 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc	-0.5 to Vcc	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

NOTES:

2635 tbl 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
- Input and Vcc terminals only.
- Outputs and I/O terminals only.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

NOTE:

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- This parameter is measured at characterization but not tested.

*E for 151 only. OE for 251 only.

PIN DESCRIPTION

Pin Names	Description
I0 - I7	Data Inputs
S0 - S2	Selects Inputs
E	Enable Input (Active LOW)-FCT151
OE	Output Enable Input (Active LOW)-FCT251
Z	Data Output
Z-bar	Inverted Data Output

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FUNCTION TABLE⁽²⁾

Inputs				Outputs	
S2	S1	S0	E/OE ⁽¹⁾	Z	Z-bar
X	X	X	H	L(151)	H(151)
X	X	X	H	Z(251)	Z(251)
L	L	L	L	I0	I0
L	L	H	L	I1	I1
L	H	L	L	I2	I2
L	H	H	L	I3	I3
H	L	L	L	I4	I4
H	L	H	L	I5	I5
H	H	L	L	I6	I6
H	H	H	L	I7	I7

NOTES:

2635 tbl 02

- E for 151, OE for 251.
- H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't care, Z = High Impedance.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = 0°C to +70°C, VCC = 5.0V ± 5%; Military: TA = -55°C to +125°C, VCC = 5.0V ± 10%

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max.	V _I = 2.7V	—	—	5	μA
I _{IL}	Input LOW Current	V _{CC} = Max.	V _I = 0.5V	—	—	-5	μA
I _{OZH}	High Impedance Output Current	V _{CC} = Max.	V _O = 2.7V	—	—	10	μA
I _{OZL}			V _O = 0.5V	—	—	-10	μA
I _I	Input HIGH Current	V _{CC} = Max., V _I = V _{CC} (Max.)		—	—	20	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _N = -18mA		—	-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _O = GND		-60	-120	-225	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -6mA MIL. I _{OH} = -8mA COM'L.	2.4	3.3	—	V
			I _{OH} = -12mA MIL. I _{OH} = -15mA COM'L.	2.0	3.0	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 32mA MIL. I _{OL} = 48mA COM'L.	—	0.3	0.5	V
V _H	Input Hysteresis	—		—	200	—	mV
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} = GND or V _{CC}		—	0.2	1.5	mA

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open E or OE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁵⁾	V _{CC} = Max. Outputs Open f _i = 10MHz 50% Duty Cycle E or OE = GND One Input Toggling	V _{IN} = V _{CC} V _{IN} = GND	—	3.2	6.5	mA
			V _{IN} = 3.4V V _{IN} = GND	—	3.5	7.5	

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_iN_O)
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_O = Number of Outputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE – IDT54/74FCT151T/AT/CT

Symbol	Parameter	Condition(1)	IDT54/74FCT151T				IDT54/74FCT151AT				IDT54/74FCT151CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	
tPLH tPHL	Propagation Delay SN to Z	CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	6.6	1.5	7.4	1.5	5.6	1.5	6.2	ns
tPLH tPHL	Propagation Delay SN to Z		1.5	10.5	1.5	11.5	1.5	6.8	1.5	7.6	1.5	5.8	1.5	6.5	ns
tPLH tPHL	Propagation Delay E to Z		1.5	7.0	1.5	7.5	1.5	5.6	1.5	6.3	1.5	4.8	1.5	5.4	ns
tPLH tPHL	Propagation Delay E to Z		1.5	9.5	1.5	11.0	1.5	5.8	1.5	6.6	1.5	5.0	1.5	5.7	ns
tPLH tPHL	Propagation Delay IN to Z		1.5	6.5	1.5	7.5	1.5	5.2	1.5	5.8	1.5	4.4	1.5	4.9	ns
tPLH tPHL	Propagation Delay IN to Z		1.5	7.5	1.5	9.0	1.5	5.5	1.5	6.1	1.5	4.7	1.5	5.2	ns
tPLH tPHL	Propagation Delay IN to Z		1.5	7.5	1.5	9.0	1.5	5.5	1.5	6.1	1.5	4.7	1.5	5.2	ns

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE – IDT54/74FCT251T/AT/CT

Symbol	Parameter	Condition(1)	IDT54/74FCT251T				IDT54/74FCT251AT				IDT54/74FCT251CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	
tPLH tPHL	Propagation Delay SN to Z	CL = 50pF RL = 500Ω	1.5	9.0	1.5	9.5	1.5	6.6	1.5	7.4	1.5	5.6	1.5	6.2	ns
tPLH tPHL	Propagation Delay SN to Z		1.5	11.0	1.5	14.0	1.5	6.8	1.5	7.6	1.5	5.8	1.5	6.5	ns
tPLH tPHL	Propagation Delay IN to Z		1.5	7.0	1.5	8.0	1.5	5.2	1.5	5.8	1.5	4.4	1.5	4.9	ns
tPLH tPHL	Propagation Delay IN to Z		1.5	7.0	1.5	8.0	1.5	5.5	1.5	6.1	1.5	4.7	1.5	5.2	ns
tPZH tPZL	Output Enable Time OE to Z		1.5	9.0	1.5	10.0	1.5	6.7	1.5	7.4	1.5	5.7	1.5	6.3	ns
tPHZ tPLZ	Output Disable Time OE to Z		1.5	7.5	1.5	8.5	1.5	6.0	1.5	6.4	1.5	5.0	1.5	5.4	ns
tPZH tPZL	Output Enable Time OE to Z		1.5	9.0	1.5	10.0	1.5	6.7	1.5	7.6	1.5	5.7	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time OE to Z		1.5	7.0	1.5	7.0	1.5	6.0	1.5	6.3	1.5	5.0	1.5	5.2	ns
tPZH tPZL	Output Enable Time OE to Z		1.5	9.0	1.5	10.0	1.5	6.7	1.5	7.6	1.5	5.7	1.5	6.5	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

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