

P54/74FCT138T–P54/74FCT138AT P54/74FCT138CT HIGH SPEED 1-OF-8 DECODER



FEATURES

- Function, Pinout and Drive Compatible with the FCT and F Logic
- FCT-C speed at 4.7ns max. (Com'I)
FCT-A speed at 5.8ns max. (Com'I)
- Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Power-off disable feature
- Matched Rise and Fall times
- Fully Compatible with TTL Input and Output Logic Levels
- 64 mA Sink Current (Com'I), 32 mA (Mil)
15 mA Source Current (Com'I), 12 mA (Mil)
- Dual 1-Of-8 Decoder with Enables
- Manufactured in 0.7 micron PACE Technology™



DESCRIPTION

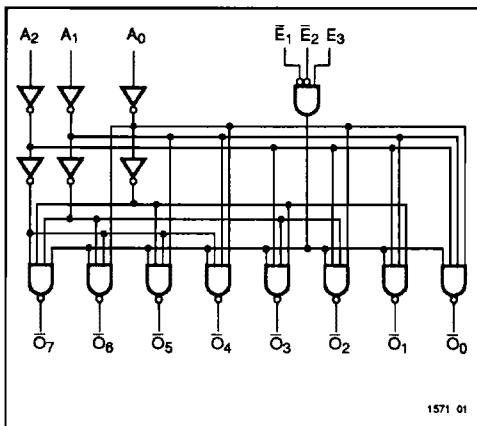
The 'FCT138T are 1-of-8 decoders. The 'FCT138T accepts three binary weighted inputs (A_0 , A_1 , A_2) and, when enabled, provides eight mutually exclusive active LOW outputs ($\bar{O}_0 - \bar{O}_7$). The 'FCT138T features three enable inputs, two active LOW (\bar{E}_1 , \bar{E}_2) and one active HIGH (E_3). All outputs will be HIGH unless \bar{E}_1 and \bar{E}_2 are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 'FCT138T devices and one inverter.

The 'FCT138T is manufactured using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.7 micron effective channel lengths giving 400 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

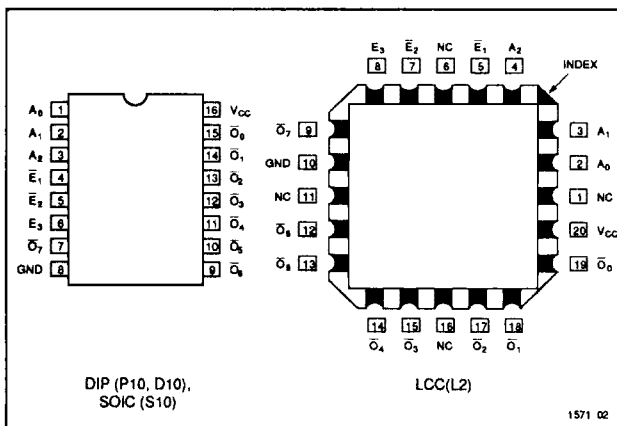
*For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V.



FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS





ABSOLUTE MAXIMUM RATINGS^{1,2}

Symbol	Parameter	Value	Unit
T _{STG}	Storage Temperature	-65 to +150	°C
T _A	Ambient Temperature Under Bias	-65 to +135	°C
V _{CC}	V _{CC} Potential to Ground	-0.5 to +7.0	V
P _T	Power Dissipation	0.5	W

1571 Tbl 01

Symbol	Parameter	Value	Unit
I _{OUTPUT}	Current Applied to Output	120	mA
V _{IN}	Input Voltage	-0.5 to +7.0	V
V _{OUT}	Voltage Applied to Output	-0.5 to +7.0	V

1571 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	-55°C	+125°C
Commercial	0°C	+70°C

1571 Tbl 03

Supply Voltage (V _{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1571 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter	Min	Typ ¹	Max	Units	V _{CC}	Conditions	
V _{IH}	Input HIGH Voltage	2.0			V			
V _{IL}	Input LOW Voltage			0.8	V			
V _H	Hysteresis		0.2		V		All inputs	
V _{IK}	Input Clamp Diode Voltage		-0.7	-1.2	V	MIN	I _{IN} = -18mA	
V _{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I _{OH} = -12mA
		Commercial	2.4	3.3		V	MIN	I _{DH} = -15mA
V _{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I _{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I _{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I _{OL} = 64mA
I _I	Input HIGH Current			20	μA	MAX	V _{IN} = V _{CC}	
I _{IH}	Input HIGH Current			5	μA	MAX	V _{IN} = 2.7V	
I _{IL}	Input LOW Current			-5	μA	MAX	V _{IN} = 0.5V	
I _{OS}	Output Short Circuit Current ²	-60	-120	-225	mA	MAX	V _{OUT} = 0.0V	
I _{OFF}	Power-off Disable			100	μA	0V	V _{OUT} = 4.5V	
C _{IN}	Input Capacitance ³		5	10	pF	MAX	All inputs	
C _{OUT}	Output Capacitance ³		9	12	pF	MAX	All outputs	
I _{CC}	Quiescent Power Supply Current		0.2	1.5	mA	MAX	V _{IN} ≤ 0.2V, V _{IN} ≥ V _{CC} - 0.2V	

1571 Tbl 05

Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ ¹	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 3.4V^2$, $f_1 = 0$, Outputs Open
I_{CCD}	Dynamic Power Supply Current ³	0.15	0.3	mA/ mHz	$V_{CC} = \text{MAX}$, One Input Toggling, 50% Duty Cycle, Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current ⁵	1.7	4.5	mA	$V_{CC} = \text{MAX}$, $f_1 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, Toggle \bar{E}_1 , \bar{E}_2 or E_3 , One Output Toggling, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.0	5.5	mA	$V_{CC} = \text{MAX}$, $f_1 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, Toggle \bar{E}_1 , \bar{E}_2 or E_3 , One Output Toggling, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$

1571 Tbl 06

Notes:

1. Typical values are at $V_{CC} = 5.0V$, +25°C ambient.
2. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + I_{CC} D_H N_T + I_{CCD} (f_1/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)

- D_H = Duty Cycle for TTL Inputs High
 - N_T = Number of TTL Inputs at D_H
 - I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 - f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 - f_1 = Output Frequency
 - N_1 = Number of Inputs at f_1
- All currents are in milliamperes and all frequencies are in megahertz.



TRUTH TABLE

Inputs						Outputs							
\bar{E}_1	\bar{E}_2	E_3	A_0	A_1	A_2	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3	\bar{O}_4	\bar{O}_5	\bar{O}_6	\bar{O}_7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	L	H	H	H
L	L	H	L	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level, L=LOW Voltage Level, X=Don't Care

1571 Tbl 07



AC CHARACTERISTICS

Sym	Parameter	'FCT138T				'FCT138AT				'FCT138CT				Units	Fig. No.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.		
t_{PLH} t_{PHL}	Prop Delay A_0 to \bar{O}_n	1.5	12.0	1.5	9.0	1.5	7.8	1.5	5.8	1.5	6.0	1.5	4.7	ns	1, 5
t_{PLH} t_{PHL}	Prop Delay \bar{E}_1 or \bar{E}_2 to \bar{O}_n	1.5	12.5	1.5	9.0	1.5	8.0	1.5	5.9	1.5	6.5	1.5	5.0	ns	1, 5
t_{PLH} t_{PHL}	Prop Delay E_3 to \bar{O}_n	1.5	12.5	1.5	9.0	1.5	8.0	1.5	5.9	1.5	6.5	1.5	5.0	ns	1, 5

1571 Tbl 08

Note:

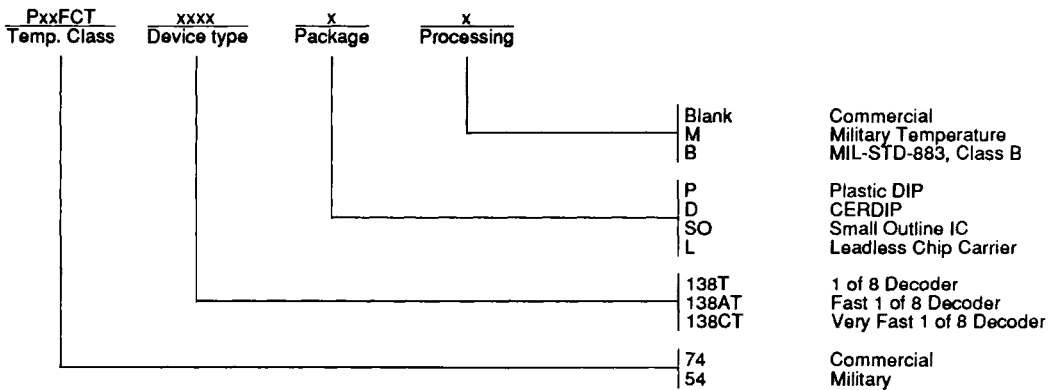
1. Minimum limits are guaranteed but not tested on Propagation Delays.

DEFINITION OF FUNCTIONAL TERMS

PIN Names	Description
$A_0 - A_2$	Address Inputs
$\bar{E}_1 - \bar{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
$\bar{O}_0 - \bar{O}_7$	Outputs (Active LOW)

1571 Tbl 08

ORDERING INFORMATION



1571 03