# 1.8V CMOS 16-BIT BUFFER/ DRIVER WITH INVERTED 3-STATE OUTPUTS

**IDT74AUC16240**

## FEATURES:

- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **1.8V Optimized**
- **0.8V to 2.7V Operating Range**
- **Inputs/outputs tolerant up to 3.6V**
- **±9mA @ 2.3V output drivers**
- **Supports hot insertion**
- **Available in TSSOP, TVSOP, and VFBGA packages**

## APPLICATIONS:

- **high performance, low voltage communications systems**
- **high performance, low voltage computing systems**

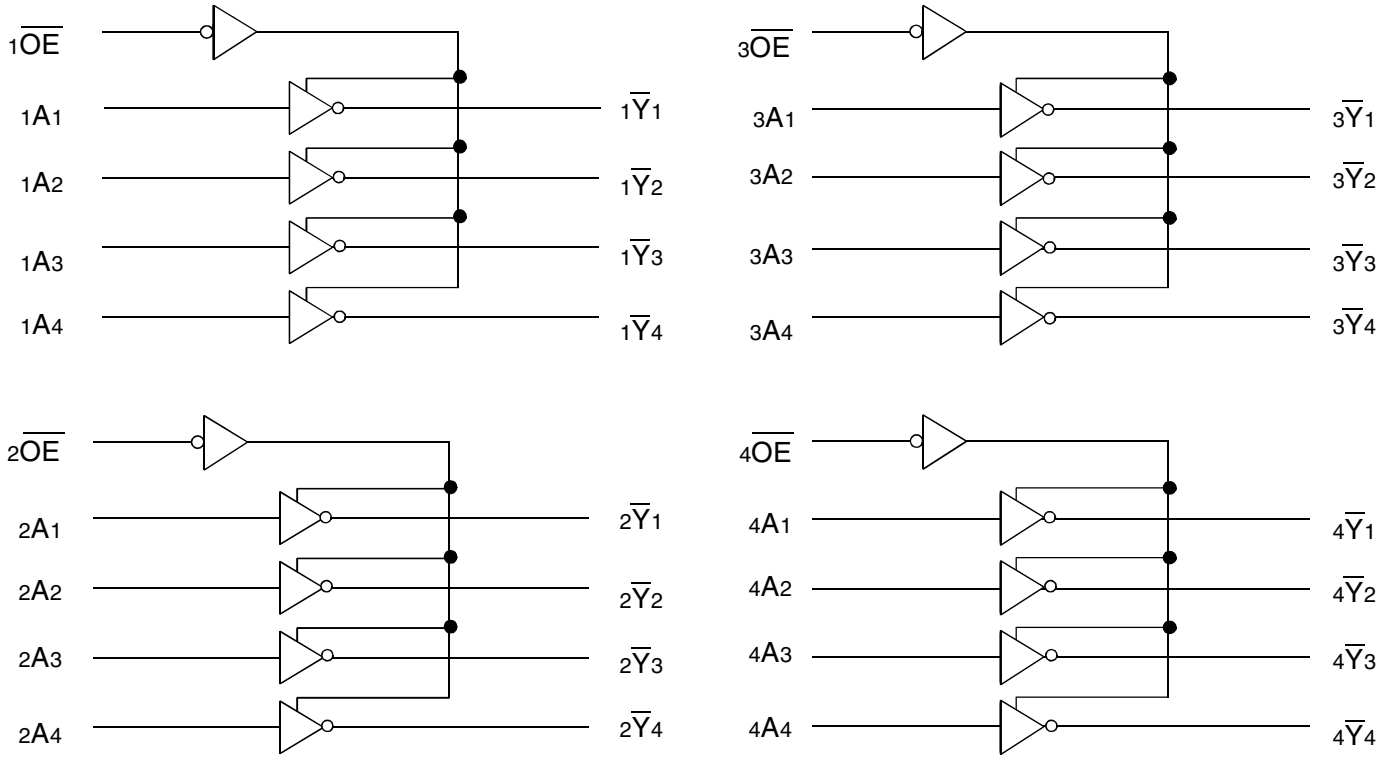
## DESCRIPTION:

This 16-bit buffer/driver is built using advanced CMOS technology. The AUC16240 is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented recievers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides inverted outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

This device is fully specified for partial power-down applications using $I_{OFF}$. The $I_{OFF}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{DD}$ through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## FUNCTIONAL BLOCK DIAGRAM



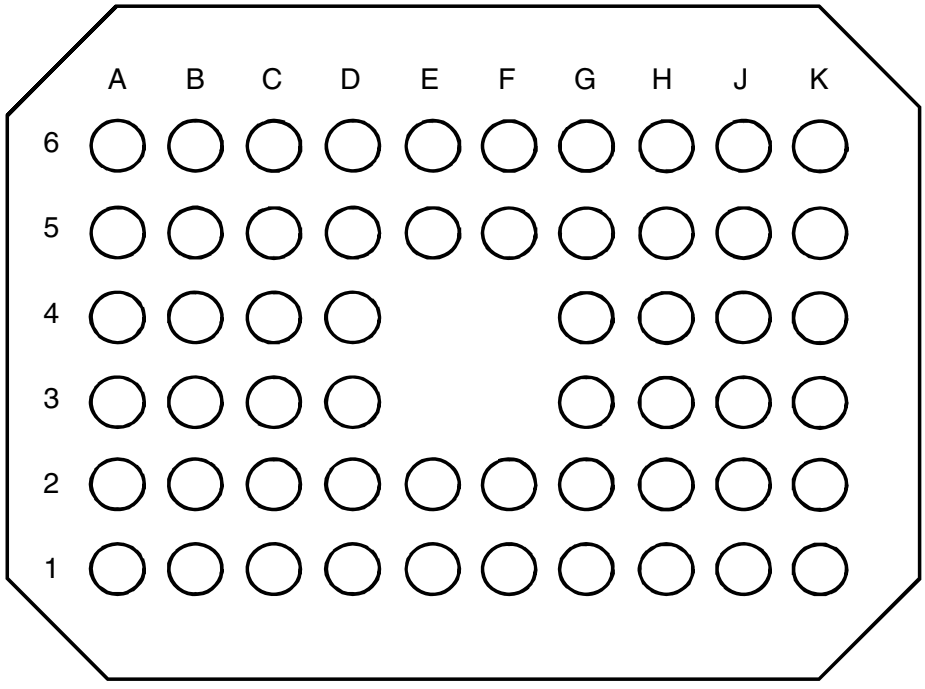
## PINOUT CONFIGURATION

| | A | B | C | D | E | F | G | H | J | K |
|---|---|---|---|---|---|---|---|---|---|---|
| 6 | $2\overline{OE}$ | 1A2 | 1A4 | 2A2 | 2A4 | 3A1 | 3A3 | 4A1 | 4A3 | $3\overline{OE}$ |
| 5 | NC | 1A1 | 1A3 | 2A1 | 2A3 | 3A2 | 3A4 | 4A2 | 4A4 | NC |
| 4 | NC | GND | $V_{DD}$ | GND | | | GND | $V_{DD}$ | GND | NC |
| 3 | NC | GND | $V_{DD}$ | GND | | | GND | $V_{DD}$ | GND | NC |
| 2 | NC | $1\overline{Y}1$ | $1\overline{Y}3$ | $2\overline{Y}1$ | $2\overline{Y}3$ | $3\overline{Y}2$ | $3\overline{Y}4$ | $4\overline{Y}2$ | $4\overline{Y}4$ | NC |
| 1 | $1\overline{OE}$ | $1\overline{Y}2$ | $1\overline{Y}4$ | $2\overline{Y}2$ | $2\overline{Y}4$ | $3\overline{Y}1$ | $3\overline{Y}3$ | $4\overline{Y}1$ | $4\overline{Y}3$ | $4\overline{OE}$ |

**VFBGA**

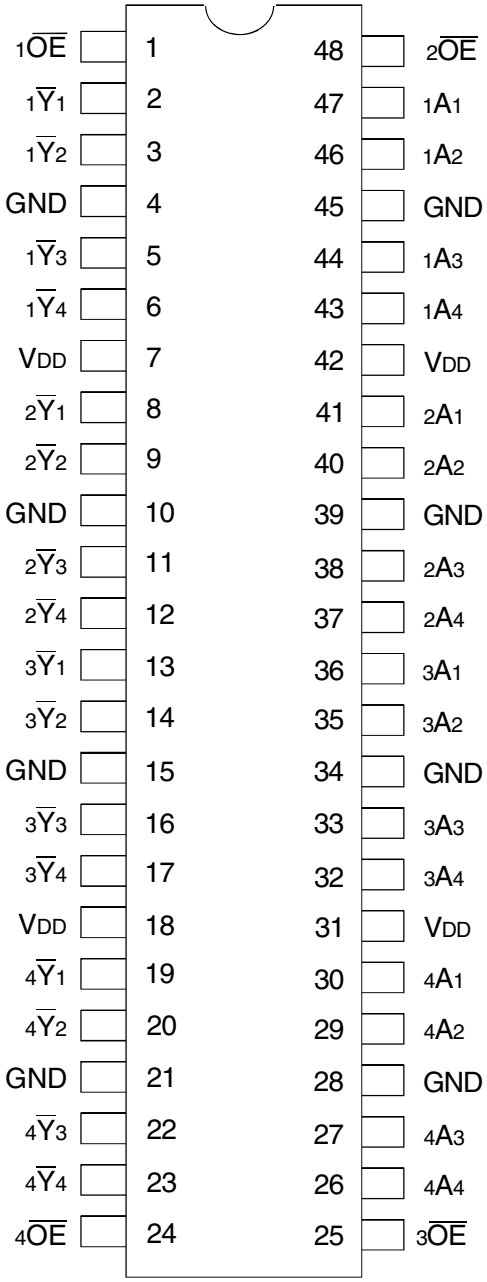
**NOTE:**
NC = No Internal Connection

## 56 BALL VFBGA PACKAGE LAYOUT




**TOP VIEW**

## PIN CONFIGURATION




**TSSOP/ TVSOP**
**TOP VIEW**

## PIN DESCRIPTION

| Pin Names | Description |
|---|---|
| x$\overline{OE}$ | 3-State Output Enable Inputs (Active Low) |
| xAx | Data Inputs |
| x$\overline{Y}$x | 3-State Outputs |

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Description | Max | Unit |
|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND (all input and $V_{DD}$ terminals) | –0.5 to +3.6 | V |
| $V_{TERM}$ | Terminal Voltage with Respect to GND (any I/O or Output terminals in high-impedance or power-off state) | –0.5 to +3.6 | V |
| $V_{TERM}$ | Terminal Voltage with Respect to GND (any I/O or Output terminals in high or low state) | –0.5 to +3.6 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | ° C |
| $I_{OUT}$ | Continuous DC Output Current | ±20 | mA |
| $I_{IK}$ | Continuous Clamp Current, $V_I < 0$, or $V_I > V_{DD}$ | ±50 | mA |
| $I_{OK}$ | Continuous Clamp Current, $V_O < 0$ | –50 | mA |
| $I_{DD}$ $I_{SS}$ | Continuous Current through each $V_{DD}$ or GND | ±100 | mA |

**NOTE:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz, $V_{DD}$ = 2.5V)

| Symbol | Parameter | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$(1) | Input Capacitance | $V_{IN}$ = 0V | 3 | 4 | pF |
| $C_{OUT}$(2) | Output Capacitance | $V_{OUT}$ = 0V | 5.5 | 6 | pF |
| $C_I$(3) | Input Port Capacitance | $V_{IN}$ = 0V | 3 | 4 | pF |

**NOTES:**
1. Applies to Control Inputs.
2. Applies to Data Outputs.
3. Applies to Data Inputs.

## FUNCTION TABLE (EACH 4-BIT BUFFER)(1)

| Inputs | | Output |
|---|---|---|
| x$\overline{OE}$ | xAx | x$\overline{Y}$x |
| L | H | L |
| L | L | H |
| H | X | Z |

**NOTE:**
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance

## RECOMMENDED OPERATING CHARACTERISTICS(1)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | 0.8 | 2.7 | V |
| $V_{IH}$ | Input HIGH Voltage Level | $V_{DD}$ = 0.8V | $V_{DD}$ | — | V |
| | | $V_{DD}$ = 1.1V to 1.3V | 0.65 x $V_{DD}$ | — | |
| | | $V_{DD}$ = 1.4V to 1.6V | 0.65 x $V_{DD}$ | — | |
| | | $V_{DD}$ = 1.65V to 1.95V | 0.65 x $V_{DD}$ | — | |
| | | $V_{DD}$ = 2.3V to 2.7V | 1.7 | — | |
| $V_{IL}$ | Input LOW Voltage Level | $V_{DD}$ = 0.8V | — | 0 | V |
| | | $V_{DD}$ = 1.1V to 1.3V | — | 0.35 x $V_{DD}$ | |
| | | $V_{DD}$ = 1.4V to 1.6V | — | 0.35 x $V_{DD}$ | |
| | | $V_{DD}$ = 1.65V to 1.95V | — | 0.35 x $V_{DD}$ | |
| | | $V_{DD}$ = 2.3V to 2.7V | — | 0.7 | |
| $V_I$ | Input Voltage | | 0 | 2.7 | V |
| $V_O$ | Output Voltage | Active State | 0 | $V_{DD}$ | V |
| | | 3-State | 0 | 2.7 | |
| $I_{OH}$ | HIGH Level Output Current | $V_{DD}$ = 0.8V | — | –0.7 | mA |
| | | $V_{DD}$ = 1.1V | — | –3 | |
| | | $V_{DD}$ = 1.4V | — | –5 | |
| | | $V_{DD}$ = 1.65V | — | –8 | |
| | | $V_{DD}$ = 2.3V | — | –9 | |
| $I_{OL}$ | LOW Level Output Current | $V_{DD}$ = 0.8V | — | 0.7 | mA |
| | | $V_{DD}$ = 1.1V | — | 3 | |
| | | $V_{DD}$ = 1.4V | — | 5 | |
| | | $V_{DD}$ = 1.65V | — | 8 | |
| | | $V_{DD}$ = 2.3V | — | 9 | |
| $\Delta t/\Delta v$ | Input Transition Rise or Fall Rate | $V_{DD}$ = 0.8V to 1.3V | — | 20 | ns/V |
| | | $V_{DD}$ = 1.6V to 1.95V | — | 10 | |
| | | $V_{DD}$ = 2.7V | — | 5 | |
| $T_A$ | Operating Free-Air Temperature | | –40 | +85 | °C |

**NOTE:**
1. All unused inputs of the device must be held at $V_{DD}$ or GND to ensure proper operation.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE(1)

Following Conditions Apply Unless Otherwise Specified:
Operating Conditions: $T_A$ = –40°C to +85°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{IH}$<br>$I_{IL}$ | Input HIGH or LOW Current<br>All Inputs | $V_{DD}$ = 2.7V, $V_I$ = $V_{DD}$ or GND | | — | — | ±5 | µA |
| $I_{OFF}$ | Input/Output Power Off Leakage | $V_{DD}$ = 0V, $V_{IN}$ or $V_O \leq$ 2.7V | | — | — | ±10 | µA |
| $I_{OZH}$ | High Impedance Output Current | $V_{DD}$ = 2.7V | $V_O$ = $V_{DD}$ | — | — | ±10 | µA |
| $I_{OZL}$ | (3-State Output Pins) | | $V_O$ = GND | — | — | ±10 | |
| $I_{DDL}$<br>$I_{DDH}$<br>$I_{DDZ}$ | Quiescent Power Supply Current | $V_{DD}$ = 0.8V to 2.7V<br>$V_{IN}$ = GND or $V_{DD}$ | | — | — | 20 | µA |

**NOTE:**
1. All unused inputs of the device must be held at $V_{DD}$ or GND to ensure proper operation.

## OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{DD}$ = 0.8V - 2.7V | $I_{OH}$ = –100µA | $V_{DD}$ - 0.1 | — | — | V |
| | | $V_{DD}$ = 0.8V | $I_{OH}$ = –0.7mA | — | 0.55 | — | |
| | | $V_{DD}$ = 1.1V[2] | $I_{OH}$ = –3mA | 0.8 | — | — | |
| | | $V_{DD}$ = 1.4V[3] | $I_{OH}$ = –5mA | 1 | — | — | |
| | | $V_{DD}$ = 1.65V[4] | $I_{OH}$ = –8mA | 1.2 | — | — | |
| | | $V_{DD}$ = 2.3V[5] | $I_{OH}$ = –9mA | 1.8 | — | — | |
| $V_{OL}$ | Output LOW Voltage | $V_{DD}$ = 0.8V - 2.7V | $I_{OH}$ = 100µA | — | — | 0.2 | V |
| | | $V_{DD}$ = 0.8V | $I_{OL}$ = 0.7mA | — | 0.25 | — | |
| | | $V_{DD}$ = 1.1V[2] | $I_{OL}$ = 3mA | — | — | 0.3 | |
| | | $V_{DD}$ = 1.4V[3] | $I_{OL}$ = 5mA | — | — | 0.4 | |
| | | $V_{DD}$ = 1.65V[4] | $I_{OL}$ = 8mA | — | — | 0.45 | |
| | | $V_{DD}$ = 2.3V[5] | $I_{OH}$ = 9mA | — | — | 0.6 | |

**NOTES:**
1. $V_{IL}$ and $V_{IH}$ must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS table for the appropriate $V_{DD}$ range. $T_A$ = -40°C to +85°C.
2. Demonstrates operation for nominal $V_{DD}$ = 1.2V.
3. Demonstrates operation for nominal $V_{DD}$ = 1.5V.
4. Demonstrates operation for nominal $V_{DD}$ = 1.8V.
5. Demonstrates operation for nominal $V_{DD}$ = 2.5V.

## OPERATING CHARACTERISTICS, $T_A$ = 25°C

| Symbol | Parameter | Test Conditions | $V_{DD}$ = 0.8V | $V_{DD}$ = 1.2V | $V_{DD}$ = 1.5V | $V_{DD}$ = 1.8V | $V_{DD}$ = 2.5V | Unit |
|---|---|---|---|---|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance Outputs Enabled | $C_L$ = 0pF f = 10MHz | 24 | 24 | 25 | 26 | 30 | pF |
| $C_{PD}$ | Power Dissipation Capacitance Outputs Disabled | | 2 | 2 | 2 | 3 | 4 | pF |

## SWITCHING CHARACTERISTICS[1]

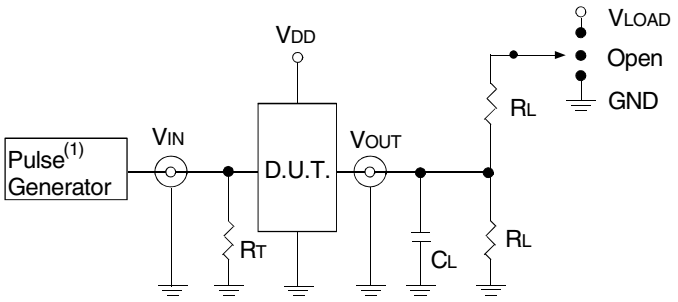
| | | $V_{DD}$ = 0.8V | $V_{DD}$ = 1.2V±0.1V | | $V_{DD}$ = 1.5V±0.1V | | $V_{DD}$ = 1.8V±0.15V | | | $V_{DD}$ = 2.5V±0.2V | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Typ. | Min. | Max. | Min. | Max. | Min. | Typ. | Max. | Min. | Max. | Unit |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay xAx to x$\overline{Y}$x | 5.9 | 0.9 | 2.6 | 0.7 | 1.8 | 0.6 | 1.4 | 2 | 0.4 | 1.6 | ns |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time x$\overline{OE}$ to x$\overline{Y}$x | 7.9 | 1.2 | 3.8 | 0.8 | 2.5 | 0.7 | 1.5 | 2.5 | 0.7 | 2 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time x$\overline{OE}$ to x$\overline{Y}$x | 9.3 | 2.1 | 6 | 1.5 | 4.8 | 1.8 | 2.7 | 4.5 | 0.6 | 2.3 | ns |

**NOTE:**
1. See TEST CIRCUITS AND WAVEFORMS. $T_A$ = -40°C to +85°C.

# TEST CIRCUITS AND WAVEFORMS

## TEST CONDITIONS(1)

| Symbol | VDD = 0.8V | VDD = 1.2V±0.1V | VDD = 1.5V±0.1V | VDD = 1.8V±0.15V | VDD = 2.5V±0.2V | Unit |
|---|---|---|---|---|---|---|
| VLOAD | 2xVDD | 2xVDD | 2xVDD | 2xVDD | 2xVDD | V |
| VT | VDD/2 | VDD/2 | VDD/2 | VDD/2 | VDD/2 | V |
| VLZ | 100 | 100 | 100 | 150 | 150 | mV |
| VHZ | 100 | 100 | 100 | 150 | 150 | mV |
| RL | 2 | 2 | 2 | 1 | 0.5 | KΩ |
| CL | 15 | 15 | 15 | 30 | 30 | pF |



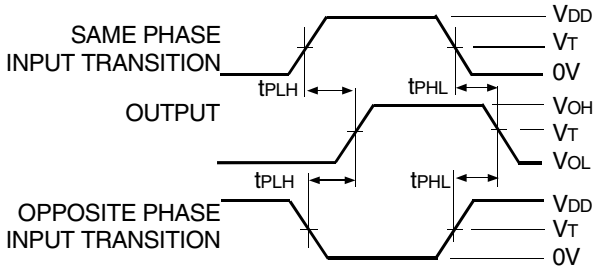

***Test Circuits for All Outputs***

**DEFINITIONS:**
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

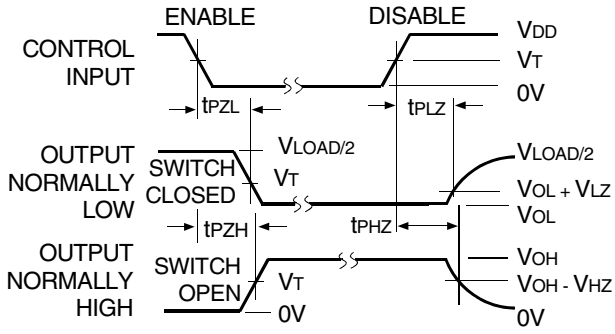
**NOTE:**
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; Slew Rate ≥ 1V/ns.

## SWITCH POSITION

| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | VLOAD |
| Disable High<br>Enable High | GND |
| All Other Tests | Open |



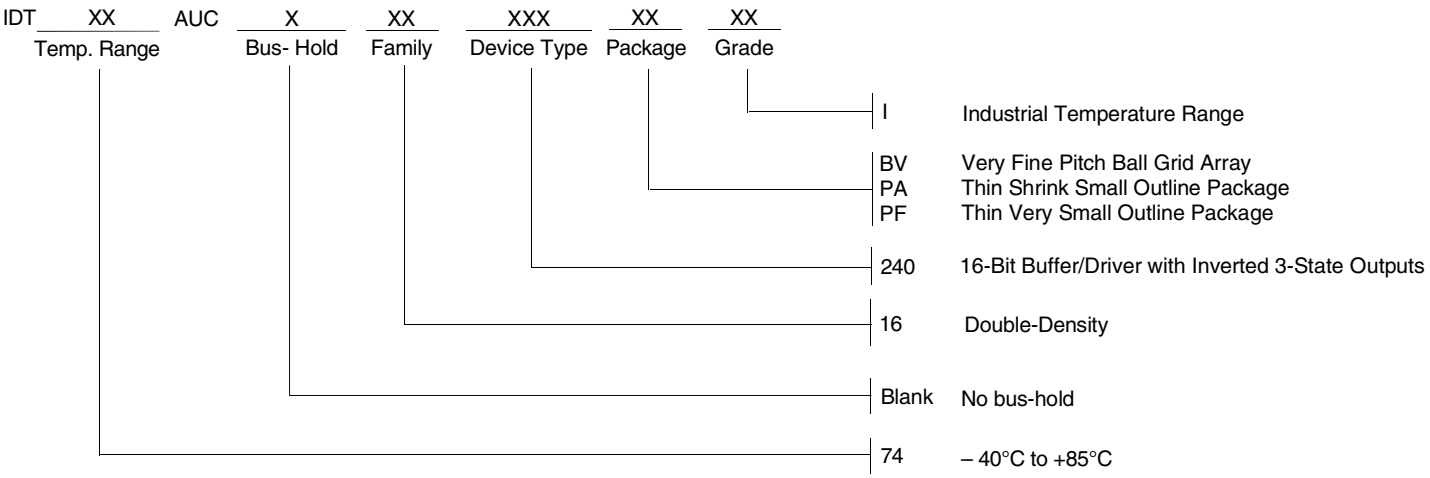

***Propagation Delay***




**NOTE:**
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

***Enable and Disable Times***

## ORDERING INFORMATION




*CORPORATE HEADQUARTERS*
6024 Silver Creek Valley Road
San Jose, CA 95138

*for SALES:*
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

*for Tech Support:*
logichelp@idt.com