- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- ***DOC*™ (Dynamic Output Control) Circuit Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation**
- **Dynamic Drive Capability Is Equivalent to Standard Outputs With $I_{OH}$ and $I_{OL}$ of ±24 mA at 2.5-V $V_{CC}$**
- **Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications**
- **$I_{off}$ Feature Supports Partial Power-Down Mode Operation**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) and Thin Very Small-Outline (DGV) Packages**

## description

A Dynamic Output Control (DOC) circuit is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical $V_{OL}$ vs $I_{OL}$ and $V_{OH}$ vs $I_{OH}$ curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

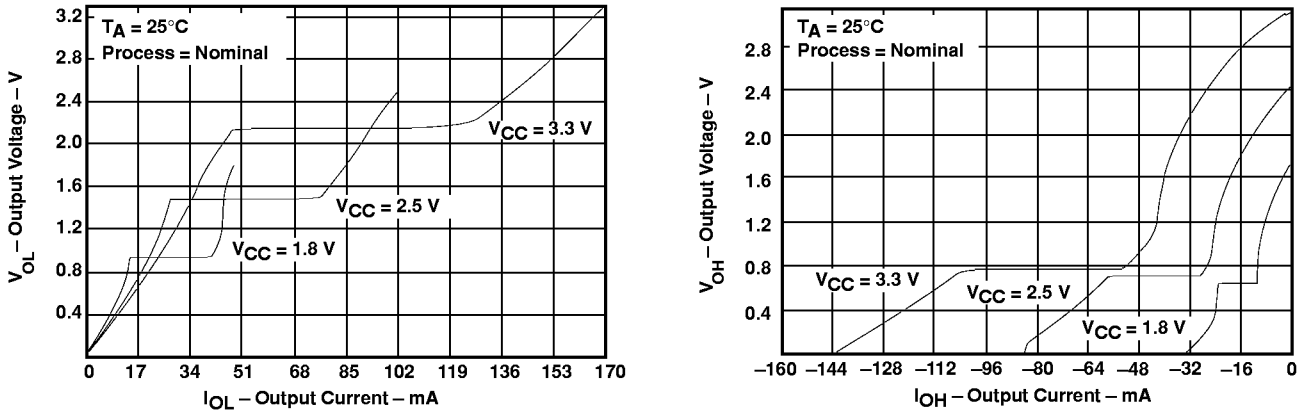



**Figure 1. Output Voltage vs Output Current**

This 16-bit universal bus driver is operational at 1.2-V to 3.6-V $V_{CC}$, but designed specifically for 1.65-V to 3.6-V $V_{CC}$ operation.

Data flow from A to Y is controlled by the output-enable ($\overline{OE}$) input. The device operates in the transparent mode when the latch-enable ($\overline{LE}$) input is low. When $\overline{LE}$ is high, the A data is latched if the clock (CLK) input is held at a high or low logic level. If $\overline{LE}$ is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

PRODUCT PREVIEW

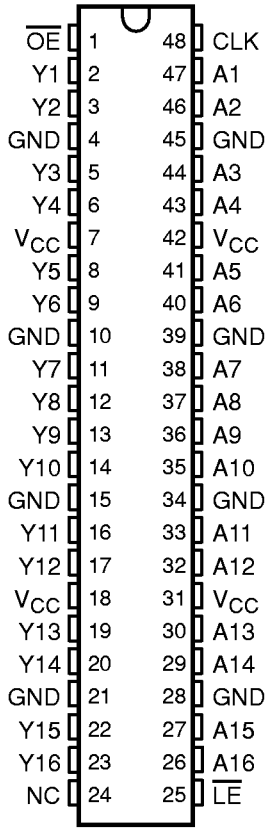
## description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74AVCH16334 is characterized for operation from –40°C to 85°C.

## terminal assignments

**DGG OR DGV PACKAGE**
**(TOP VIEW)**



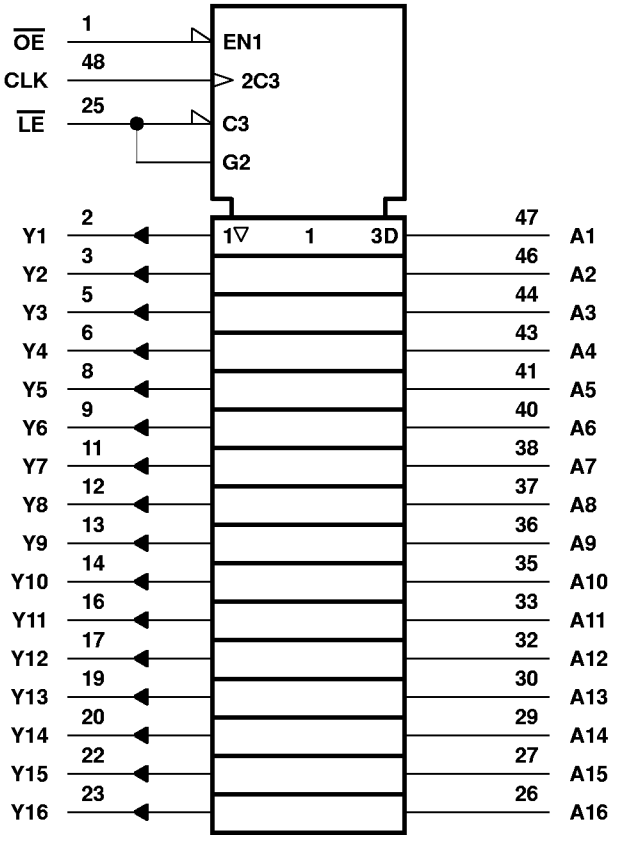

NC – No internal connection

**FUNCTION TABLE**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{OE}$ | $\overline{LE}$ | CLK | A | Y |
| H | X | X | X | Z |
| L | L | X | L | L |
| L | L | X | H | H |
| L | H | ↑ | L | L |
| L | H | ↑ | H | H |
| L | H | L or H | X | $Y_0$† |

† Output level before the indicated steady-state input conditions were established

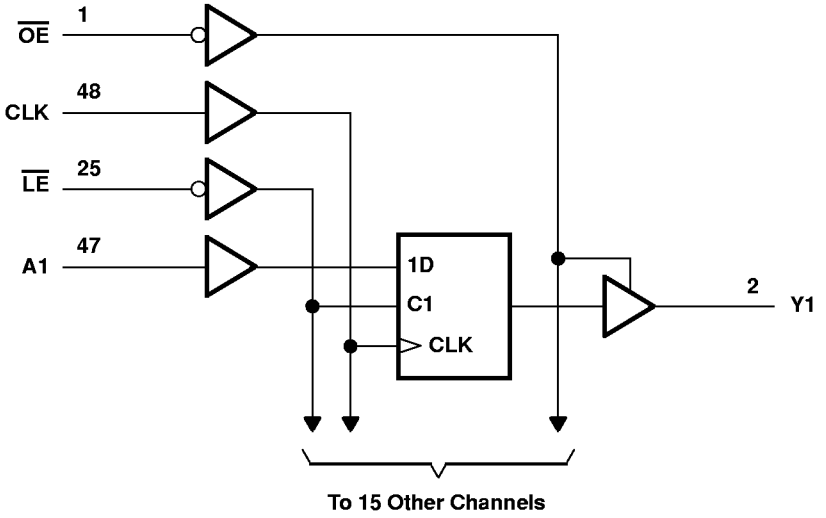
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . –50 mA
Continuous output current, $I_O$ . . . . . ±50 mA
Continuous current through each $V_{CC}$ or GND . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package . . . . . 89°C/W
DGV package . . . . . 93°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
3. The package thermal impedance is calculated in accordance with JESD 51.

PRODUCT PREVIEW

## recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Operating | 1.65 | 3.6 | V |
| | | Data retention only | 1.2 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.2 V | $V_{CC}$ | | V |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 0.65 × $V_{CC}$ | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.2 V | | GND | V |
| | | $V_{CC}$ = 1.65 V to 1.95 V | | 0.35 × $V_{CC}$ | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | 0.8 | |
| $V_I$ | Input voltage | | 0 | 3.6 | V |
| $V_O$ | Output voltage | Active state | 0 | $V_{CC}$ | V |
| | | 3-state | 0 | 3.6 | V |
| $I_{OHS}$ | Static high-level output current† | $V_{CC}$ = 1.65 V to 1.95 V | | –4 | mA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | –8 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | –12 | |
| $I_{OLS}$ | Static low-level output current† | $V_{CC}$ = 1.65 V to 1.95 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 8 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | 12 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 1.65 V to 3.6 V | | 5 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

† Dynamic drive capability is equivalent to standard outputs with $I_{OH}$ and $I_{OL}$ of ±24 mA at 2.5-V $V_{CC}$. See Figure 1 for $V_{OL}$ vs $I_{OL}$ and $V_{OH}$ vs $I_{OH}$ characteristics. Refer to the TI application reports, ***AVC Logic Family Technology and Applications***, literature number **SCEA006**, and ***Dynamic Output Control (DOC™) Circuitry Technology and Applications***, literature number **SCEA009**.

NOTE 4: All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OHS}$ = –100 μA | | 1.65 V to 3.6 V | $V_{CC}$–0.2 | | | V |
| | | $I_{OHS}$ = –4 mA, | $V_{IH}$ = 1.07 V | 1.65 V | 1.2 | | | |
| | | $I_{OHS}$ = –8 mA, | $V_{IH}$ = 1.7 V | 2.3 V | 1.75 | | | |
| | | $I_{OHS}$ = –12 mA, | $V_{IH}$ = 2 V | 3 V | 2.3 | | | |
| $V_{OL}$ | | $I_{OLS}$ = 100 μA | | 1.65 V to 3.6 V | | | 0.2 | V |
| | | $I_{OLS}$ = 4 mA, | $V_{IL}$ = 0.57 V | 1.65 V | | | 0.45 | |
| | | $I_{OLS}$ = 8 mA, | $V_{IL}$ = 0.7 V | 2.3 V | | | 0.55 | |
| | | $I_{OLS}$ = 12 mA, | $V_{IL}$ = 0.8 V | 3 V | | | 0.7 | |
| $I_I$ | Control inputs | $V_I = V_{CC}$ or GND | | 3.6 V | | | ±2.5 | μA |
| $I_{BHL}$‡ | | $V_I$ = 0.57 V | | 1.65 V | 25 | | | μA |
| | | $V_I$ = 0.7 V | | 2.3 V | 45 | | | |
| | | $V_I$ = 0.8 V | | 3 V | 75 | | | |
| $I_{BHH}$§ | | $V_I$ = 1.07 V | | 1.65 V | –25 | | | μA |
| | | $V_I$ = 1.7 V | | 2.3 V | –45 | | | |
| | | $V_I$ = 2 V | | 3 V | –75 | | | |
| $I_{BHLO}$¶ | | $V_I$ = 0 to $V_{CC}$ | | 1.95 V | 200 | | | μA |
| | | | | 2.7 V | 300 | | | |
| | | | | 3.6 V | 500 | | | |
| $I_{BHHO}$# | | $V_I$ = 0 to $V_{CC}$ | | 1.95 V | –200 | | | μA |
| | | | | 2.7 V | –300 | | | |
| | | | | 3.6 V | –500 | | | |
| $I_{off}$ | | $V_I$ = 0 or 3.6 V | | 0 | | | ±10 | μA |
| $I_{OZ}$ | | $V_O = V_{CC}$ or GND | | 3.6 V | | | ±10 | μA |
| $I_{CC}$ | | $V_I = V_{CC}$ or GND, | $I_O$ = 0 | 3.6 V | | | 40 | μA |
| $C_i$ | Control inputs | $V_I = V_{CC}$ or GND | | 2.5 V | | | | pF |
| | | | | 3.3 V | | | | |
| | Data inputs | | | 2.5 V | | | | |
| | | | | 3.3 V | | | | |
| $C_o$ | Outputs | $V_O = V_{CC}$ or GND | | 2.5 V | | | | pF |
| | | | | 3.3 V | | | | |

† Typical values are measured at $T_A$ = 25°C.
‡ The bus-hold circuit can sink at least the minimum low sustaining current at $V_{IL}$ max. $I_{BHL}$ should be measured after lowering $V_{IN}$ to GND and then raising it to $V_{IL}$ max.
§ The bus-hold circuit can source at least the minimum high sustaining current at $V_{IH}$ min. $I_{BHH}$ should be measured after raising $V_{IN}$ to $V_{CC}$ and then lowering it to $V_{IH}$ min.
¶ An external driver must source at least $I_{BHLO}$ to switch this node from low to high.
# An external driver must sink at least $I_{BHHO}$ to switch this node from high to low.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 6)**

| | | | | $V_{CC}$ = 1.2 V | | $V_{CC}$ = 1.5 V ± 0.1 V | | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | | | | | | | | | | | | MHz |
| $t_w$ | Pulse duration | $\overline{LE}$ low | | | | | | | | | | | | ns |
| | | CLK high or low | | | | | | | | | | | | |
| $t_{su}$ | Setup time | Data before CLK↑ | | | | | | | | | | | | ns |
| | | Data before $\overline{LE}$↑ | CLK high | | | | | | | | | | | |
| | | | CLK low | | | | | | | | | | | |
| $t_h$ | Hold time | Data after CLK↑ | | | | | | | | | | | | ns |
| | | Data after $\overline{LE}$↑ | CLK high or low | | | | | | | | | | | |

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 6)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.2 V | | $V_{CC}$ = 1.5 V ± 0.1 V | | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | | | | | | | | | | | MHz |
| $t_{pd}$ | A | Y | | | | | | | | | | | ns |
| | $\overline{LE}$ | | | | | | | | | | | | |
| | CLK | | | | | | | | | | | | |
| $t_{en}$ | $\overline{OE}$ | Y | | | | | | | | | | | ns |
| $t_{dis}$ | $\overline{OE}$ | Y | | | | | | | | | | | ns |

**switching characteristics from 0°C to 85°C, $C_L$ = 0 pF†**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 3.3 V ± 0.15 V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $t_{pd}$ | A | Y | | | ns |
| | CLK | | | | |

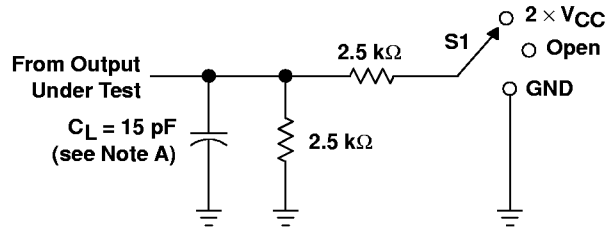
† Texas Instruments SPICE simulation data

**operating characteristics, $T_A$ = 25°C**

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | $C_L$ = 0, f = 10 MHz | | | | pF |
| | | Outputs disabled | | | | | |

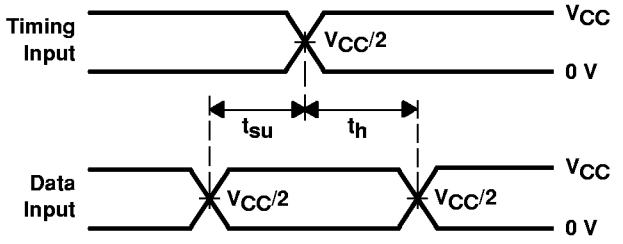
PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 1.2 V

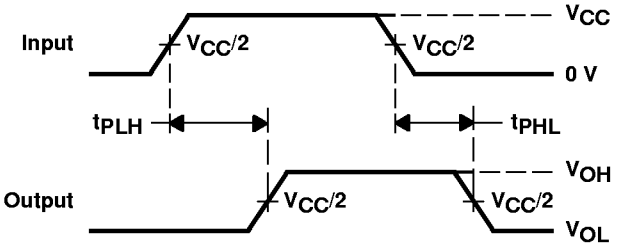



| TEST | S1 |
|---|---|
| $t_{pd}$<br>$t_{PLZ}/t_{PZL}$<br>$t_{PHZ}/t_{PZH}$ | Open<br>2 × $V_{CC}$<br>GND |

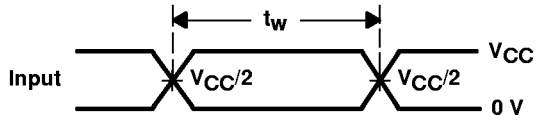
LOAD CIRCUIT



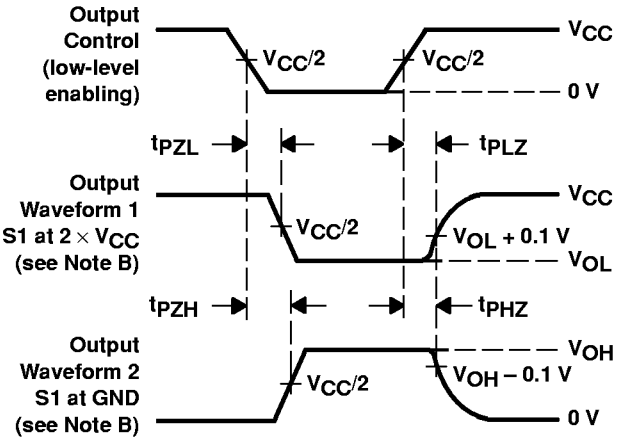

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION

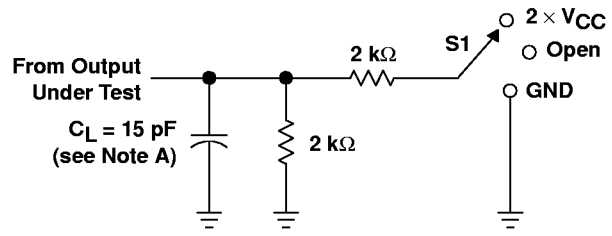



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

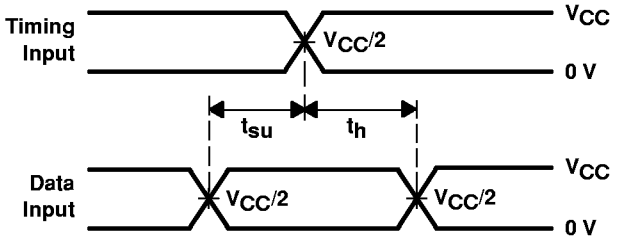
**Figure 2. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 1.5 V ± 0.1 V

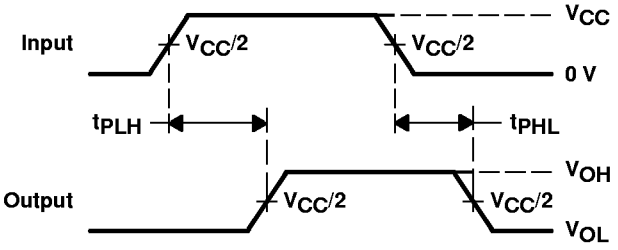



LOAD CIRCUIT

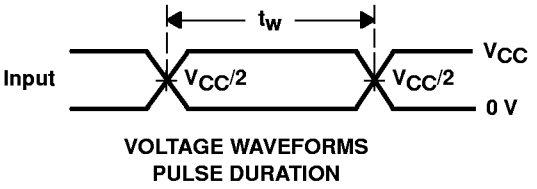
| TEST | S1 |
|---|---|
| $t_{pd}$<br>$t_{PLZ}/t_{PZL}$<br>$t_{PHZ}/t_{PZH}$ | Open<br>2 × $V_{CC}$<br>GND |



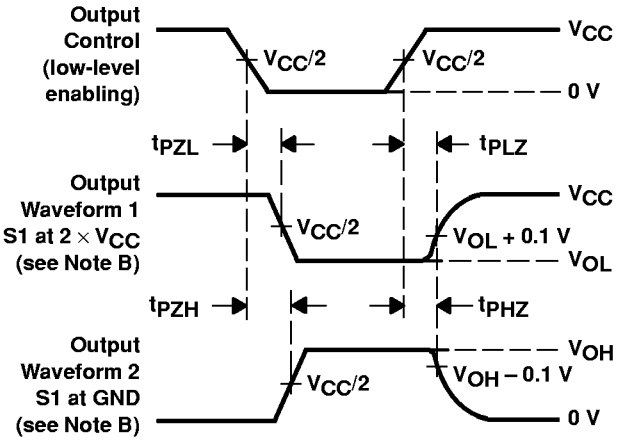

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION



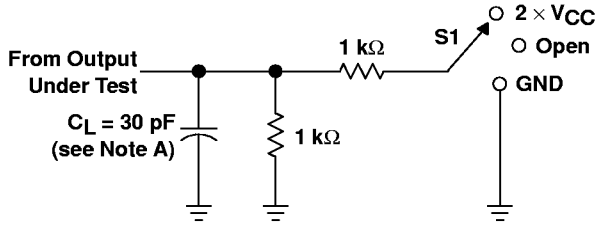

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 3. Load Circuit and Voltage Waveforms**

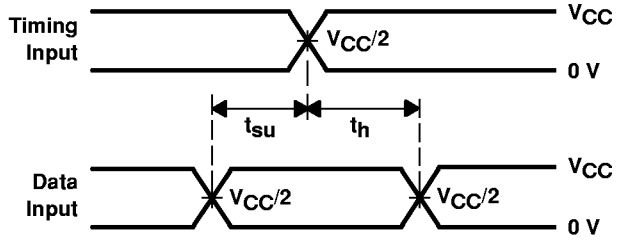
PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 1.8 V ± 0.15 V

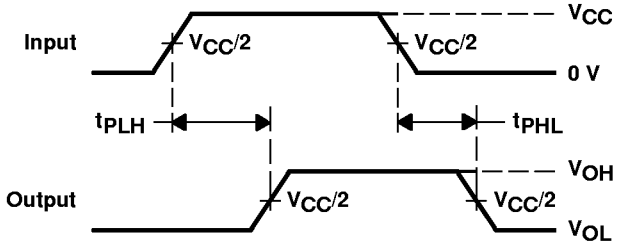



| TEST | S1 |
|---|---|
| $t_{pd}$<br>$t_{PLZ}/t_{PZL}$<br>$t_{PHZ}/t_{PZH}$ | Open<br>2 × $V_{CC}$<br>GND |

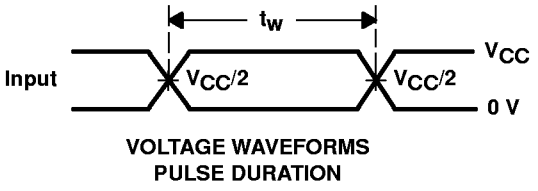
LOAD CIRCUIT



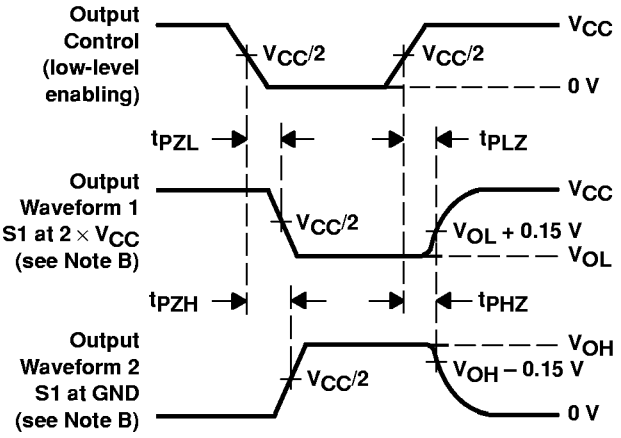

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION

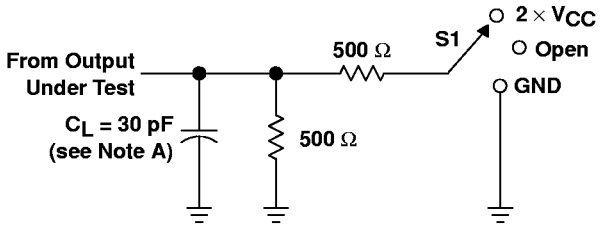



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

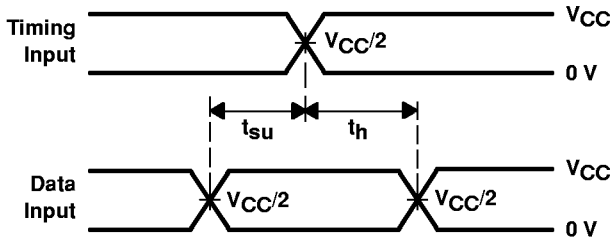
**Figure 4. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.5 V ± 0.2 V

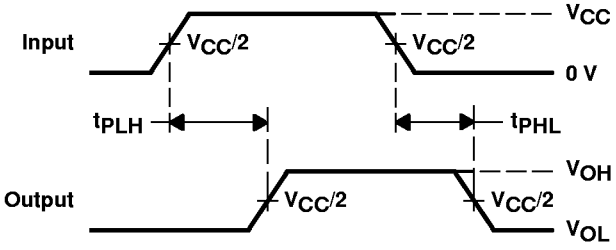



LOAD CIRCUIT

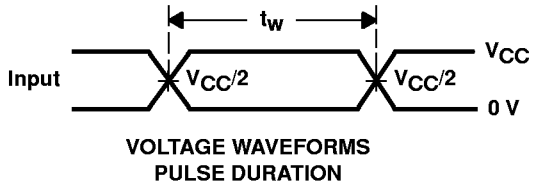
| TEST | S1 |
|---|---|
| $t_{pd}$<br>$t_{PLZ}/t_{PZL}$<br>$t_{PHZ}/t_{PZH}$ | Open<br>2 × $V_{CC}$<br>GND |



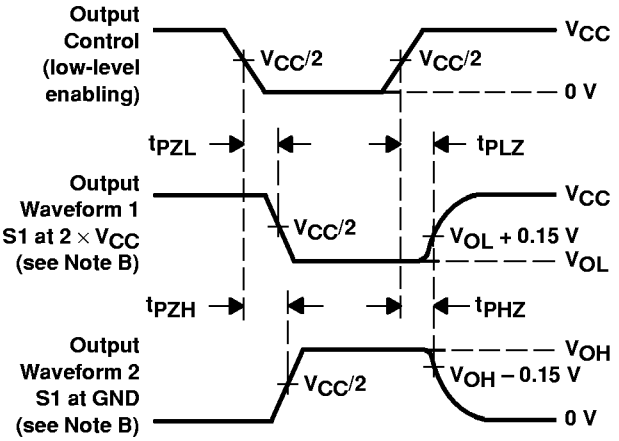

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION



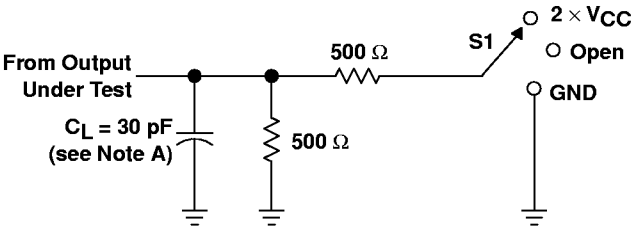

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 5. Load Circuit and Voltage Waveforms**

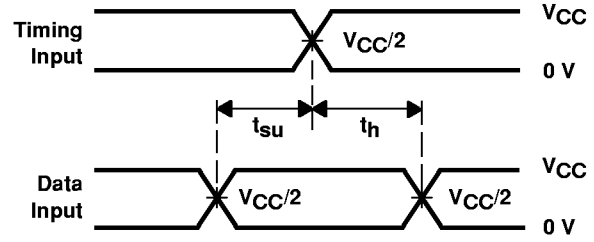
PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 3.3 V ± 0.3 V

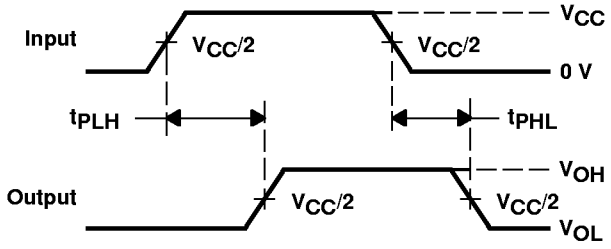



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

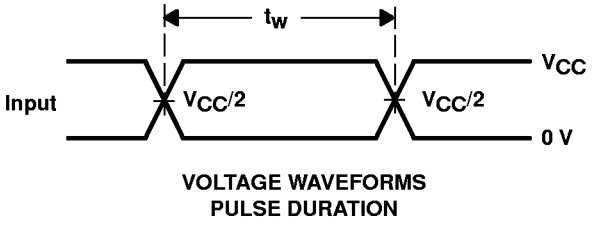
LOAD CIRCUIT



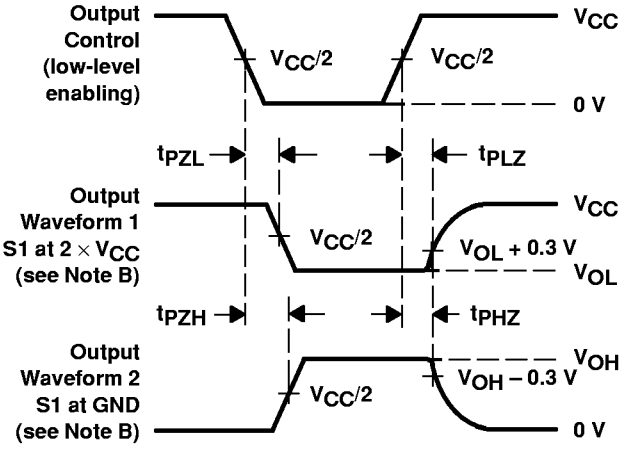

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 6. Load Circuit and Voltage Waveforms**

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