

TC74HC377AP, TC74HC377AF, TC74HC377AFW**OCTAL D - TYPE FLIP - FLOP**

The TC74HC377A is a high speed CMOS OCTAL D - TYPE FLIP - FLOP fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This 8-bit D - type flip - flop is controlled by a clock input (CK) and an output enable input (\bar{G}).

The signal level applied to the D inputs are transferred to Q outputs during the positive going transition of CK.

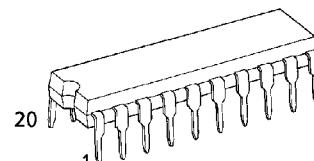
When the \bar{G} is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

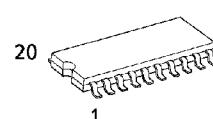
FEATURES :

- High Speed..... $f_{MAX} = 73\text{MHz}(\text{typ.})$
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..... $|I_{OH}| = I_{OL} = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays..... $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range..... V_{CC} (opr.) = $2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS377

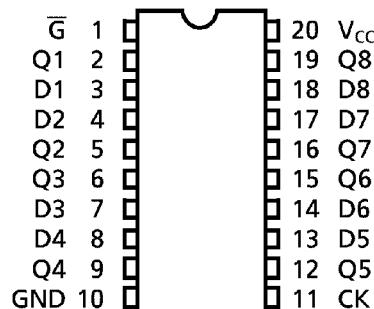
(Note) The JEDEC SOP (FW) is not available in Japan.



P (DIP20-P-300-2.54A)
Weight : 1.30g (Typ.)



F (SOP20-P-300-1.27) FW (SOL20-P-300-1.27)
Weight : 0.22g (Typ.) Weight : 0.46g (Typ.)

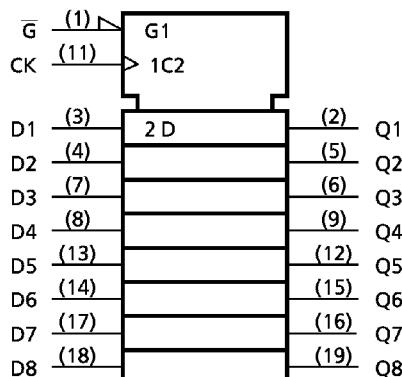
PIN ASSIGNMENT

(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUTS
\bar{G}	CK	D	Q
H	X	X	NO CHANGE
L	—	L	L
L	—	H	H
X	—	X	NO CHANGE

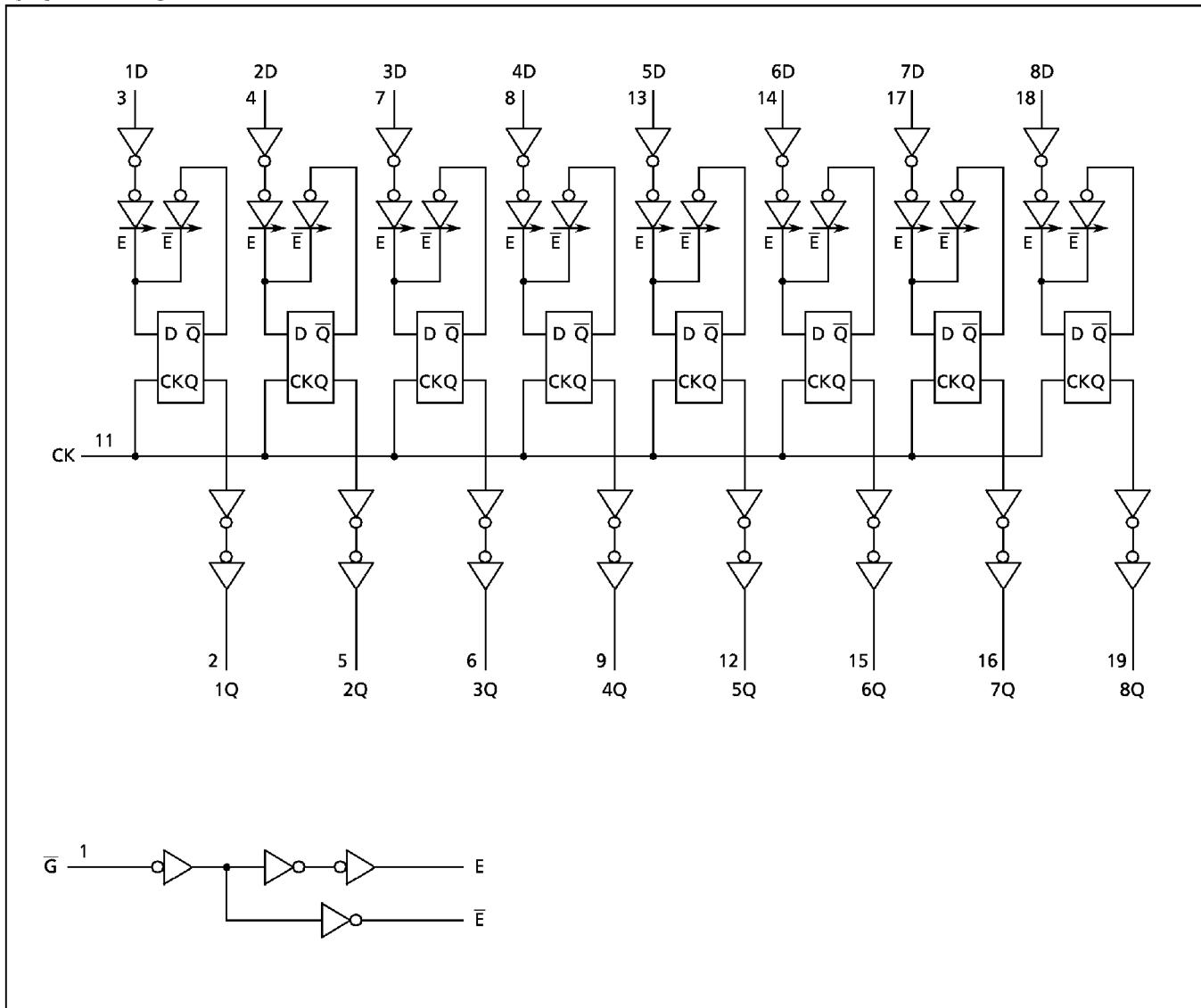
X : Don't Care

IEC LOGIC SYMBOL

961001EBA2

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SYSTEM DIAGRAM



961001EBA2'

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7	V
DC Input Voltage	V_{IN}	-0.5~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	-0.5~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} / Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{STG}	-65~150	°C

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	t_r, t_f	0~ 1000 ($V_{CC} = 2.0\text{V}$) 0~ 500 ($V_{CC} = 4.5\text{V}$) 0~ 400 ($V_{CC} = 6.0\text{V}$)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0	1.50	—	—	1.50	—	V
			4.5	3.15	—	—	3.15	—	
			6.0	4.20	—	—	4.20	—	
Low - Level Input Voltage	V_{IL}		2.0	—	—	0.50	—	0.50	V
			4.5	—	—	1.35	—	1.35	
			6.0	—	—	1.80	—	1.80	
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0	—	1.9	V
			$I_{OH} = -20\mu\text{A}$	4.5	4.4	4.5	—	4.4	
			$I_{OH} = -20\mu\text{A}$	6.0	5.9	6.0	—	5.9	
			$I_{OH} = -4\text{ mA}$ $I_{OH} = -5.2\text{ mA}$	4.5	4.18	4.31	—	4.13	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IL}$	$I_{OL} = 20\mu\text{A}$	6.0	5.68	5.80	—	5.63	V
			$I_{OL} = 20\mu\text{A}$	2.0	—	0.0	0.1	—	
			$I_{OL} = 20\mu\text{A}$	4.5	—	0.0	0.1	—	
			$I_{OL} = 20\mu\text{A}$	6.0	—	0.0	0.1	—	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0	—	—	± 0.1	—	± 1.0	μA
			6.0	—	—	4.0	—	40.0	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	6.0	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}(\text{V})$	Ta = 25°C		Ta = -40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time (D-CK)	t_s		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time (G-CK)	t_s		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Hold Time	t_h		2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Clock Frequency	f		2.0	—	7	6	MHz
			4.5	—	36	29	
			6.0	—	42	34	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, Ta = 25°C, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	4	8	ns
			—	14	24	
Propagation Delay Time (CK-Q)	t_{pLH} t_{pHL}		—	—	—	MHz
			38	73	—	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}(\text{V})$	Ta = 25°C			Ta = -40~85°C	UNIT
				MIN.	TYP.	MAX.	MIN.	
Output Transition Time	t_{TLH} t_{THL}		2.0	—	30	75	—	95
			4.5	—	8	15	—	19
			6.0	—	7	13	—	16
Propagation Delay Time (CK-Q)	t_{pLH} t_{pHL}		2.0	—	57	140	—	175
			4.5	—	17	28	—	35
			6.0	—	13	24	—	30
Maximum Clock Frequency	f_{MAX}		2.0	7	18	—	6	—
			4.5	36	59	—	29	—
			6.0	42	77	—	34	—
Input Capacitance	C_{IN}		—	5	10	—	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$		—	32	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

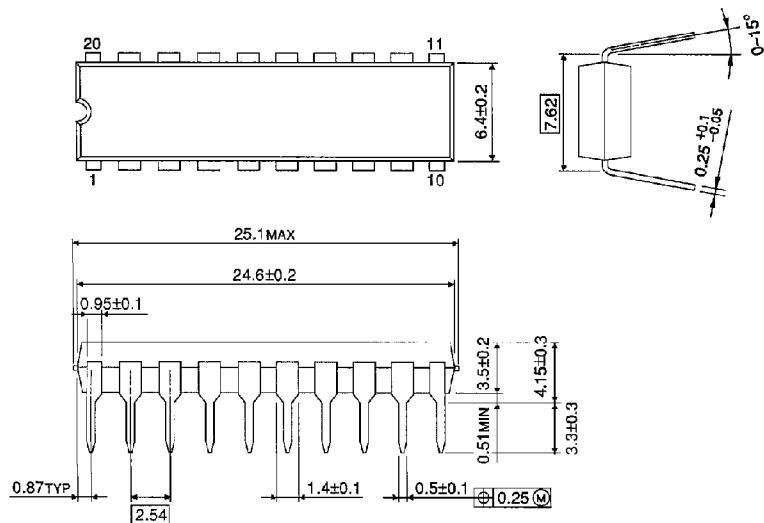
$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per Flip Flop)}$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation :

$$C_{PD}(\text{total}) = 22 + 10 \cdot n$$

DIP 20PIN OUTLINE DRAWING (DIP20-P-300-2.54A)

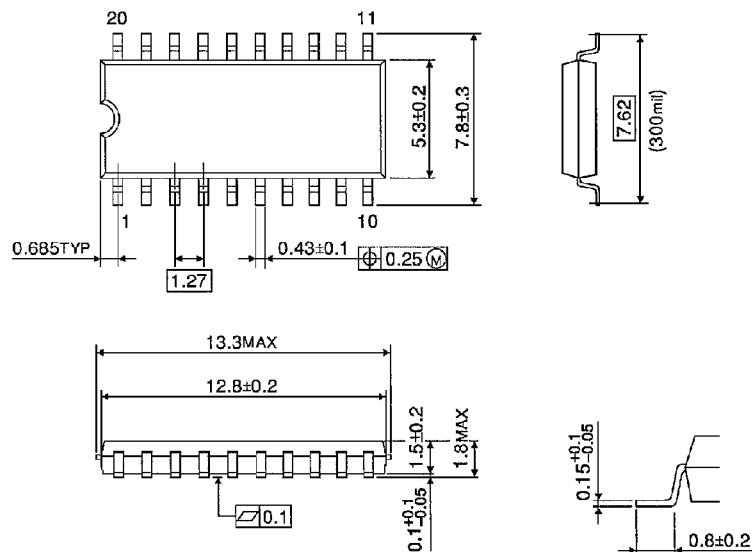
Unit in mm



Weight : 1.30g (Typ.)

SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300-1.27)

Unit in mm

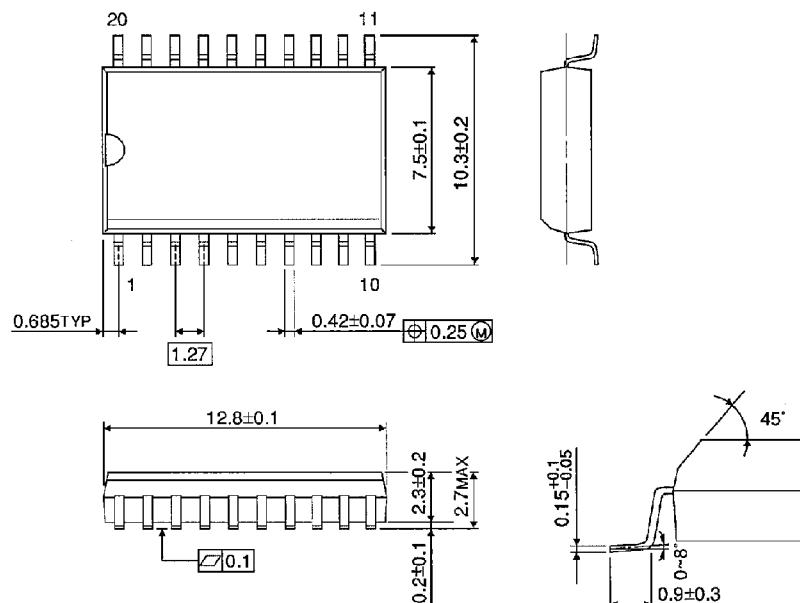


Weight : 0.22g (Typ.)

SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20-P-300-1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)