Octal transceiver with direction pin; 3-state; inverting

74HL33640

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **Inverting 3-state outputs**
- **Direct interface with TTL levels**

DESCRIPTION

The 74HL33640 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74HL33640 is an octal transceiver featuring inverting 3-state bus compatible outputs in both send and receive directions. The "640" features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.
The "640" is identical to the "245" but has inverting outputs.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = $\overline{B}$	inputs
L	H	inputs	B = $\overline{A}$
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 50 pF V_{CC} = 3.3 V	2.2	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HL33640D	24	SO	plastic	SOT137-1
74HL33640DB	24	SSOP	plastic	SOT340-1
74HL33640PW	24	TSSOP	plastic	SOT355-1

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	A_0 to A_7	data inputs/outputs
5, 6, 7, 8	GND	ground (0 V)
13	$\overline{OE}$	output enable input (active LOW)
14, 15, 16, 17, 20, 21, 22, 23	B_7 to B_0	data inputs/outputs
18, 19	V_{CC}	positive supply voltage
24	DIR	direction control

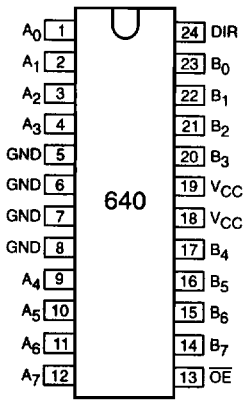

Fig.1 Pin configuration.

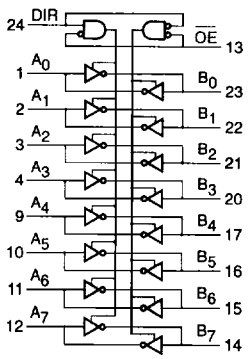

Fig.2 Logic symbol.

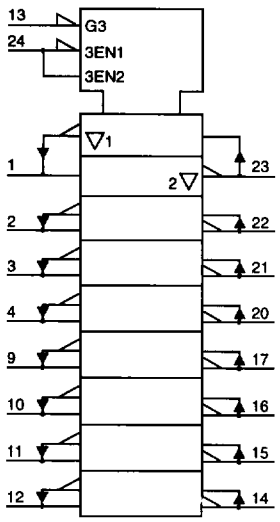

Fig.3 IEC logic symbol.

DC CHARACTERISTICS FOR 74HL33640

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HL33640

GND = 0 V; $t_r = t_f$ = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		−40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay	–	14.0	–	16.0	ns	1.2	Fig. 4
	A_n to B_n;	–	5.3	–	6.0		2.0	
	B_n to A_n	–	3.5	–	4.0		3.0	
t_{PZH}/t_{PZL}	3-state output enable time	–	17.8	–	20.7	ns	1.2	Fig. 5, 6
	$\overline{OE}$ to A_n;	–	7.5	–	8.5		2.0	
	$\overline{OE}$ to B_n	–	5.4	–	6.1		3.0	
t_{PHZ}/t_{PLZ}	3-state output disable time	–	15.0	–	16.7	ns	1.2	Fig. 5, 6
	$\overline{OE}$ to A_n;	–	6.4	–	7.0		2.0	
	$\overline{OE}$ to B_n	–	4.7	–	5.1		3.0	
t_{PZH}/t_{PZL}	3-state output enable time	–	21.4	–	23.5	ns	1.2	Fig. 5, 6
	DIR to A_n;	–	8.8	–	9.6		2.0	
	DIR to B_n	–	6.3	–	6.8		3.0	
t_{PHZ}/t_{PLZ}	3-state output disable time	–	17.4	–	19.0	ns	1.2	Fig. 5, 6
	DIR to A_n;	–	7.3	–	7.9		2.0	
	DIR to B_n	–	5.3	–	5.7		3.0	

AC WAVEFORMS

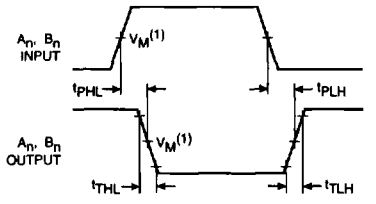

Fig. 4 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

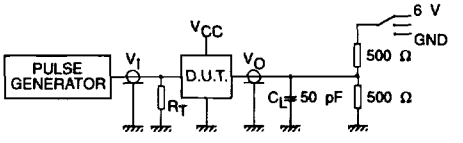

Fig. 6 Test conditions: Load circuitry for enable / disable times; switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

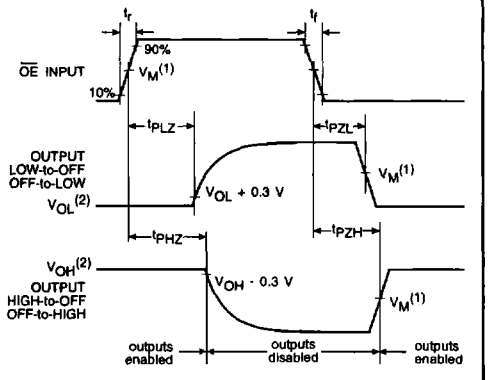

Fig.5 Waveforms showing the 3-state enable and disable times.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.