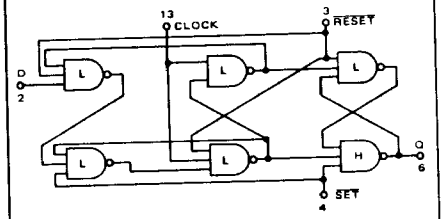
QUAD TYPE D FLIP-FLOP

MC4015L,P*

ADVANCE INFORMATION / NEW PRODUCT

1/4 OF DEVICE SHOWN
(CLOCK AND $\overline{\text{RESET}}$ COMMON TO ALL FOUR FLIP-FLOPS)

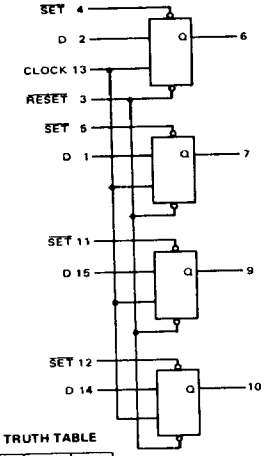


Input Loading Factor:
D = 1 CLOCK = 8
SET = 2 RESET = 8
Output Loading Factor = 11
Total Power Dissipation = 190 mW typ/pkg
Propagation Delay Time = 16 ns typ
Setup Time = 15 ns max
Hold Time = 5.0 ns max
Operating Frequency = 30 MHz typ

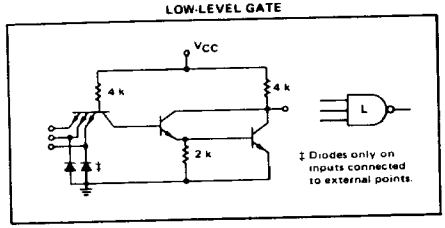
V_{CC} = PIN 16
GND = PIN 8

This quad type D flip-flop triggers on the positive edge of the clock input. During the clock transition the state of the D input is transferred to the Q output. The device is useful in shift registers and simple counters.

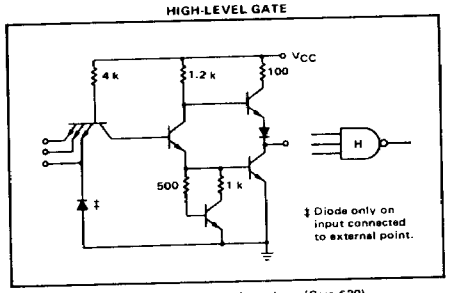
Power dissipation is minimized and output drive capability is maximized by connecting low and high-level gates as shown by the logic diagram to form each of the four flip-flops.



LOW-LEVEL GATE



HIGH-LEVEL GATE



TRUTH TABLE

D	Q_{n-1}	Q_n
0	0	0
0	1	0
1	0	1
1	1	1

Q_{n-1} = time period prior to clock pulse
Q_n = time period following clock pulse

OPERATING CHARACTERISTICS

Data must be present at the D input 15 ns prior to the rise of the clock, and remain 5.0 ns after the clock signal rises. Data may be changed any time during the clock cycle except the interval between the setup time (15 ns) and the hold time (5.0 ns) without affecting the operation of the flip-flop. The data input is inhibited when the clock is high. When the clock is in the low state, the input steering section continually reflects the state of the D input. Information present at the D input during the time interval between the setup and hold times is transferred to the bistable section on the positive edge of the clock, and outputs Q and $\overline{Q}$ respond accordingly.

The flip-flops can be set or reset directly at any time, regardless of the state of the clock, by applying a low state to the direct $\overline{\text{Set}}$ or $\overline{\text{Reset}}$ inputs.

* L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4000 INPUT LOADING FACTOR	MC4000 OUTPUT LOADING FACTOR
MC4000	1.0	11
MC400	1.0	10
MC2000	0.67	6
MC3000	0.7	8
MC7400	1.0	10
MC830	1.15**	12

Note: Differences in MC4000 series loading factors result from differences in specifications for each family.

**Applies only when input is being driven by MDTL gate with 2.0 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6.0 k ohm pullup resistors reduce drive capability to fan-out of 3.

DC ELECTRICAL CHARACTERISTICS

(T_A = 0 to 75°C)

Characteristic	Symbol	Value	Conditions
Input			
Forward Current — D	I_{F1}	-1.6 mAdc max	V_{in} = 0.4 Vdc, V_{CC} = 5.25 Vdc
$\overline{SET}$		-3.2 mAdc max	
$\overline{RESET}$, CLOCK		-12.8 mAdc max	
D	I_{F2}	-1.4 mAdc max	V_{in} = 0.4 Vdc, V_{CC} = 4.75 Vdc
$\overline{SET}$		-2.8 mAdc max	
$\overline{RESET}$, CLOCK		-11.2 mAdc max	
Leakage Current — D	I_R	40 μAdc max	V_{in} = 2.5 Vdc, V_{CC} = 5.25 Vdc
$\overline{SET}$		80 μAdc max	
$\overline{RESET}$, CLOCK		320 μAdc max	
Breakdown Voltage	BV_{in}	5.5 Vdc max	I_{in} = 1.0 mAdc, V_{CC} = 5.25 Vdc, T_A = 25°C
Clamp Voltage	V_D	-1.5 Vdc max	I_D = -10 mAdc, V_{CC} = 4.75 Vdc, T_A = 25°C
Threshold Voltage	V_{th} "1"	2.0 Vdc	T_A = 0°C
		1.8 Vdc	T_A = +25°C, or T_A = +75°C
	V_{th} "0"	1.1 Vdc	T_A = 0°C, or T_A = +25°C
		0.9 Vdc	T_A = +75°C
Output			
Output Voltage	V_{OL}	0.4 Vdc max	$\overline{RESET}$ = 0, I_{OL} = 16 mAdc, V_{CC} = 4.75 Vdc
		0.4 Vdc max	$\overline{RESET}$ = 0, I_{OL} = 17.6 mAdc, V_{CC} = 5.25 Vdc
	V_{OH}	2.5 Vdc min	$\overline{SET}$ = 0, I_{OH} = -1.6 mAdc, V_{CC} = 4.75 Vdc
Short-Circuit Current	I_{SC}	-20 to -65 mAdc	V_{CC} = 5.0 Vdc, output grounded

The DSP56008 signals that may be programmed as General Purpose I/O are listed with their primary function in **Table 3-9**.

Table 3-9 DSP56002 General Purpose I/O Pin Identification in PGA Package

Pin Number	Primary Function	Port	GPIO ID
E11	H0	B	PB0
D11	H1		PB1
C11	H2		PB2
E10	H3		PB3
D10	H4		PB4
B12	H5		PB5
A11	H6		PB6
B11	H7		PB7
C9	HA0		PB8
B9	HA1		PB9
A9	HA2		PB10
D9	$\overline{\text{HR/W}}$		PB11
B10	$\overline{\text{HEN}}$		PB12
C10	$\overline{\text{HREQ}}$		PB13
A10	$\overline{\text{HACK}}$		PB14
C12	RXD	C	PC0
D12	TXD		PC1
E12	SCLK		PC2
F11	SC0		PC3
G12	SC1		PC4
F13	SC2		PC5
F12	SCK		PC6
G13	SRD		PC7
G11	STD		PC8
H11	TIO	No port assigned	