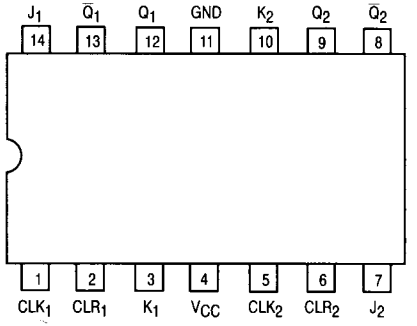
MOTOROLA

Dual J-K Flip-Flop With Clear

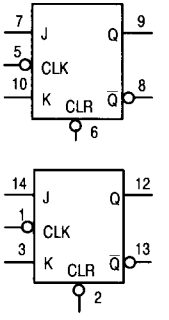
ELECTRICALLY TESTED PER:
MIL-M-38510/30101

The 54LS73A offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

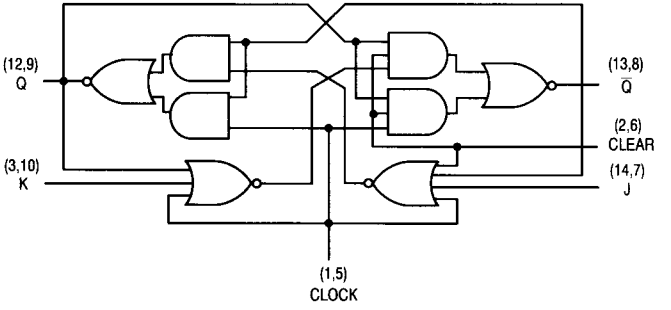
CONNECTION DIAGRAM



LOGIC SYMBOL



LOGIC DIAGRAM
(one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Military 54LS73A

AVAILABLE AS:

1) JAN: JM38510/30101BXA
2) SMD: N/A
3) 883: 54LS73A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: SEE 54LS113A

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	BURN-IN (COND. A)
CLK_1	1	1	V_{CC}
CLR_1	2	2	GND
K_1	3	3	V_{CC}
V_{CC}	4	4	V_{CC}
CLK_2	5	5	V_{CC}
CLR_2	6	6	GND
J_2	7	7	V_{CC}
$\bar{Q}_2$	8	8	V_{CC}
Q_2	9	9	OPEN
K_2	10	10	V_{CC}
GND	11	11	GND
Q_1	12	12	OPEN
$\bar{Q}_1$	13	13	V_{CC}
J_1	14	14	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

MODE SELECT — TRUTH TABLE

Operating Mode	Inputs			Outputs	
	$\bar{C}_D$	J	K	Q	$\bar{Q}$
Reset (Clear)	L	X	X	L	H
Toggle	H	h	h	$\bar{q}$	q
Load "0" (Reset)	H	l	h	L	H
Load "1" (Set)	H	h	l	H	L
Hold	H	l	l	q	$\bar{q}$

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Don't Care
l, h, (q) = Lower case letters indicate the state of referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

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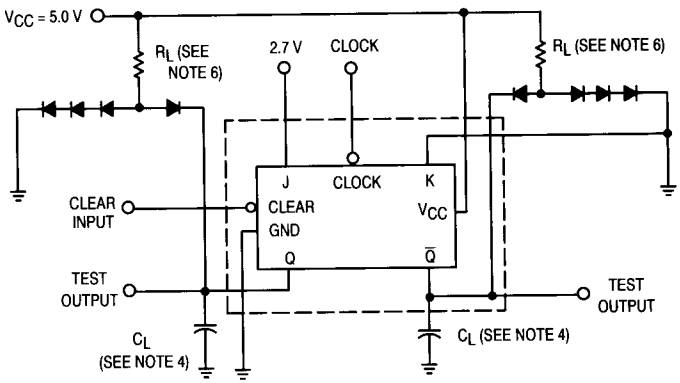
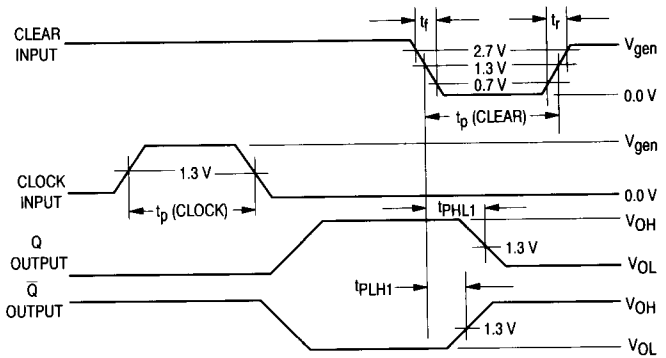
CLEAR SWITCHING TEST CIRCUIT



WAVEFORMS



NOTES:

1. Clear inputs dominate regardless of the state of the clock or J-K inputs.
2. Clear input pulse characteristics: V_{gen} = 3.0 V, $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, t_p (clear) = 30 ns, PRR ≤ 1.0 MHz.
3. All diodes are 1N3064, or equivalent.
4. C_L = 50 pF ± 10% (including jig and probe capacitance).
5. Voltage measurements are to be made with respect to network ground terminal.
6. R_L = 2.0 kΩ ± 5.0%.
7. Clock input pulse characteristics: V_{gen} = 3.0 V, t_p (clock) = 25 ns, PRR ≤ 1.0 MHz.

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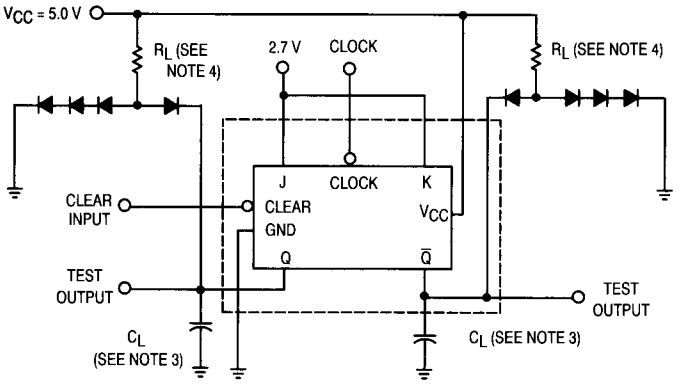
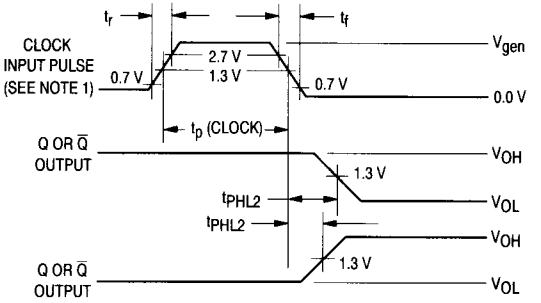
SYNCHRONOUS SWITCHING TEST CIRCUIT



WAVEFORMS



NOTES:

1. Clock input characteristics for t_{PLH}, t_{PHL} (clock to output): V_{gen} = 3.0 V, $t_r \leq 15$ ns, t_f = 6.0 ns, t_p (clock) = 25 ns and PRR ≤ 1.0 MHz. When testing f_{MAX} the clock input characteristics are: V_{gen} = 3.0 V, $t_r = t_f \leq 6.0$ ns, t_p (clock) ≤ 20 ns and PRR = see table.
2. All diodes are 1N3064, or equivalent.
3. C_L = 50 pF ± 10% (including jig and probe capacitance).
4. R_L = 2.0 kΩ ± 5.0%.

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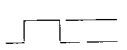
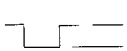
Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = − 0.4 mA, V_{IN} = 2.0 V, V_{IL} = 0.7 V.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IH} = 2.0 V, V_{IL} = 0.7 V.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = − 18 mA, other inputs are open.
I_{IH1}	Logical "1" Input Current (J & K inputs)		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other input = 4.5 V, CLK & CLR = GND.
I_{IHH1}	Logical "1" Input Current (J & K inputs)		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other input = 4.5 V, CLK & CLR = GND.
I_{IH2}	Logical "1" Input Current (CLR inputs)		60		60		60	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other input = 4.5 V, CLK & J = GND.
I_{IHH2}	Logical "1" Input Current (CLR inputs)		300		300		300	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other input = 4.5 V, CLK & J = GND.
I_{IH3}	Logical "1" Input Current (CLK inputs)		80		80		80	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, CLR − K & J = GND.
I_{IHH3}	Logical "1" Input Current (CLK inputs)		400		400		400	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, CLR − K & J = GND.
I_{IL1}	Logical "0" Input Current (J & K inputs)	− 0.12	− 0.36	− 0.12	− 0.36	− 0.12	− 0.36	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, CLR & K = 4.5 V, CLK = (See Note 2).
I_{IL2}	Logical "0" Input Current (CLK inputs)	− 0.24	− 0.72	− 0.24	− 0.72	− 0.24	− 0.72	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, J & K = 4.5 V, CLR = (See Note 2).
I_{IL3}	Logical "0" Input Current (CLR inputs)	− 0.12	− 0.72	− 0.12	− 0.72	− 0.12	− 0.72	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, CLK − J & K = 4.5 V.
I_{OS}	Output Short Circuit Current	−15	−100	−15	−100	−15	−100	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, CLK − CLR & J = GND, V_{OUT} = 2.25 V.
I_{CC}	Power Supply Current		8.0		8.0		8.0	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs), or V_{IN} = 5.5 V (all inputs).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

NOTES:

1. 

2. 

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output CLR to Q_n	5.0 —	28 20	5.0 —	40 35	5.0 —	40 35	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output CLR to Q_n	5.0 —	21 20	5.0 —	32 27	5.0 —	32 27	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PHL2} t_{PHL2}	Propagation Delay /Data-Output CLK to Q_n or $\overline{Q}n$	5.0 —	30 20	5.0 —	42 37	5.0 —	42 37	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PLH2} t_{PLH2}	Propagation Delay /Data-Output CLK to Q_n or $\overline{Q}n$	5.0 —	22 20	5.0 —	32 27	5.0 —	32 27	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
f_{MAX}	Maximum Clock Frequency	25		25		25		MHz	V_{CC} = 5.0 V, V_{IN} = 2.7 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%.
f_{MAX}	Maximum Clock Frequency	30						MHz	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.

NOTES:

1. f_{MAX}, min. limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
2. Tests shall be performed in sequence, attributes data only.
3. The limits specified for C_L = 15 pF are guaranteed but not tested.

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