BiCMOS CURRENT MODE PWM CONTROLLER

FEATURES

- Low Power BiCMOS Design
- Tough CMOS™ Construction
- Low Supply Current .....1.0 mA Typ @ 100 kHz
- Wide Supply Voltage Operation .....8V to 18V
- Latch-Up Immunity.....500 mA on Outputs
- Input Will Withstand Negative Inputs to –5 Volts
- High Output Drive .....0.7A Peak (1.2A on 14 and 16-Pin Versions)
- 2 kV ESD Protection
- Current Mode Control
- Fast Rise/Fall Time (Max) .....60 ns @ 1000 pf
- High Frequency Operation.....300 kHz
- Clock Ramp Reset Current .....2.5 mA ±10%
- Low Propagation Delay Current Amp to Output .....140 ns Typ
- Pin Compatible with UC3842/3843/3844/3845

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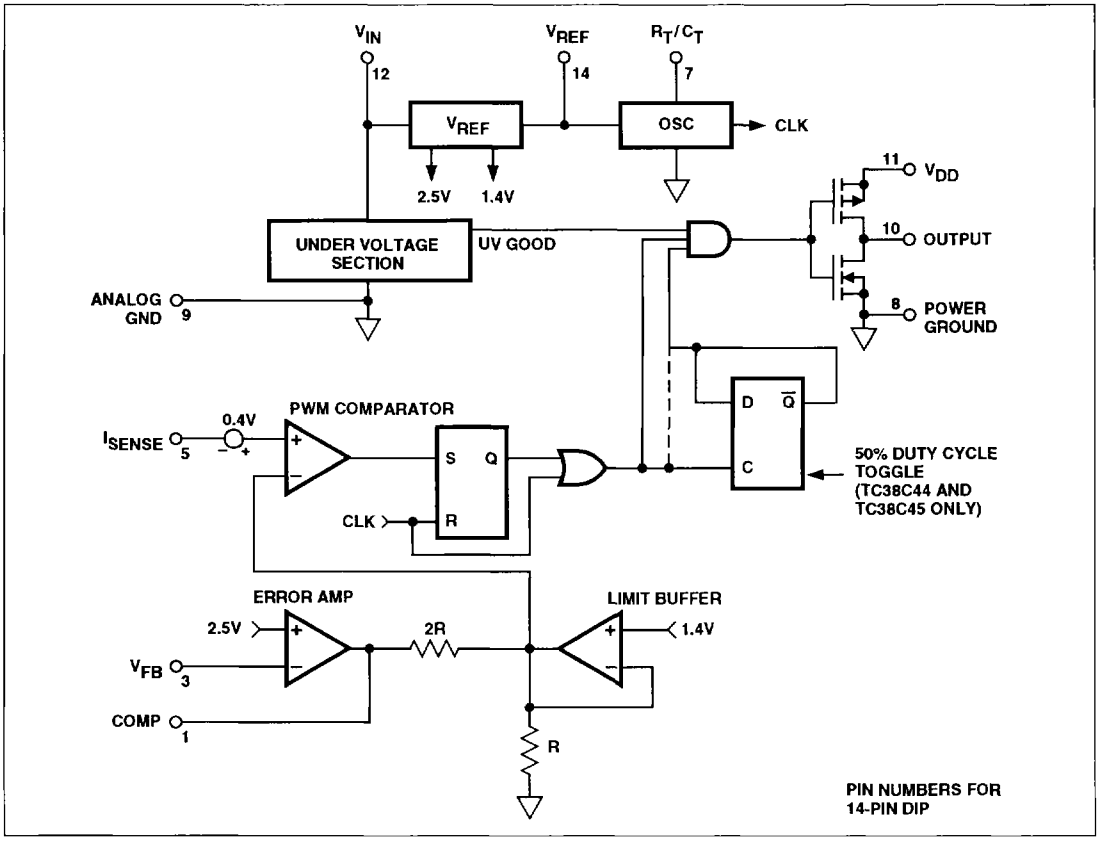
BLOCK DIAGRAM



TC18C42/3/4/5
TC28C42/3/4/5
TC38C42/3/4/5

GENERAL DESCRIPTION

The TC38C42/3/4/5 are current mode BiCMOS PWM control ICs. With a low 1.0 mA supply current along with the high drive currents (0.7A peak) they provide a low cost solution for a PWM that operates to 300 kHz and directly drives MOSFETs up to HEX 3 size.

Performance of the oscillator and current sense amplifier have been greatly improved over previous bipolar versions. Voltage and temperature stability have been improved by a factor of 3. Noise immunity (PSRR) has also been improved. These improvements make for a more reliable power system.

Tough CMOS™ design and construction provide input and output latch protection, outstanding ESD tolerance, and high reliability manufacturing techniques and materials. Tough CMOS™ means high reliability.

The TC38C42/3/4/5 are pin compatible with earlier bipolar versions so that designers can easily update older designs. Improvements have been added though. For example, clock ramp reset current is specified at 2.5 mA (±10%) for accurate deadtime control. A few component values must be changed (R_T & C_T) to use TC38C42 family in existing bipolar designs.

The 14-pin DIP and 16-pin SO versions have separate and internally isolated grounds, and are rated for higher output current (1.2A). These separate grounds allow for 'bootstrap' operation of the PWM to further improve efficiency.

REFERENCE SECTION

The reference is a zener based design with a buffer amplifier to drive the output. It is unstable with capacitances between 0.01 µF and 3.3 µF. In a normal application a 4.7 µF is used. In some lower noise layouts the capacitor can be eliminated entirely.

The reference is active as soon as the 38C4X has power supplied. This is different than its bipolar counterparts, in that the bipolar reference comes on only after the IC has come out of its under voltage mode. Thus, on the 38C4X, the reference pin can not be used as a reset function such as on a soft start circuit.

OSCILLATOR SECTION

The oscillator frequency is set by the combination of a resistor from the reference to the R_T/C_T pin and by a capacitor from this pin to ground. The oscillator is designed to have ramp amplitude from 0.15 to 2.5 volts. This is approximate, as over shoot on the oscillator comparator causes the ramp amplitude to increase with frequency due to comparator delay. Minimum values for C_T and R_T are 33 pF and 1 kΩ respectively. Maximum values are dependent on leakage currents in the capacitor, not on the input currents to the R_T/C_T pin.

Frequency of Operation

The frequency of oscillation for the TC38C4X family is controlled by a resistor to V_{REF} (R_T) and a capacitor to ground (C_T). V_{REF} supplies current through the resistor and charges the capacitor until its voltage reaches the threshold of the upper comparator (≈2.5V). A 2.5 mA current is then applied to the capacitor to discharge it to near ground (≈0.15V). The discharge current is then shut off and the cycle repeats. An approximate equation for the frequency of operation is:

$$f_O \approx \frac{1}{R_T C_T} \quad (R_T \text{ in Ohms and } C_T \text{ in Farads})$$

The value of R_T affects the discharge current and the upper and lower comparators each have delay. As R_T gets smaller and as the frequency of operation gets higher, the above equation falls apart. Figure 5 illustrates this effect.

Dead Time

The value of R_T has a effect on the discharge rate but the primary consideration is the value of C_T. The time required to discharge the capacitor is approximately 1000 C_T.

ORDERING INFORMATION

Part No.	Package	Temperature
TC18C**MJA	8-pin CerDIP	–55°C to +125°C
TC18C**MJD	14-pin CerDIP	–55°C to +125°C
TC28C**EJA	8-pin CerDIP	–40°C to +85°C
TC28C**EJD	14-pin CerDIP	–40°C to +85°C
TC28C**EOE	16-pin SOIC Wide	–40°C to +85°C
TC28C**EPA	8-pin Plastic DIP	–40°C to +85°C
TC28C**EPD	14-pin Plastic	–40°C to +85°C
TC38C**COE	16-pin SOIC Wide	0°C to +70°C
TC38C**CPA	8-pin Plastic DIP	0°C to +70°C
TC38C**CPD	14-pinPlastic	0°C to +70°C

	Duty Cycle Limitation	
Start-up Voltage	99%	49%
14.5 V	X8C42	X8C44
8.4 V	X8C43	X8C45

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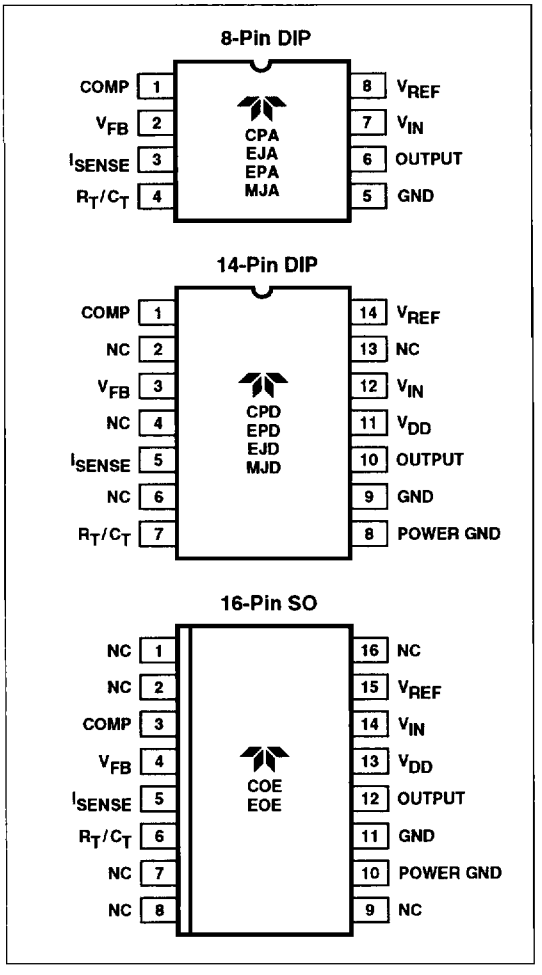
PIN CONFIGURATIONS



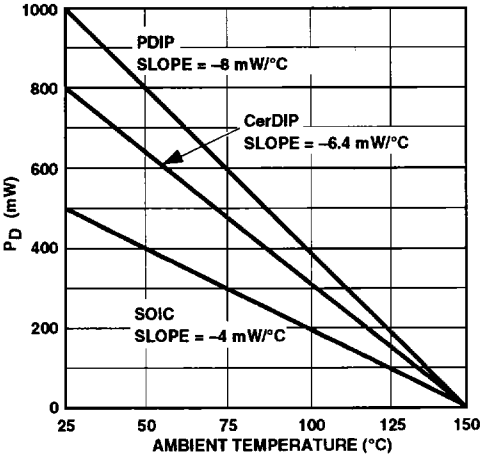
ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Maximum Chip Temperature ..... 150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (10 sec) ..... +300°C
Package Thermal Resistance
- CerDip $R_{\theta J\text{-}A}$ ..... 150°C/W
- CerDip $R_{\theta J\text{-}C}$ ..... 55°C/W
- PDIP $R_{\theta J\text{-}A}$ ..... 125°C/W
- PDIP $R_{\theta J\text{-}C}$ ..... 45°C/W
- SOIC $R_{\theta J\text{-}A}$ ..... 250°C/W
- SOIC $R_{\theta J\text{-}C}$ ..... 75°C/W

Operating Temperature
- 18C4X ..... $-55C° \leq T_A \leq +125°C$
- 28C4X ..... $-40C° \leq T_A \leq +85°C$
- 38C4X ..... $0C° \leq T_A \leq +70°C$

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

Package Power Dissipation



TC18C42/3/4/5
TC28C42/3/4/5
TC38C42/3/4/5

ELECTRICAL CHARACTERISTICS: unless otherwise stated, these specifications apply over specified temperature range. $V_{IN} = V_{DD} = 15V$; $R_T = 71\ k\Omega$; $C_T = 150\ pF$

		TC18C4X TC28C4X			TC38C4X			
Parameter	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Reference Section								
Output Voltage	$T_A = 25°C$, $I_O = 1\ mA$	4.95	5	5.05	4.90	5	5.10	V
Line Regulation	$9.5V \le V_{IN} \le 15V$, $I_O = 1\ mA$	—	±3	±10	—	±3	±10	mV
Load Regulation	$1mA \le I_O \le 11\ mA$	—	±5	±15	—	±3	±10	mV
Temp Stability	(note 1)	—	±0.25	±0.5	—	±0.25	±0.5	mV/°C
Output Noise Voltage	$10\ Hz \le f \le 10\ kHz$, $T_A = 25°C$ (note 1)	—	100	—	—	100	—	µV(rms)
Long Term Stability	$T_A = 125°C$, 1000 Hrs. (note 1)	—	±0.5	—	—	±0.5	—	%
Output Short Circuit		-20	-50	-100	-30	-50	-100	mA
Oscillator Section								
Initial Accuracy	$T_A = 25°C$ (note 4)	95	100	105	95	100	105	kHz
Voltage Stability	$9.5V \le V_{IN} \le 15V$	—	±0.2	±0.3	—	±0.2	±0.3	%
Temp Stability	$T_{MIN} \le T_A \le T_{MAX}$ (note 1); Figure 2	—	±0.01	±0.05	—	±0.01	±0.03	%/°C
Clock Ramp Reset	R_T/C_T pin at 4V	2.25	2.5	2.75	2.25	2.5	2.75	mA
Amplitude	R_T/C_T pin peak to peak	2.45	2.65	2.85	2.45	2.65	2.85	V
Maximum Freq	(note 1)	300	—	—	300	—	—	kHz
Error Amp Section								
Input Offset Voltage	$V_{(COMP)} = 2.5V$	—	±15	±50	—	±15	±50	mV
Input Bias Current	(note 1)	—	±0.3	±2	—	±0.3	±2	nA
A_{VOL}	$2V \le V_O \le 4V$	70	90	—	70	90	—	dB
Gain Bandwidth Product	(note 1)	650	750	—	650	750	—	kHz
PSRR	$9.5V \le V_{IN} \le 15V$	80	100	—	80	100	—	dB
Output Sink Current	$V_{FB} = 2.7V$, $V_{(COMP)} = 1.1V$ (note 1)	1.2	1.5	—	1.5	1.7	—	mA
Output Source Current	$V_{FB} = 2.3V$, $V_{(COMP)} = 5V$ (note 1)	3	3.4	—	3.9	4.2	—	mA
V_{OUT} High	$V_{FB} = 2.3V$, $R_L = 10k$ to ground	5.8	6	6.5	5.8	6	6.5	V
V_{OUT} Low	$V_{FB} = 2.7V$, $R_L = 10k$ to V_{REF}	0.1	0.7	1.1	0.1	0.7	1.1	V
Rise Response	(note 1)	—	5	7	—	5	7	µs
Fall Response	(note 1)	—	3	5	—	3	5	µs
Current Sense Section								
Gain Ratio	(notes 2 & 3)	2.8	2.9	3.1	2.8	2.9	3.1	V/V
Maximum Input Signal	$V_{(COMP)} = 5V$ (note 2)	0.85	0.95	1.05	0.85	0.95	1.05	V
PSRR	$9.5V \le V_{IN} \le 15V$ (notes 1, 2 & 5)	70	80	—	70	80	—	dB
Input Bias Current	(note 1)	—	±0.3	±2	—	±0.3	±2	nA
Delay to Output	V(ISENSE) = 1V (note 1); Figure 3	—	140	160	—	140	150	ns
Output Section								
$r_{DS\ (ON)}$	$I_{SINK} = 20\ mA$	—	7	15	—	7	15	Ω
$r_{DS\ (ON)}$	$I_{SOURCE} = 20\ mA$	—	11	20	—	11	15	Ω
Rise Time	$C_L = 1\ nF$ (note 1)	—	40	60	—	35	60	ns
Fall Time	$C_L = 1\ nF$ (note 1)	—	30	40	—	30	40	ns
Cross Conduction	In coulombs (note 1)	—	6.5	—	—	6.5	—	nC
V_{DD} Max	(note 1)	—	—	18	—	—	18	V

ELECTRICAL CHARACTERISTICS (Cont): unless otherwise stated, these specifications apply over specified temperature range. $V_{IN} = V_{DD} = 15V$; $R_T = 71\ k\Omega$; $C_T = 150\ pF$.

		TC18C4X TC28C4X			TC38C4X			
Parameter	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Under Voltage Lockout Section								
Start Threshold	X8C42/4	14.1	14.5	14.9	14.1	14.5	14.9	V
	X8C43/5	8	8.4	8.8	8	8.4	8.8	V
Under Voltage Threshold	X8C42/4	8.6	9	9.4	8.6	9	9.4	V
	X8C43/5	7.3	7.6	7.9	7.3	7.6	7.9	V
PWM Section								
Maximum Duty Cycle	X8C42/3 (note 1)	95	97	100	95	97	100	%
	X8C44/5 (note 1)	46	48	50	47	48	50	%
Minimum Duty Cycle				0			0	%
Supply Current								
Start Up	$T_A = 25°C$, $V_{IN} < V_{UV}$; Figure 1	50	170	300	50	170	300	µA
Operating	$V_{FB} = V(I_{SENSE}) = 0V$; Figure 4		1	2		1	1.5	mA

NOTES: 1. These parameters, although guaranteed, are not 100% tested in production.
2. Parameter measured at trip point of latch.
3. Gain ratio is defined as:

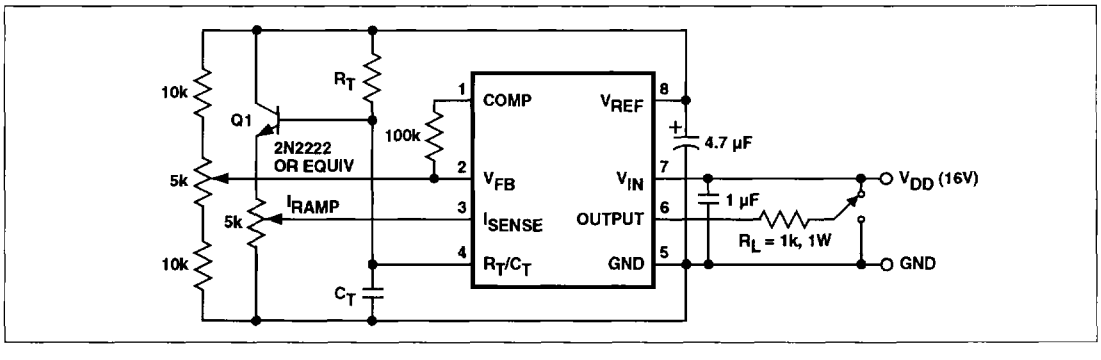
$$\frac{\Delta V_{COMP}}{\Delta V(I_{SENSE})}$$

where $0 \le V(I_{SENSE}) \le 0.8V$

4. Output frequency equals oscillator frequency for the X8C42 and X8C43. Output frequency is one half oscillator frequency for the X8C44 and X8C45.
5. PSRR of V_{REF}, Error Amp and PWM Comparator combination.

BENCH TEST OPERATIONAL SIMULATION

The timing ramp (R_T/C_T) is buffered by the emitter follower and fed back to the I_{SENSE} input. This ramp simulates the dI/dT current ramp which would flow through the primary of the transformer. The output voltage of the power supply is simulated by feeding some of the reference voltage into V_{FB}. The combination of the two input levels determines the operating characteristics of the current mode controller.



TC18C42/3/4/5
TC28C42/3/4/5
TC38C42/3/4/5

TYPICAL CHARACTERISTICS

Start Current vs. Temperature

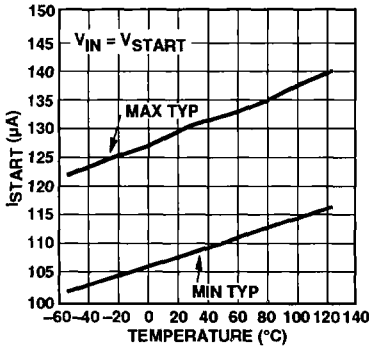


Figure 1

Oscillator Frequency Changes vs. Temperature

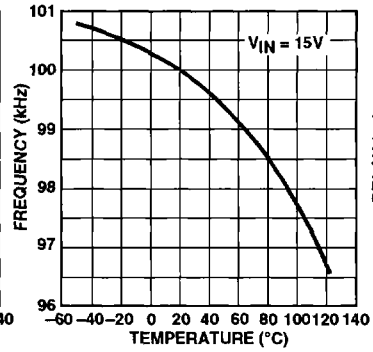


Figure 2

I_{SENSE} to Out Delay

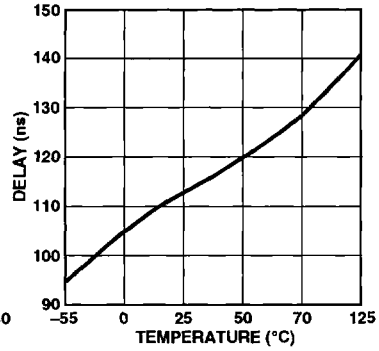


Figure 3

I_{DD} vs. Temperature

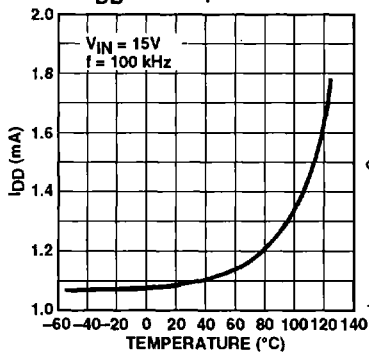


Figure 4

Frequency of Operation

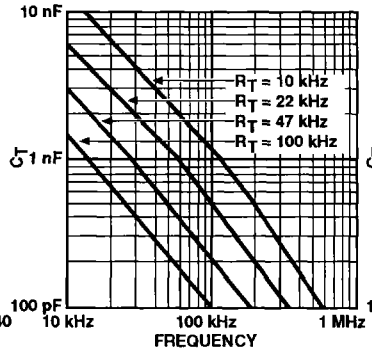


Figure 5

Dead Time vs. C_T

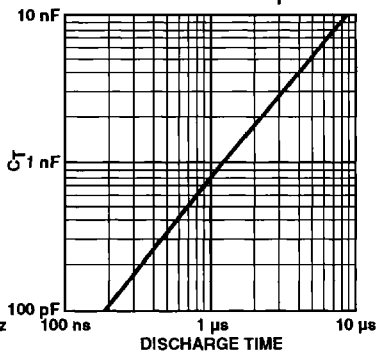


Figure 6