

TC74LVX573F/FW/FS

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

The TC74LVX573 is a high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.

Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

This device is suitable for low voltage and battery operated systems.

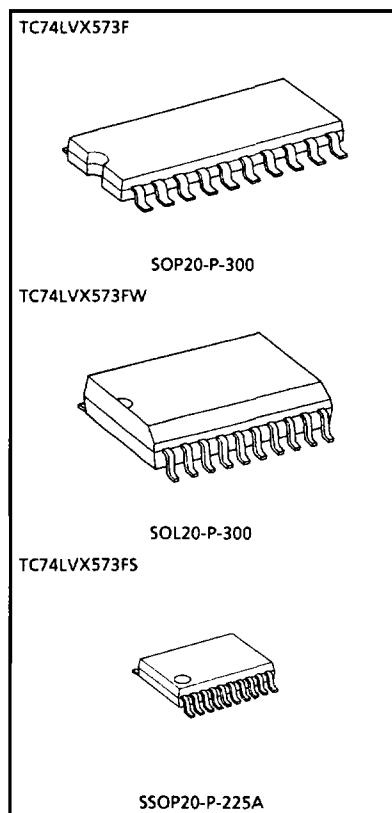
This 8bit D-type latch is controlled by a latch enable input (LE) and a output enable input (\overline{OE}).

When the \overline{OE} input is high, the eight outputs are in a high impedance state.

An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

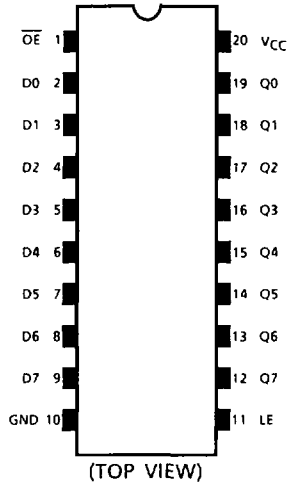
FEATURES

- High speed : $t_{pd} = 6.4ns$ (Typ.) ($V_{CC} = 3.3V$)
- Low power dissipation : $I_{CC} = 4\mu A$ (Max.) ($T_a = 25^\circ C$)
- Input voltage level : $V_{IL} = 0.8V$ (Max.) ($V_{CC} = 3V$)
 $V_{IH} = 2.0V$ (Min.) ($V_{CC} = 3V$)
- Power down protection is provided on all inputs.
- Balanced propagation delays : $t_{pLH} \approx t_{pHL}$
- Low noise : $V_{OLP} = 0.8V$ (Max.)
- Pin and function compatible with 74HC573

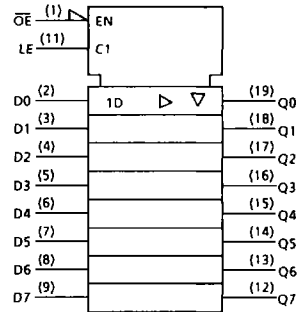


Weight SOP20-P-300 : 0.22g (Typ.)
SOL20-P-300 : 0.46g (Typ.)
SSOP20-P-225A : 0.09g (Typ.)

PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

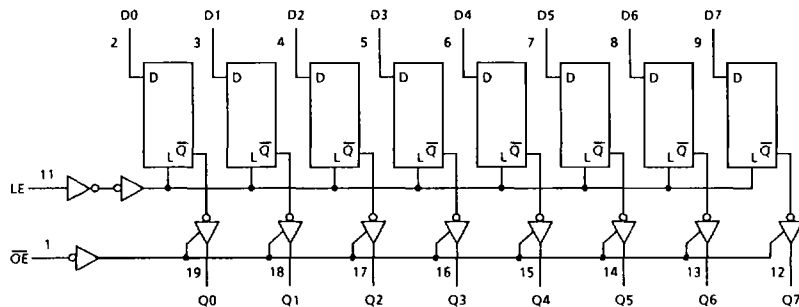
INPUTS			OUTPUTS
\overline{OE}	LE	D	
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

X : Don't Care

Z : High Impedance

Q_n : Q outputs are latched at the time when the LE input is taken to a low logic level.

SYSTEM DIAGRAM



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V _{CC}	-0.5~7.0	V
DC Input Voltage	V _{IN}	-0.5~7.0	V
DC Output Voltage	V _{OUT}	-0.5~V _{CC} +0.5	V
Input Diode Current	I _{IK}	-20	mA
Output Diode Current	I _{OK}	±20	mA
DC Output Current	I _{OUT}	±25	mA
DC V _{CC} / Ground Current	I _{CC}	±75	mA
Power Dissipation	P _D	180	mW
Storage Temperature	T _{stg}	-65~150	°C
Lead Temperature 10s	T _L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V _{CC}	2.0~3.6	V
Input Voltage	V _{IN}	0~5.5	V
Output Voltage	V _{OUT}	0~V _{CC}	V
Operating Temperature	T _{opr}	-40~85	°C
Input Rise And Fall Time	dt/dv	0~100	ns/V

ELECTRICAL CHARACTERISTICS

DC characteristics

PARAMETER	SYM-BOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
Input Voltage	"H" Level	V _{IH}	2.0	1.5	—	—	1.5	—	V	
			3.0	2.0	—	—	2.0	—		
			3.6	2.4	—	—	2.4	—		
	"L" Level	V _{IL}	2.0	—	—	0.5	—	0.5		
			3.0	—	—	0.8	—	0.8		
			3.6	—	—	0.8	—	0.8		
Output Voltage	"H" Level	V _{OH} V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	2.0	1.9	2.0	—	1.9	V	
			I _{OH} = -50μA	3.0	2.9	3.0	—	2.9		
			I _{OH} = -4mA	3.0	2.58	—	—	2.48		
	"L" Level	V _{OL} V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	2.0	—	0.0	0.1	—		0.1
			I _{OL} = 50μA	3.0	—	0.0	0.1	—		0.1
			I _{OL} = 4mA	3.0	—	—	0.36	—		0.44
3-state Output Off-state Current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	3.6	—	—	±0.25	—	±2.5	μA	
Input Leakage Current	I _{IN}	V _{IN} = 5.5V or GND	3.6	—	—	±0.1	—	±1.0	μA	
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	3.6	—	—	4.0	—	40.0	μA	

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYM-BOL	TEST CONDITION	Ta = 25°C		Ta = -40~85°C		UNIT
			VCC (V)	LIMIT	LIMIT	LIMIT	
Minimum Pulse Width (LE)	t_W (H)		2.7	6.5	7.5	ns	
			3.3 ± 0.3	5.0	5.0		
Minimum Set-up Time	t_s		2.7	5.0	5.0	ns	
			3.3 ± 0.3	3.5	3.5		
Minimum Hold Time	t_h		2.7	1.5	1.5	ns	
			3.3 ± 0.3	1.5	1.5		

AC characteristics (Input $t_r = t_f = 3ns$)

PARAMETER	SYM-BOL	TEST CONDITION	VCC (V)		Ta = 25°C			Ta = -40~85°C		UNIT
			VCC (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (LE-Q)	t_{pLH}		2.7	15	—	8.2	15.6	1.0	18.5	ns
				50	—	10.7	19.1	1.0	22.0	
	3.3 ± 0.3		15	—	6.4	10.1	1.0	12.0		
			50	—	8.9	13.6	1.0	15.5		
Propagation Delay Time (D-Q)	t_{pLH}		2.7	15	—	7.6	14.5	1.0	17.5	ns
				50	—	10.1	18.0	1.0	21.0	
	3.3 ± 0.3		15	—	5.9	9.3	1.0	11.0		
			50	—	8.4	12.8	1.0	14.5		
Output Enable Time	t_{pZL}	$R_L = 1k\Omega$	2.7	15	—	7.8	15.0	1.0	18.5	ns
				50	—	10.3	18.5	1.0	22.0	
	3.3 ± 0.3		15	—	6.1	9.7	1.0	12.0		
			50	—	8.6	13.2	1.0	15.5		
Output Disable Time	t_{pLZ} t_{pHZ}	$R_L = 1k\Omega$	2.7	50	—	12.1	19.1	1.0	22.0	ns
			3.3 ± 0.3	50	—	10.1	13.6	1.0	15.5	
Output To Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
			3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	(Note 2)			—	4	10	—	10	pF
Output Capacitance	C_{OUT}				—	6	—	—	—	pF
Power Dissipation Capacitance	C_{pD}	(Note 3)			—	29	—	—	—	pF

(Note 1) Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

(Note 2) Parameter guaranteed by design.

(Note 3) C_{pD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{pD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per Latch)}$$

And the total C_{pD} when n pcs. of Latch operate can be gained by the following equation :

$$C_{pD}(\text{total}) = 21 + 8 \cdot n$$

TC74LVX573F/FW/FS

Noise characteristics ($T_a = 25^\circ\text{C}$, Input $t_r = t_f = 3\text{ns}$, $C_L = 50\text{pF}$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	LIMIT	UNIT
			Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	-0.5	-0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V

INPUT EQUIVALENT CIRCUIT

