

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

T-46-07-11

MC54/74HC373

Octal 3-State Noninverting Transparent Latch

High-Performance Silicon-Gate CMOS

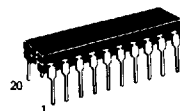
The MC54/74HC373 is identical in pinout to the LS373. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

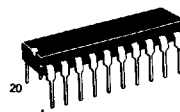
The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

The HC373 is identical in function to the HC573, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HC533, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 186 FETs or 46.5 Equivalent Gates



J SUFFIX
 CERAMIC
 CASE 732-03



N SUFFIX
 PLASTIC
 CASE 738-03

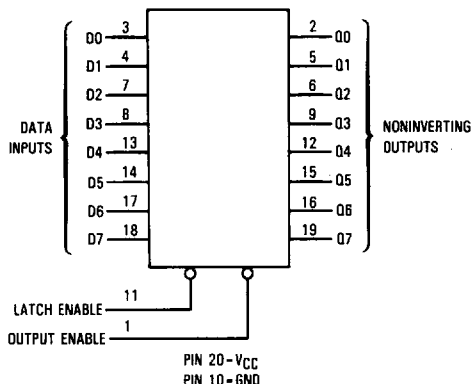
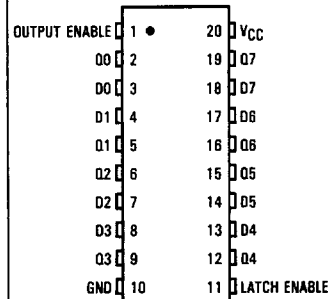


DW SUFFIX
 SOIC
 CASE 751D-03

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 6.

LOGIC DIAGRAM**PIN ASSIGNMENT****FUNCTION TABLE**

Inputs		Output	
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

X = don't care
 Z = high impedance

5

MC54/74HC373

T-46-07-11

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	-55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} =2.0 V V _{CC} =4.5 V V _{CC} =6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} =0.1 V or V _{CC} -0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} =0.1 V or V _{CC} -0.1 V I _{out} ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V _{OH}	Minimum High-Level Output Voltage	V _{in} =V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V _{in} =V _{IH} or V _{IL} I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	6.0	5.9	5.9	5.9	
			6.0	3.98	3.84	3.70	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} =V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V _{in} =V _{IH} or V _{IL} I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	6.0	0.1	0.1	0.1	
			6.0	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	V _{in} =V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
			6.0	±0.5	±5.0	±10.0	
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} =V _{IL} or V _{IH} V _{out} =V _{CC} or GND	6.0	±0.5	±5.0	±10.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} =V _{CC} or GND I _{out} =0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

5

MC5A/74HC373

T-46-07-11

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Latch) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V _{CC} = 5.0 V		pF
		41		

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, Input D to Latch Enable (Figure 4)	2.0	25	30	40	ns
		4.5	5	6	8	
		6.0	5	6	7	
t _h	Minimum Hold Time, Latch Enable to Input D (Figure 4)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t _w	Minimum Pulse Width, Latch Enable (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

MC54/74HC373

T-46-07-11

SWITCHING WAVEFORMS

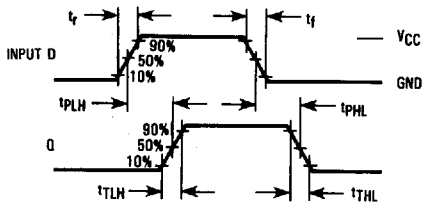


Figure 1.

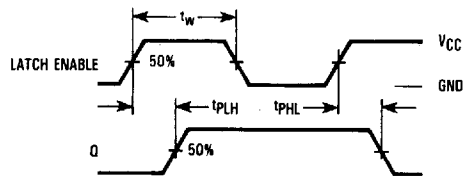


Figure 2.

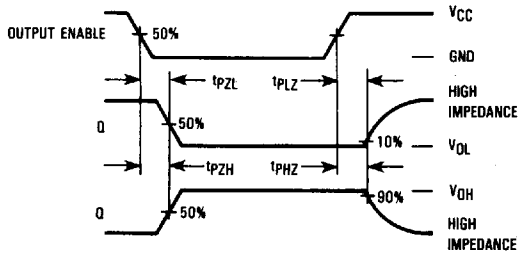


Figure 3.

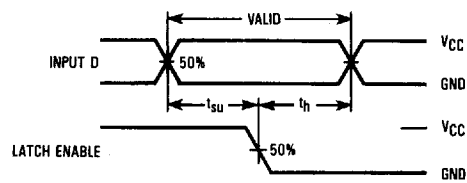
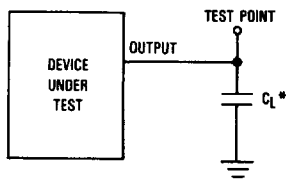


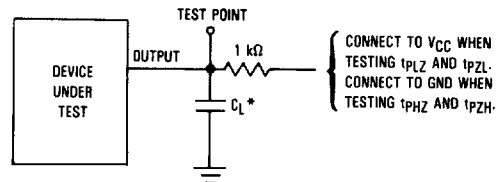
Figure 4.

TEST CIRCUITS



*Includes all probe and jig capacitance.

Figure 5.



*Includes all probe and jig capacitance.

Figure 6.

EXPANDED LOGIC DIAGRAM

