54F620, 54F623
Transceivers

54F620 – Inverting 3-State Octal Bus Transceiver
54F623 – Non-Inverting 3-State Octal Bus Transceiver

Product Specification

Military FAST Products

FEATURES

- **High-impedance NPN base inputs for reduced loading (70μA in High and Low states)**
- **Ideal for applications which require high output drive and minimal bus loading**
- **Octal bidirectional bus interface**
- **3-State buffer outputs sink 48mA and source 12mA**
  - **54F620, inverting**
  - **54F623, non-inverting**

DESCRIPTION

The 54F623 is an octal transceiver featuring non-inverting 3-State bus-compatible outputs in both send and receive directions. The outputs are capable of sinking 48mA and sourcing up to 12mA, providing very good capacitive drive characteristics. The 54F620 is an inverting version of the 54F623.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

ORDERING INFORMATION

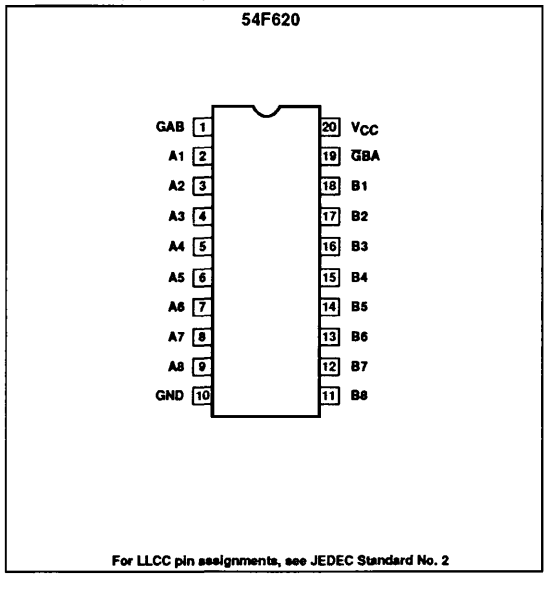
DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54F620/BRA 54F623/BRA
20-Pin Ceramic FlatPack	54F620/BSA 54F623/BSA
20-Pin Ceramic LLCC	54F620/B2A 54F623/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

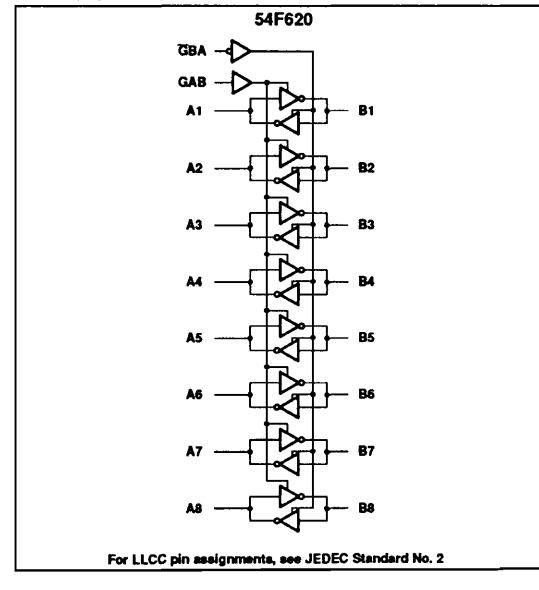
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_1 - A_8, B_1 - B_8	Data inputs	3.5/0.116	70μA/70μA
$\overline{G}BA$, GAB	3-State output enable inputs (active Low)	1.0/0.033	20μA/20μA
A_1 - A_8	Data outputs	150/40	3mA/24mA
B_1 - B_8	Data outputs	600/80	12mA/48mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

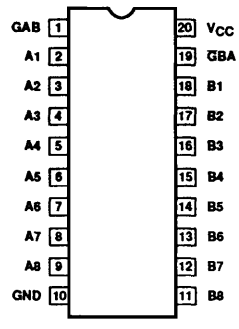


LOGIC SYMBOL



PIN CONFIGURATION

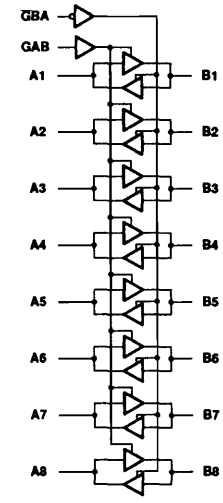
54F623



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL

54F623



For LLCC pin assignments, see JEDEC Standard No. 2

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the Enable inputs ($\overline{G}BA$ and GAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 54F620 and 54F623 the capability to store data by the simultaneous enabling of $\overline{G}BA$ and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain in their last states.

FUNCTION TABLE

ENABLE	INPUTS	OPERATION	
$\overline{G}BA$	GAB	54F620	54F623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Z	Z
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

H = High voltage level
L = Low voltage level
Z = High impedance

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage range		-0.5 to +7.0	V
V_I	Input voltage range		-0.5 to +7.0	V
I_I	Input current range		-30 to +5.0	mA
V_O	Voltage applied to output in High output state range		-0.5 to +5.5	V
I_O	Current applied to output in Low output state	$A_1 - A_8$	40	mA
		$B_1 - B_8$	96	mA
T_{STG}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage[5]		2.0			V
V_{IL}	Low-level input voltage[5]				0.7	V
I_{IK}	Input clamp current				-18	mA
I_{OH2}	High-level output current	A_1 - A_8			-3.0	mA
I_{OH1}		B_1 - B_8			-1.0	mA
I_{OH3}	High-level output current	B_1 - B_8			-12.0	mA
I_{OL}	Low-level output current	A_1 - A_8			20.0	mA
		B_1 - B_8			48.0	mA
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		A_1 - A_8	V_{CC} = Min,	I_{OH2} = -3mA	2.4			V
			B_1 - B_8	V_{IL} = Max,	I_{OH1} = -1mA	2.5	3.4		V
			B_1 - B_8	V_{IH} = Min	I_{OH3} = -12mA	2.0			V
V_{OL}	Low-level output voltage		A_1 - A_8	V_{CC} = Min, V_{IL} = Max,	I_{OL} = 20mA		0.35	0.50	V
			B_1 - B_8	V_{IH} = Min	I_{OL} = 48mA		0.40	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		$\overline{G}BA$, GAB	V_{CC} = 0.0V, V_I = 7.0V				100	µA
			Others	V_{CC} = 5.5V, V_I = 5.5V				1	mA
I_{IH1}	High-level input current		$\overline{G}BA$, GAB	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		only	V_{CC} = Max, V_I = 0.5V				-20	µA
I_{OZH} + I_{IH}	Off-state current High-level voltage applied		A_1 - A_8	V_{CC} = Max, V_O = 2.7V				70	µA
I_{OLZ} + I_{IL}	Off-state current Low-level voltage applied		B_1 - B_8	V_{CC} = Max, V_O = 0.5V				-70	µA
I_{OS}	Short-circuit output current[3]		A_1 - A_8	V_{CC} = Max		-60		-150	mA
			B1 - B8			-100		-225	mA
I_{CC}	Supply current (total)	F620	I_{CCH}	V_{CC} = Max	$\overline{G}BA$ = GAB = 4.5V; A_1 - A_8 = GND		70	92	mA
			I_{CCL}		$\overline{G}BA$ = GAB = 4.5V; A_1 - A_8 = 4.5V		84	110	mA
			I_{CCZ}		GAB = GND; $\overline{G}BA$ = A_1 - A_8 = 4.5V		70	92	mA
		F623	I_{CCH}		$\overline{G}BA$ = GAB = 4.5V; A_1 - A_8 = 4.5V		110	140	mA
			I_{CCL}		$\overline{G}BA$ = GAB = 4.5V; A_1 - A_8 = GND		110	140	mA
			I_{CCZ}		GAB = GND; $\overline{G}BA$ = A_1 - A_8 = 4.5V		99	130	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	54F620 LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	2.5 1.0	4.5 2.5	6.5 4.5	2.0 1.0	8.5 5.5	ns ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	2.5 1.0	4.5 2.5	6.5 4.5	2.0 1.0	8.5 5.5	ns ns
t_{PZH} t_{PZL}	Output enable to High or Low level $\overline{G}BA$ to A_n	Waveform 3 Waveform 4	3.0 4.0	7.5 7.5	10.5 10.5	2.5 3.5	12.5 12.5	ns ns
t_{PHZ} t_{PLZ}	Output disable from High or Low level $\overline{G}BA$ to A_n	Waveform 3 Waveform 4	2.5 2.0	4.5 4.5	7.5 7.0	2.0 1.5	9.0 8.0	ns ns
t_{PZH} t_{PZL}	Output enable to High or Low level GAB To B_n	Waveform 3 Waveform 4	4.5 4.5	7.5 7.5	10.5 10.0	4.0 4.0	12.5 12.0	ns ns
t_{PHZ} t_{PLZ}	Output disable from High or Low level GAB to B_n	Waveform 3 Waveform 4	3.0 4.0	6.5 6.5	9.5 9.5	2.5 3.5	12.0 11.5	ns ns

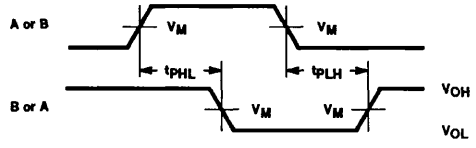
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	54F623 LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	2.0 3.0	4.0 5.0	5.5 7.0	2.0 2.5	7.0 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	2.0 2.5	4.0 4.5	5.5 6.5	2.0 2.5	7.5 8.0	ns ns
t_{PZH} t_{PZL}	Output enable to High or Low level $\overline{G}BA$ to A_n	Waveform 3 Waveform 4	5.0 5.0	8.5 7.5	10.5 9.5	5.0 5.0	13.5 11.0	ns ns
t_{PHZ} t_{PLZ}	Output disable from High or Low level $\overline{G}BA$ to A_n	Waveform 3 Waveform 4	2.5 2.5	4.5 4.5	6.5 6.5	2.5 2.5	10.0 7.5	ns ns
t_{PZH} t_{PZL}	Output enable to High or Low level GAB To B_n	Waveform 3 Waveform 4	5.0 4.5	8.0 7.0	10.0 9.0	5.0 4.5	12.5 10.0	ns ns
t_{PHZ} t_{PLZ}	Output disable from High or Low level GAB to B_n	Waveform 3 Waveform 4	3.0 4.0	6.0 7.0	8.5 9.0	3.0 4.0	11.5 11.0	ns ns

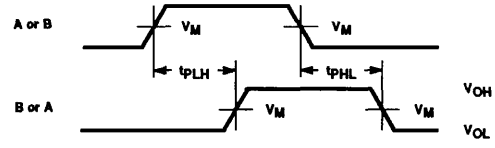
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with outputs open.
5. When testing devices to the functional table specified, refer to the 'Recommended Operating Conditions' section of Application Note 202, "Testing and Specifying FAST Logic".

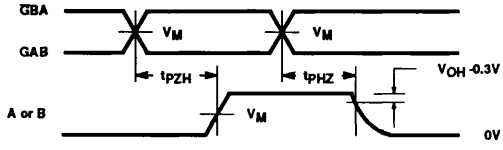
AC WAVEFORMS



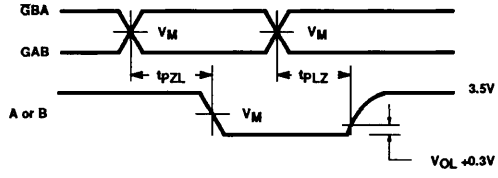
Waveform 1. For Inverting Outputs



Waveform 2. For non-Inverting Outputs



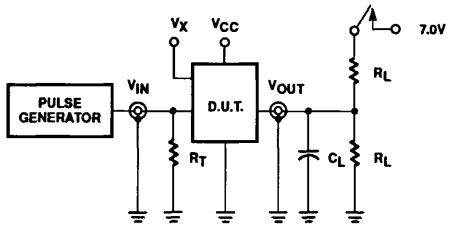
Waveform 3. 3-State Output Enable Time to High Level Output Disable Time from High Level



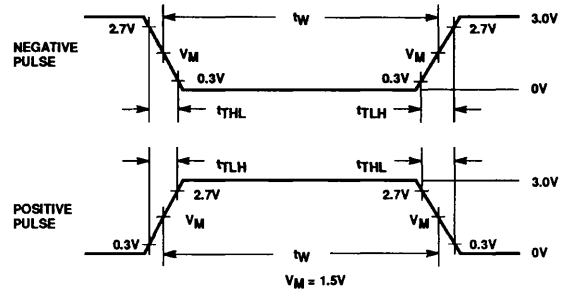
Waveform 4. 3-State Output Enable Time to Low Level Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs and Open Collector Outputs



V_M = 1.5V

Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.