

54F/74F676

16-Bit Serial/Parallel-In, Serial-Out Shift Register

General Description

The 'F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the Mode (M) input is HIGH, information present on the parallel data (P₀-P₁₅) inputs is entered on the falling edge of the Clock Pulse (CP) input signal. When M is LOW, data is shifted out of the most significant bit position while information present on the Serial (SI) input shifts into the least significant bit position. A HIGH signal on the Chip Select (CS) input prevents both parallel and serial operations.

Features

- 16-bit parallel-to-serial conversion
- 16-bit serial-in, serial-out
- Chip select control
- Slim 24 lead 300 mil package

Ordering Code: See Section 11

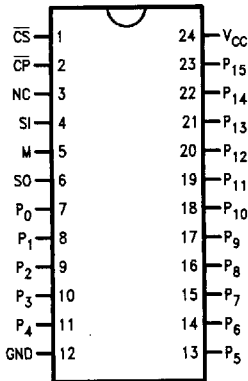
Commercial	Military	Package Number	Package Description
74F676PC		N24A	24-Lead (0.600" Wide) Molded Dual-In-Line
74F676SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F676DM (Note 2)	J24A	24-Lead (0.600" Wide) Ceramic Dual-In-Line
	54F676SDM (Note 2)	J24F	24-Lead (0.300" Wide) Ceramic Dual-In-Line
74F676SC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
	54F676FM (Note 2)	W24C	24-Lead Cerpack
	54F676LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX.

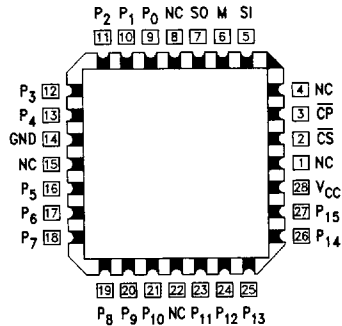
Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



Pin Assignment for LCC

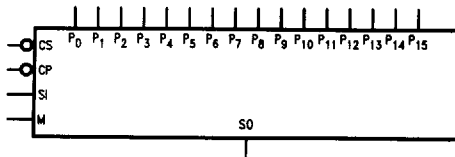


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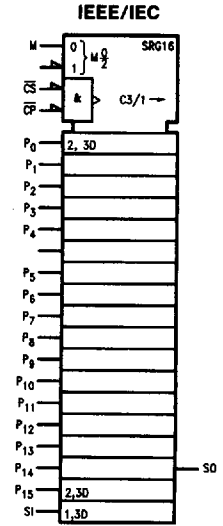
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Logic Symbols



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Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
P ₀ -P ₁₅	Parallel Data Inputs	1.0/1.0	20 μ A/ -0.6 mA
\overline{CS}	Chip Select Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
\overline{CP}	Clock Pulse Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
M	Mode Select Input	1.0/1.0	20 μ A/ -0.6 mA
SI	Serial Data Input	1.0/1.0	20 μ A/ -0.6 mA
SO	Serial Output	50/33.3	-1 mA/20 mA

Functional Description

The 16-bit shift register operates in one of three modes, as indicated in the Shift Register Operations Table.

HOLD—a HIGH signal on the Chip Select (\overline{CS}) input prevents clocking, and data is stored in the sixteen registers.

Shift/Serial Load—data present on the SI pin shifts into the register on the falling edge of \overline{CP} . Data enters the Q₀ position and shifts toward Q₁₅ on successive clocks, finally appearing on the SO pin.

Parallel Load—data present on P₀-P₁₅ are entered into the register on the falling edge of \overline{CP} . The SO output represents the Q₁₅ register output.

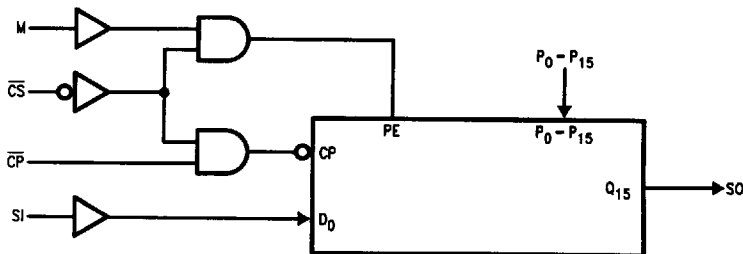
To prevent false clocking, \overline{CP} must be LOW during a LOW-to-HIGH transition of \overline{CS} .

Shift Register Operations Table

Control Input			Operating Mode
\overline{CS}	M	\overline{CP}	
H	X	X	Hold
L	L	\sim	Shift/Serial Load
L	H	\sim	Parallel Load

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 \sim = HIGH-to-LOW Transition

Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage						Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage						
V _{OH}	Output HIGH Voltage	54F 10% V _{CC}	2.5		V	Min	I _{OH} = -1 mA
		74F 10% V _{CC}	2.5				I _{OH} = -1 mA
		74F 5% V _{CC}	2.7				I _{OH} = -1 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA
		74F 10% V _{CC}		0.5			I _{OL} = 20 mA
I _{IH}	Input HIGH Current	54F		20.0	μA	Max	V _{IN} = 2.7V
		74F		5.0			
I _{BVI}	Input HIGH Current Breakdown Test	54F		100	μA	Max	V _{IN} = 7.0V
		74F		7.0			
I _{CEX}	Output HIGH Leakage Current	54F		250	μA	Max	V _{OUT} = V _{CC}
		74F		50			
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA, All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV, All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current		-60	-150	mA	Max	V _{OUT} = 0V
I _{CC}	Power Supply Current			72	mA	Max	

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	110		45		90	MHz	2-1	
t_{PLH}	Propagation Delay $\overline{\text{CP}}$ to SO	4.5	9.0	11.0	4.5	17.0	4.5	12.0	ns	2-3
t_{PHL}		5.0	9.0	12.5	5.0	14.5	5.0	13.5		

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_{\text{s}}(\text{H})$	Setup Time, HIGH or LOW SI to $\overline{\text{CP}}$	4.0		4.0		4.0		ns	2-6
$t_{\text{s}}(\text{L})$		4.0		4.0		4.0			
$t_{\text{h}}(\text{H})$	Hold Time, HIGH or LOW SI to $\overline{\text{CP}}$	4.0		4.0		4.0		ns	2-6
$t_{\text{h}}(\text{L})$		4.0		4.0		4.0			
$t_{\text{s}}(\text{H})$	Setup Time, HIGH or LOW P_n to $\overline{\text{CP}}$	3.0		3.0		3.0		ns	2-6
$t_{\text{s}}(\text{L})$		3.0		3.0		3.0			
$t_{\text{h}}(\text{H})$	Hold Time, HIGH or LOW P_n to $\overline{\text{CP}}$	4.0		4.0		4.0		ns	2-6
$t_{\text{h}}(\text{L})$		4.0		4.0		4.0			
$t_{\text{s}}(\text{H})$	Setup Time, HIGH or LOW M to $\overline{\text{CP}}$	8.0		8.0		8.0		ns	2-6
$t_{\text{s}}(\text{L})$		8.0		8.0		8.0			
$t_{\text{h}}(\text{H})$	Hold Time, HIGH or LOW M to $\overline{\text{CP}}$	2.0		2.0		2.0		ns	2-6
$t_{\text{h}}(\text{L})$		2.0		2.0		2.0			
$t_{\text{s}}(\text{L})$	Setup Time, LOW $\overline{\text{CS}}$ to $\overline{\text{CP}}$	10.0		12.0		10.0		ns	2-6
$t_{\text{h}}(\text{H})$	Hold Time, HIGH $\overline{\text{CS}}$ to $\overline{\text{CP}}$	10.0		10.0		10.0			
$t_{\text{w}}(\text{H})$	$\overline{\text{CP}}$ Pulse Width HIGH or LOW	4.0		5.0		4.0		ns	2-4
$t_{\text{w}}(\text{L})$		6.0		9.0		6.0			