

TC74LCX16373AFT

Low Voltage 16-Bit D-TYPE LATCH with 5V Tolerant Inputs and Outputs

The TC74LCX16373AFT is a high performance CMOS 16-bit D-TYPE LATCH. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

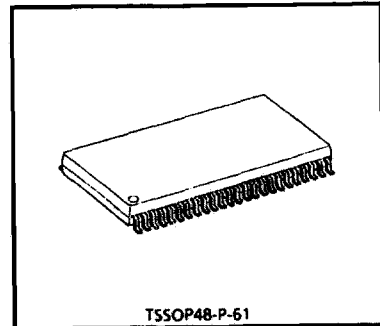
The device is designed for low voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs.

This 16-bit D-type latch is controlled by a latch enable input (LE) and an output enable input (\overline{OE}) which are common to each byte. It can be used as two 8-bit latches or one 16-bit latch. When the \overline{OE} input is high, the outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge.

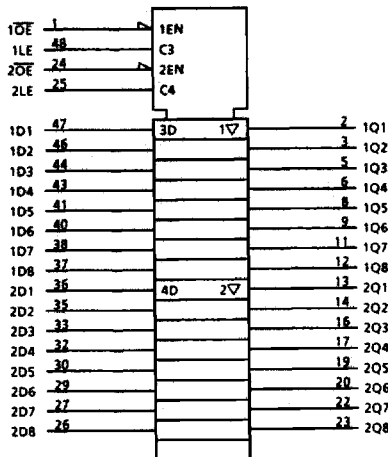
Features

- Low Voltage Operation: $V_{CC} = 2.0 \sim 3.6V$
- High Speed: $t_{pd} = 7.0ns$ (Max.) at $V_{CC} = 3.0 \sim 3.6V$
- Output Current: $I_{OH}/I_{OL} = 24mA$ (Min.) $V_{CC} = 3.0V$
- Latch up Performance: $\pm 500mA$
- Package: TSSOP (Thin Shrink Small Outline Package)
- Power down protection is provided on all inputs and outputs.

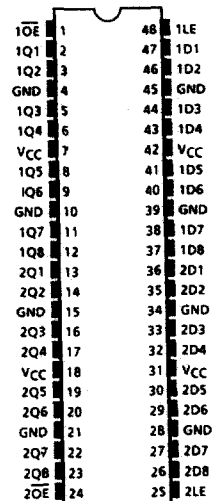


TSSOP48-P-61

Weight : 0.25 g (Typ.)



IEC Logic Symbol



(TOP VIEW)

Pin Assignment

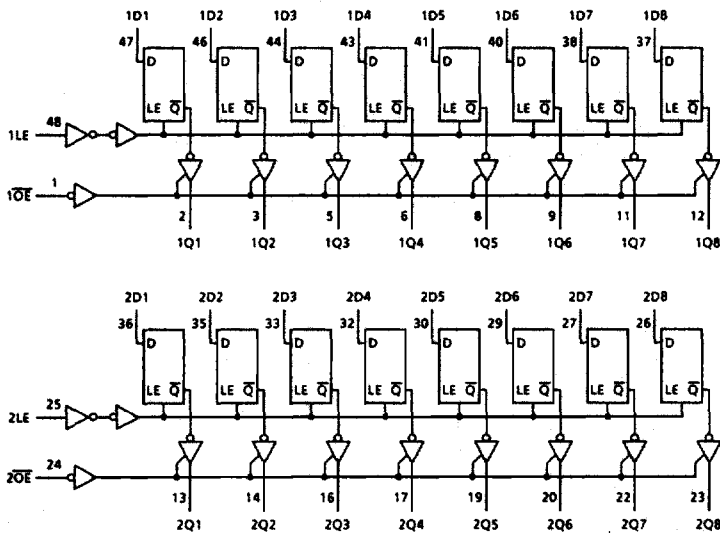
Truth Table

| Input | | | Output |
|------------------|-----|-----------|-----------|
| $\overline{1OE}$ | 1LE | 1D1 - 1D8 | 1Q1 - 1Q8 |
| H | X | X | Z |
| L | L | X | Qn |
| L | H | L | L |
| L | H | H | H |

| Input | | | Output |
|------------------|-----|-----------|-----------|
| $\overline{2OE}$ | 2LE | 2D1 - 2D8 | 2Q1 - 2Q8 |
| H | X | X | Z |
| L | L | X | Qn |
| L | H | L | L |
| L | H | H | H |

X : Don't Care
 Z : High Impedance
 Qn : No Change

System Diagram



Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|--|------------------|----------------------------|------|
| Power Supply Voltage | V_{CC} | -0.5 - 7.0 | V |
| DC Input Voltage | V_{IN} | -0.5 - 7.0 | V |
| DC Bus I/O Voltage | $V_{I/O}$ | -0.5 - 7.0 (*1) | V |
| | | -0.5 - $V_{CC} + 0.5$ (*2) | |
| Input Diode Current | I_{IK} | -50 | mA |
| Output Diode Current | I_{OK} | ±50 (*3) | mA |
| DC Output Current | I_{OUT} | ±50 | mA |
| Power Dissipation | P_D | 400 | mW |
| DC V_{CC} /Ground Current Per Supply Pin | I_{CC}/I_{GND} | ±100 | mA |
| Storage Temperature | T_{stg} | -65 - 150 | °C |

(*1) Off-State

(*2) High or Low State. I_{OUT} absolute maximum rating must be observed(*3) $V_{OUT} < GND$, $V_{OUT} > V_{CC}$ **Recommended Operating Range**

| Parameter | Symbol | Rating | Unit |
|--------------------------|-----------------|-------------------|------|
| Supply Voltage | V_{CC} | 2.0 - 3.6 | V |
| | | 1.5 - 3.6 (*4) | |
| Input Voltage | V_{IN} | 0 - 5.5 | V |
| Bus I/O Voltage | $V_{I/O}$ | 0 - 5.5 (*5) | V |
| | | 0 - V_{CC} (*6) | |
| Output Current | I_{OH}/I_{OL} | ±24 (*7) | mA |
| | | ±12 (*8) | |
| Operating Temperature | T_{opr} | -40 - 85 | °C |
| Input Rise and Fall Time | dt/dv | 0 - 10 (*9) | ns/V |

(*4) Data Retention Only

(*5) Off-State

(*6) High or Low State

(*7) $V_{CC} = 3.0 - 3.6V$ (*8) $V_{CC} = 2.7 - 3.0V$ (*9) $V_{IN} = 0.8 - 2.0V$, $V_{CC} = 3.0V$

Electrical Characteristics

DC Characteristics (Ta = -40 ~ 85°C)

| Parameter | Symbol | Test Condition | | V _{CC} (V) | Min. | Max. | Unit | |
|---------------------------------------|------------------|--|---|--------------------------|-----------|-----------------------|------|---|
| | | | | | | | | |
| Input Voltage | "H" Level | V _{IH} | | 2.7 - 3.6 | 2.0 | - | V | |
| | "L" Level | V _{IL} | | 2.7 - 3.6 | - | 0.8 | V | |
| Output Voltage | "H" Level | V _{OH} | V _{IN} = V _{IH} or V _{IL} | I _{OH} = -100μA | 2.7 - 3.6 | V _{CC} - 0.2 | - | V |
| | | | | I _{OH} = -12mA | 2.7 | 2.2 | - | |
| | | | | I _{OH} = -18mA | 3.0 | 2.4 | - | |
| | | | | I _{OH} = -24mA | 3.0 | 2.2 | - | |
| "L" Level | V _{OL} | V _{IN} = V _{IH} or V _{IL} | I _{OL} = 100μA | 2.7 - 3.6 | - | 0.2 | V | |
| | | | I _{OL} = 16mA | 3.0 | - | 0.4 | | |
| | | | I _{OL} = 12mA | 2.7 | - | 0.4 | | |
| | | | I _{OH} = 24mA | 3.0 | - | 0.55 | | |
| Input Leakage Current | I _{IN} | | V _{IN} = 0 - 5.5V | 2.7 - 3.6 | - | ±5.0 | μA | |
| 3-State Output Off-State Current | I _{OZ} | | V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 - 5.5V | 2.7 - 3.6 | - | ±5.0 | μA | |
| Power Off Leakage Current | I _{OFF} | | V _{IN} V _{OUT} = 5.5V | 0 | - | 10.0 | μA | |
| Quiescent Supply Current | I _{CC} | | V _{IN} = V _{CC} or GND | 2.7 - 3.6 | - | 20.0 | μA | |
| | | | V _{IN} V _{OUT} = 3.6 - 5.5V | 2.7 - 3.6 | - | ±20.0 | | |
| Increase in I _{CC} per Input | ΔI _{CC} | | V _{IH} = V _{CC} - 0.6V | 2.7 - 3.6 | - | 500 | μA | |

AC Electrical Characteristics (Ta = -40 ~85°C)

| Parameter | Symbol | Test Condition | V _{CC} (V) | Min. | Max. | Unit |
|---------------------------------|--|----------------|---------------------|------|------|------|
| | | | | | | |
| Propagation Delay Time (D - Q) | t _{pLH} t _{pHL} | (Fig. 1, 2) | 2.7 | — | 8.0 | ns |
| | | | 3.3±0.3 | 1.5 | 7.0 | |
| Propagation Delay Time (LE - Q) | t _{pLH} t _{pHL} | (Fig. 1, 2) | 2.7 | — | 8.0 | ns |
| | | | 3.3±0.3 | 1.5 | 7.0 | |
| 3-State Output Enable Time | t _{pZL} t _{pZH} | (Fig. 1, 3) | 2.7 | — | 8.2 | ns |
| | | | 3.3±0.3 | 1.5 | 7.2 | |
| 3-State Output Disable Time | t _{pLZ} t _{pHZ} | (Fig. 1, 3) | 2.7 | — | 8.2 | ns |
| | | | 3.3±0.3 | 1.5 | 7.2 | |
| Minimum Pulse Width (LE) | t _{w(H)} t _{w(H)} | (Fig. 1, 2) | 2.7 | 3.0 | — | ns |
| | | | 3.3±0.3 | 3.0 | — | |
| Minimum Setup Time | t _s | (Fig. 1, 2) | 2.7 | 2.5 | — | ns |
| | | | 3.3±0.3 | 2.5 | — | |
| Minimum Hold Time | t _h | (Fig. 1, 2) | 2.7 | 1.5 | — | ns |
| | | | 3.3±0.3 | 1.5 | — | |
| Output to Output Skew | t _{osLH} t _{osHL} | (*10) | 2.7 | — | — | ns |
| | | | 3.3±0.3 | — | 1.0 | |

(*10) Parameter guaranteed by design. (t_{osLH} = t_{pLHm} - t_{pLHn}, t_{osHL} = t_{pHLm} - t_{pHLn})

Dynamic Switching Characteristics (Ta = 25°C, Input t_r = t_f = 2.5ns, C_L = 50pF, R_L = 500Ω)

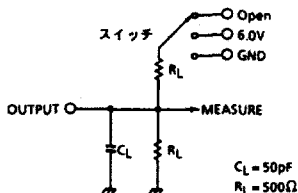
| Parameter | Symbol | Test Condition | V _{CC} (V) | Typical | Unit |
|--|------------------|--|---------------------|---------|------|
| | | | | | |
| Quiet Output Maximum Dynamic V _{OL} | V _{OLP} | V _{IH} = 3.3V, V _{IL} = 0V | 3.3 | 0.8 | V |
| Quiet Output Minimum Dynamic V _{OL} | V _{OLV} | V _{IH} = 3.3V, V _{IL} = 0V | 3.3 | 0.8 | V |

Capacitive Characteristics (Ta = 25°C)

| Parameter | Symbol | Test Condition | V _{CC} (V) | Typical | Unit |
|-------------------------------|------------------|-------------------------------|---------------------|---------|------|
| | | | | | |
| Input Capacitance | C _{IN} | — | 3.3 | 7 | pF |
| Bus Input Capacitance | C _{OUT} | | 3.3 | 8 | pF |
| Power Dissipation Capacitance | C _{PD} | f _{IN} = 10MHz (*11) | 3.3 | 25 | pF |

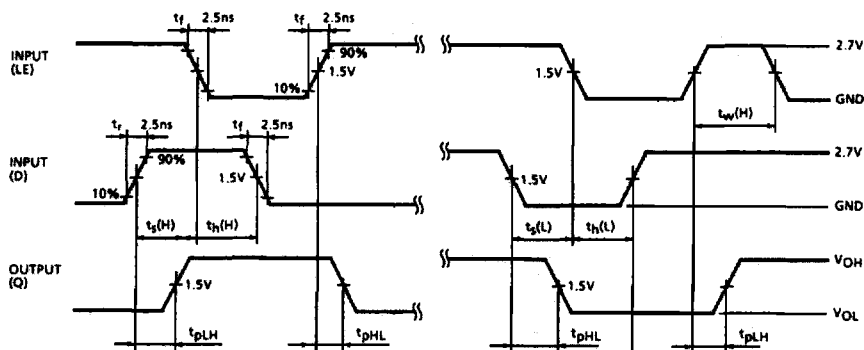
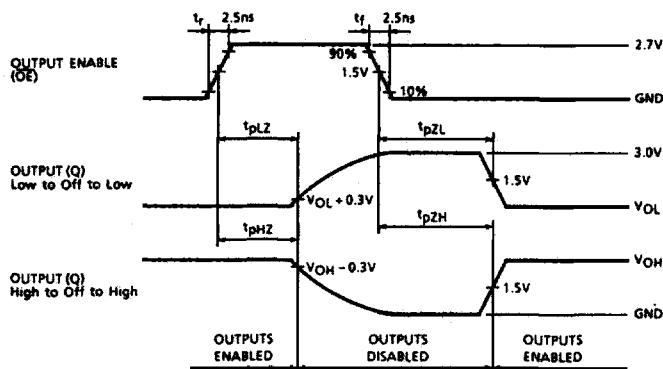
(*11) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = C_{PD} • V_{CC} • f_{IN} + I_{CC}/16 (per latch)

Fig.1 Test circuit



| Parameter | Switch |
|-----------------------|--------|
| t_{pLH} , t_{pHL} | Open |
| t_{pLZ} , t_{pZL} | 6.0V |
| t_{pHZ} , t_{pZH} | GND |
| t_w , t_s , t_h | Open |

AC wave form

Fig.2 t_{pLH} , t_{pHL} , t_w , t_s , t_h Fig.3 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH} 

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