Features

- ESD Protect for 4 high-speed I/O channels
- Provide ESD protection for each channel to
  IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-4 (EFT) (5/50ns) Level-3, 20A for I/O, 40A for Power
  IEC 61000-4-5 (Lightning) 6A (8/20μs)
- 5V operating voltage
- Low capacitance : 1.2pF typical
- Fast turn-on and Low clamping voltage
- Array of surge rated diodes with internal equivalent TVS diode
- Small package saves board space
- Solid-state silicon-avalanche and active circuit triggering technology
- Green part available

Applications

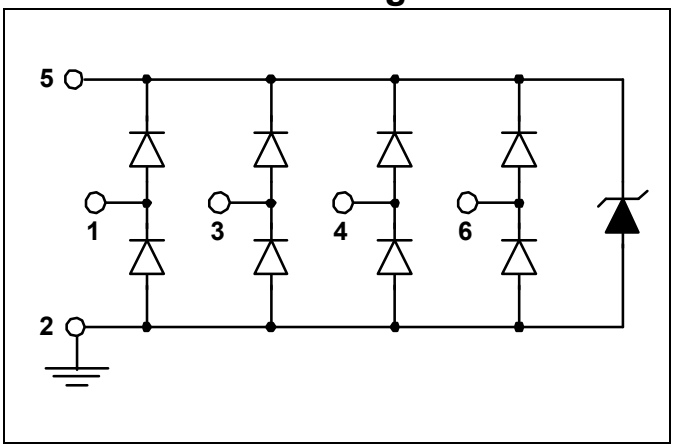
- USB2.0 Power and Data lines protection
- Notebook and PC Computers
- Monitors and Flat Panel Displays
- IEEE 1394 Firewire Ports
- Video Graphics Cards
- SIM ports

Description

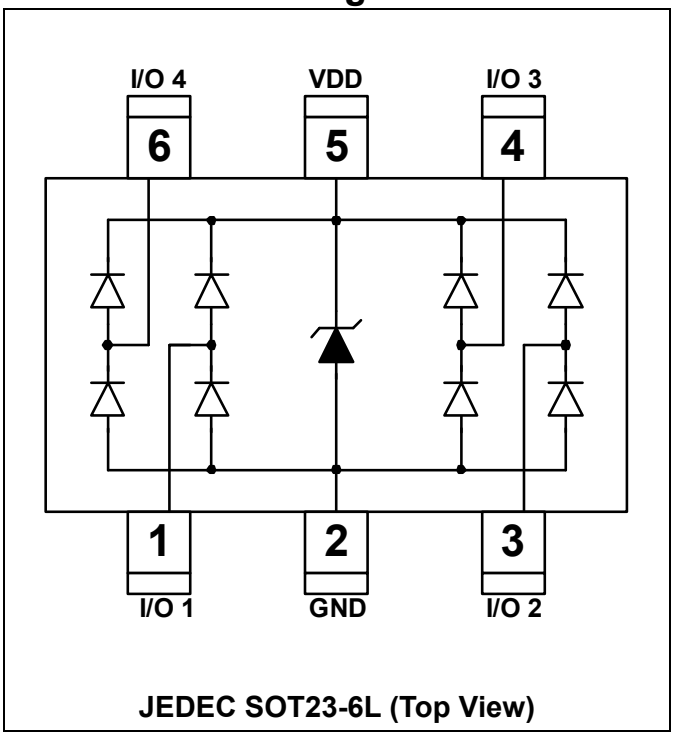
AZC002-04S is a high performance and low cost design which includes surge rated diode arrays to protect high speed data interfaces. The AZC002-04S family has been specifically designed to protect sensitive components, which are connected to data and transmission lines, from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

AZC002-04S is a unique design which includes surge rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the power supply line or to the ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components. AZC002-04S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (± 15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



JEDEC SOT23-6L (Top View)

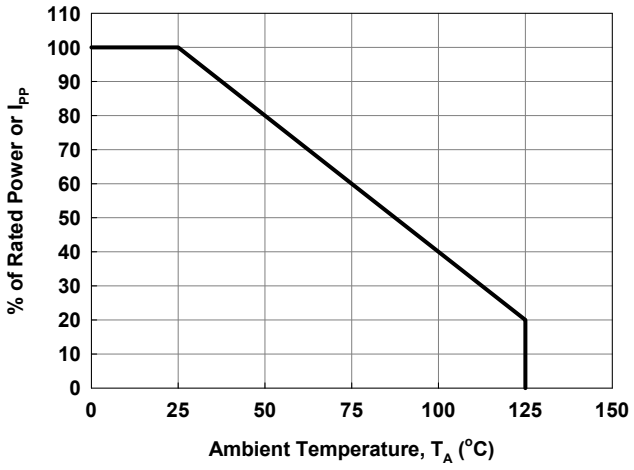
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20μs)	I_{PP}	6	**A**
Operating Supply Voltage (VDD-GND)	V_{DC}	6	**V**
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	17 12	**kV**
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	**°C**
Operating Temperature	T_{OP}	-55 to +85	**°C**
Storage Temperature	T_{STO}	-55 to +150	**°C**
DC Voltage at any I/O pin	V_{IO}	(GND – 0.5) to (VDD + 0.5)	**V**

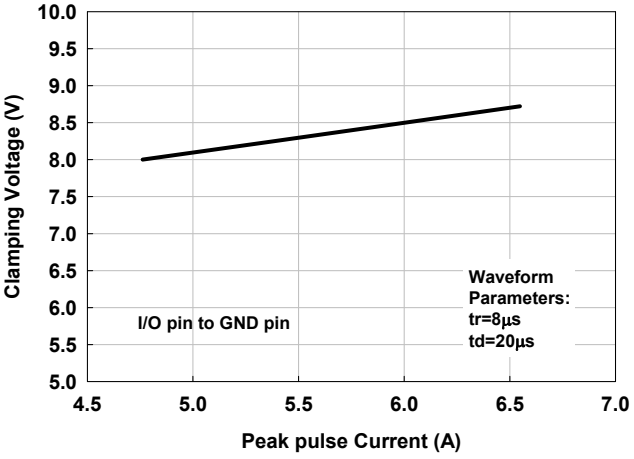
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Pin 5 to pin 2, T=25 °C			5	**V**
Reverse Leakage Current	I_{Leak}	V_{RWM} = 5V, T=25 °C, Pin 5 to pin 2			2	**μA**
Channel Leakage Current	I_{CH_Leak}	$V_{Pin\ 5}$ = 5V, $V_{Pin\ 2}$ = 0V, T=25 °C			1	**μA**
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C Pin 5 to Pin 2	6.2			**V**
Forward Voltage	V_F	I_F = 15mA, T=25 °C Pin 2 to Pin 5		0.8	1	**V**
Clamping Voltage	V_{CL}	I_{PP}=5A, tp=8/20μs, T=25 °C Any Channel pin to Ground		8.1	9	**V**
ESD Holding Voltage	V_{hold}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, Any Channel pin to Ground.		13		**V**
Channel Input Capacitance	C_{IN}	V_{pin5} = 5V, V_{pin2} = 0V, **V_{IN} = 2.5V**, f = 1MHz, T=25 °C, Any Channel pin to Ground		1.2	1.4	**pF**
Channel to Channel Input Capacitance	C_{CROSS}	V_{pin5} = 5V, V_{pin2} = 0V, **V_{IN} = 2.5V**, f = 1MHz, T=25 °C , Between Channel pins		0.1	0.12	**pF**
Variation of Channel Input Capacitance	$\triangle C_{IN}$	V_{pin5} = 5V, V_{pin2} = 0V, **V_{IN} = 2.5V**, f = 1MHz, T=25 °C , Channel_x pin to Ground - Channel_y pin to Ground		0.04	0.06	**pF**

Typical Characteristics

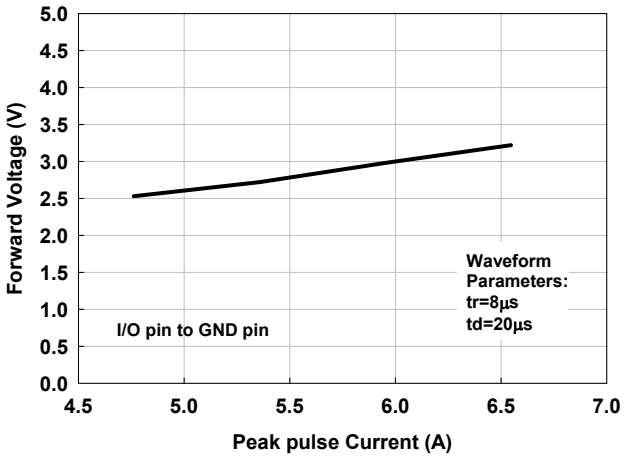
Power Derating Curve



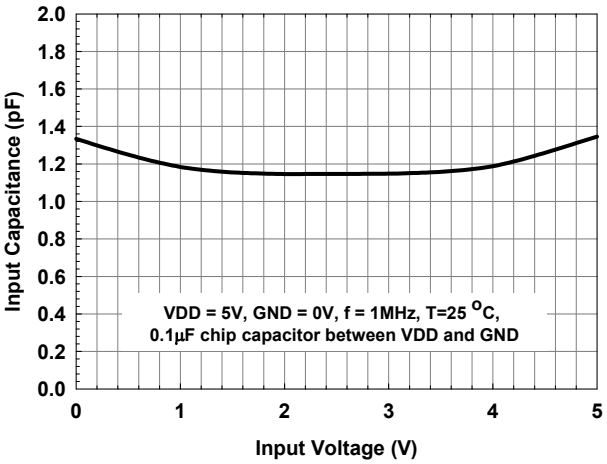
Clamping Voltage vs. Peak Pulse Current



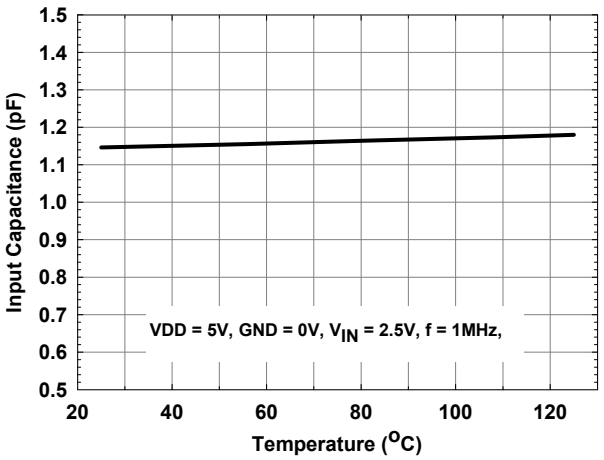
Forward Voltage vs. Forward Current



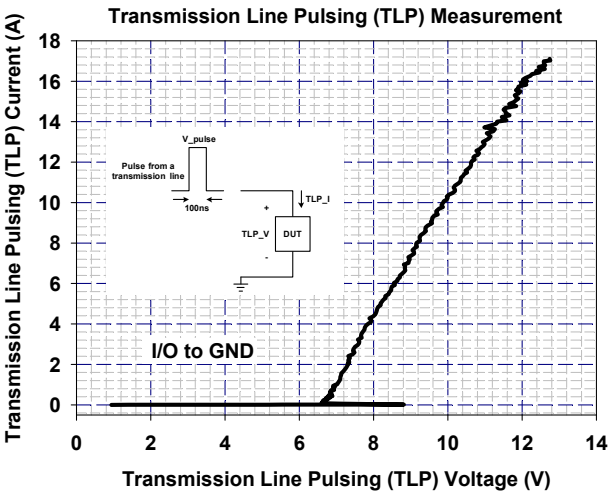
Typical Variation of C_{IN} vs. V_{IN}



Typical Variation of C_{IN} vs. Temp



Transmission Line Pulsing (TLP) Measurement



Applications Information

A. Design Considerations

The ESD protection scheme for system I/O connector is shown in the Fig. 1. In Fig. 1, the diodes D1 and D2 are general used to protect data line from ESD stress pulse. If the power-rail ESD clamping circuit is not placed between VDD and GND rails, the positive pulse ESD current (I_{ESD1}) will pass through the ESD current path1. Thus, the ESD clamping voltage V_{CL} of data line can be described as follow:

V_{CL} = Fwd voltage drop of D1 + supply voltage of VDD rail + $L_1 \times d(I_{ESD1})/dt + L_2 \times d(I_{ESD1})/dt$

Where L_1 is the parasitic inductance of data line, and L_2 is the parasitic inductance of VDD rail.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30A in 1ns. Here $d(I_{ESD1})/dt$ can be approximated by $\Delta I_{ESD1}/\Delta t$, or 30/(1x10-9). So just 10nH of total parasitic inductance (L_1 and L_2 combined) will lead to over 300V increment in V_{CL}! Besides, the ESD pulse current which is directed into the VDD rail may potentially damage any components that are attached to that rail. Moreover, it is common for the forward voltage drop of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. Of course, the discrete diode is also possible to be destroyed due to its power dissipation capability is exceeded.

The AZC002-04S has an integrated power-rail ESD clamped circuit between VDD and GND rails. It can successfully overcome previous disadvantages. During an ESD event, the positive ESD pulse current (I_{ESD2}) will be directed through the integrated power-rail ESD clamped circuit to GND rail (ESD current path2). The clamping voltage V_{CL} on the data line is small and protected IC will not be damaged because power-rail ESD clamped circuit offer a low impedance path to discharge ESD pulse current.

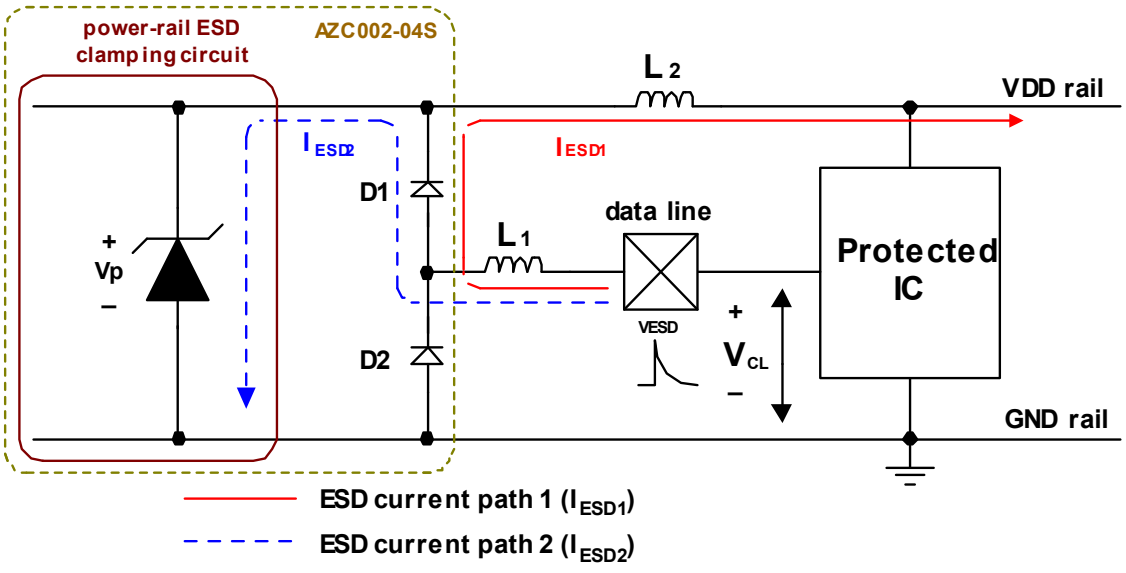


Fig. 1 Application of positive ESD pulse between data line and GND rail.

B. Device Connection

The AZC002-04S is designed to protect four data lines and power rails from transient over-voltage (such as ESD stress pulse). The device connection of AZC002-04S is shown in the Fig. 2. In Fig. 2, the four protected data lines are connected to the ESD protection pins (pin1, pin3, pin4, and pin6) of AZC002-04S. The ground pin (pin2) of AZC002-04S is a negative reference pin. This pin should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible. In addition, the power pin (pin 5) of AZC002-04S is a positive reference pin. This pin should directly connect to the VDD rail of PCB. When pin 5 of AZC002-04S is connected to the VDD rail, the leakage current of ESD protection pin of AZC002-04S becomes very small. Because the pin 5 of AZC002-04S is directly connected to VDD rail, the VDD rail also can be protected by the power-rail ESD clamped circuit (not shown) of AZC002-04S.

AZC002-04S can provide protection for 4 I/O signal lines simultaneously. If the number of I/O signal lines is less than 4, the unused I/O pins can be simply left as NC pins.

In some cases, systems are not allowed to be reset or restart after the ESD stress directly applying at the I/O-port connector. Under this situation, in order to enhance the sustainable ESD Level, a 0.1μF chip capacitor can be added between the VDD and GND rails. The place of this chip capacitor should be as close as possible to the AZC002-04S.

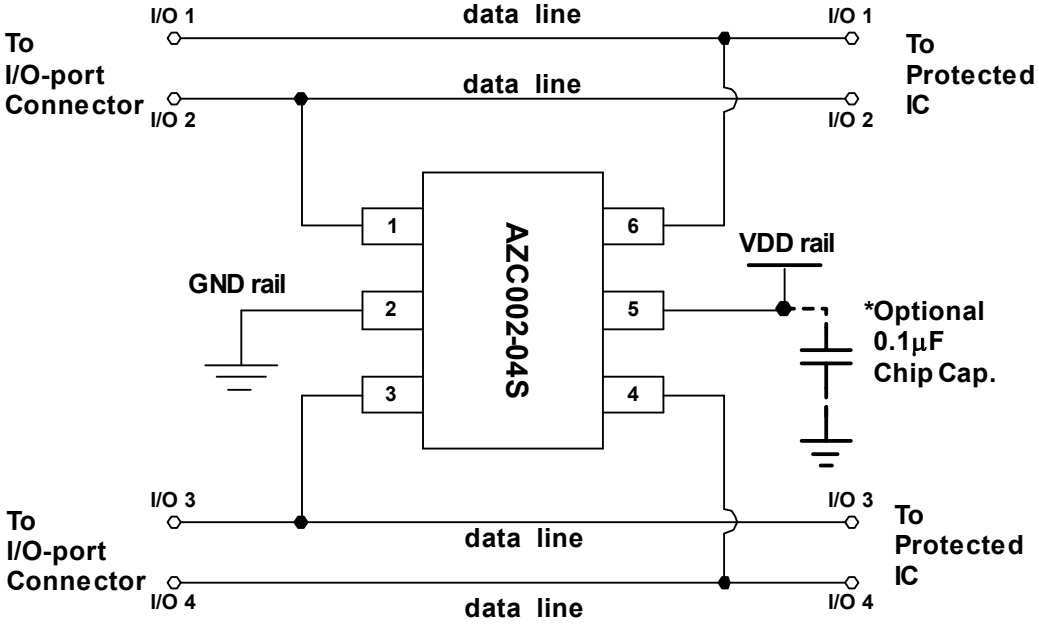


Fig. 2 Data lines and power rails connection of AZC002-04S.

C. Applications

1. Universal Serial Bus (USB) ESD Protection

The AZC002-04S can be used to protect the USB port on the monitors, computers, peripherals or portable systems. The ESD protection scheme for dual USB ports is shown in Fig. 3. In the Fig.3, each device will protect up two USB ports. The voltage bus (V_{BUS}) of USB ports (port1 and port2) are connected to the power pin (pin 5) of AZC002-04S. Each data line (D+/D-) of USB port is connected to the ESD protection pin of AZC002-04S.

When ESD voltage pulse appears on the data line, the ESD pulse current will be conducted by AZC002-04S away from the USB controller chip. In addition, the ESD pulse current also can be conducted by AZC002-04S away from the USB controller chip when the ESD voltage pulse appears on the voltage bus (V_{BUS}) of USB port. Therefore, the data lines (D+/D-) and voltage bus (V_{BUS}) of two USB ports are complementally protected with an AZC002-04S.

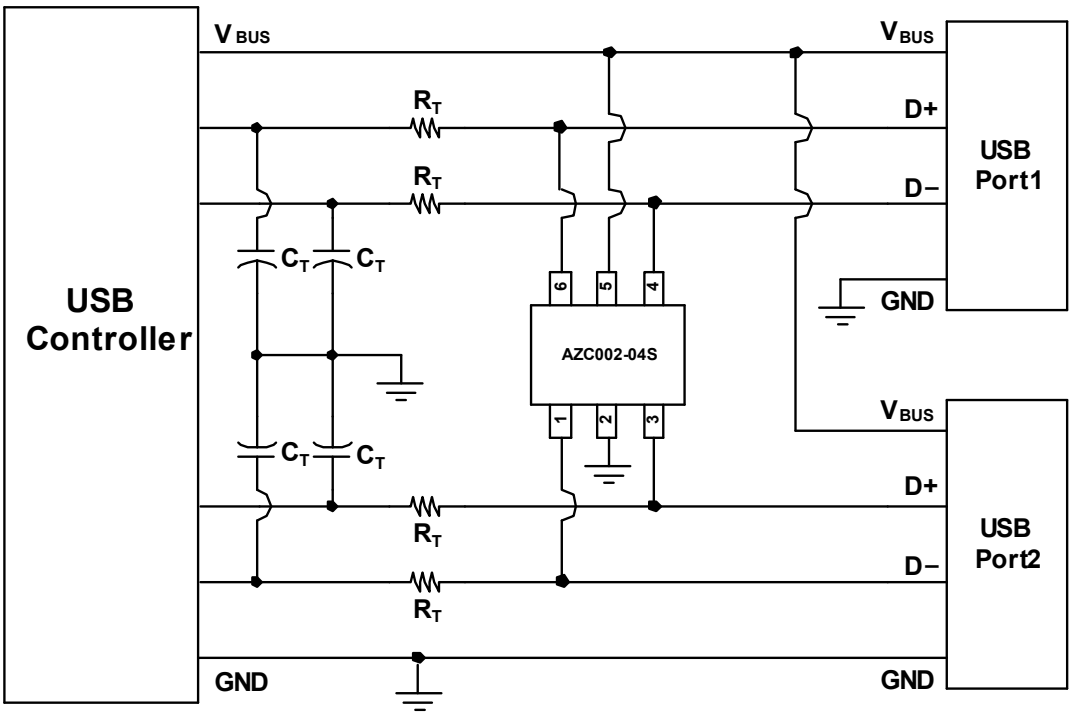


Fig. 3 ESD Protection scheme for dual USB ports by using AZC002-04S.

2. Audio Interface ESD Protection

For the audio interface, the Right/Left channel and TMC terminals should be protected from the ESD stress. The AZC002-04S can be used for the audio interface ESD protection. The ESD protection scheme for audio interface is shown in the Fig. 4. In the Fig. 4, the Right and Left channels of audio connector are connected to ESD protection pins (such as pin 1 and pin 6) of AZC002-04S. In addition, the TMC terminals of audio connector are also connected to ESD protection pins (such as pin 3 and pin 4) of AZC002-04S. For the power pin (pin 5) of AZC002-04S, it should directly connect to the VDD power supply.

When ESD voltage pulse appears on the Right/Left channel or TMC terminals of audio connector, the ESD pulse current will be discharged by AZC002-04S. Therefore, the Right/Left channel and TMC terminals of audio chip are complementally protected with an AZC002-04S.

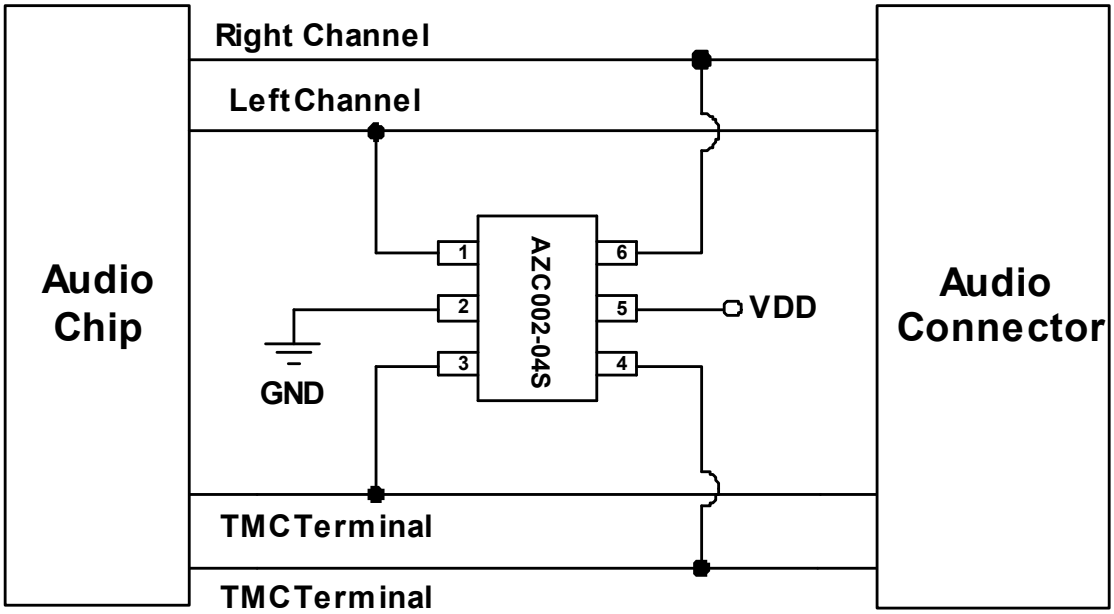


Fig. 4 ESD Protection scheme for audio interface by using AZC002-04S.

3. Video (VGA) Interface ESD Protection

For the video (VGA) interface, the exposed lines such as Red, Green, Blue, H-Sync, V-Sync, DDC CLK, and DDC DAT lines for plug and monitors should be protected from the ESD stress. The AZC002-04S also can be used for the video (VGA) interface ESD protection. The ESD protection scheme for video (VGA) interface is shown in the Fig. 5. In Fig. 5, each exposed line of video interface should connect to the ESD protection pin of AZC002-04S. The power pin (pin 5) of AZC002-04S just directly connected to the VDD power supply.

When ESD voltage appears on the signal line, the ESD pulse current will be discharged by AZC002-04S. Therefore, all exposed lines of video interface are complementally protected with an AZC002-04S.

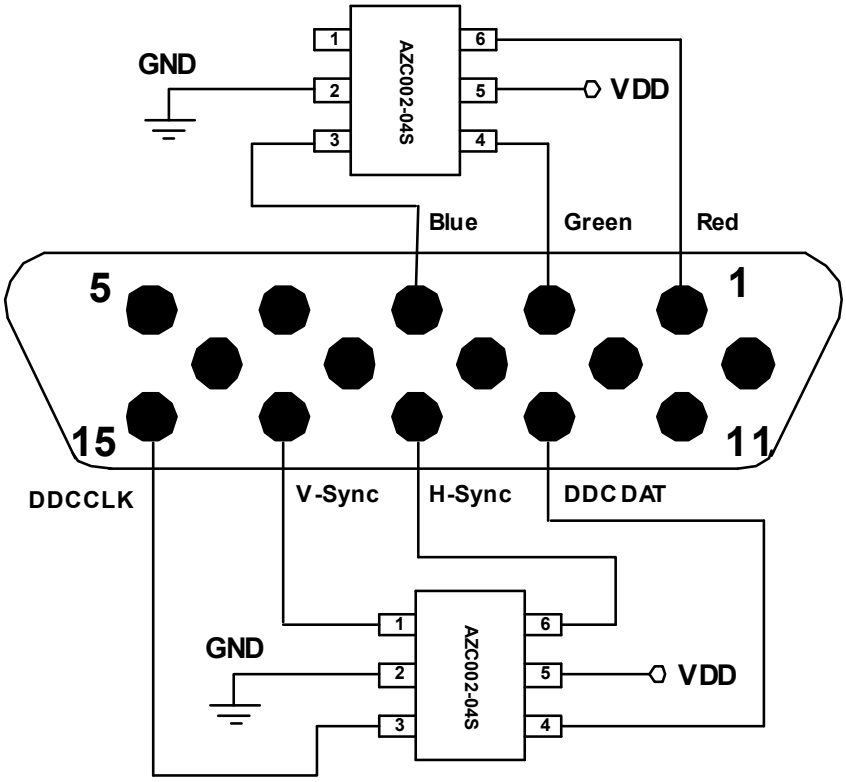


Fig. 5 ESD Protection scheme for video (VGA) interface by using AZC002-04S.

4. SIM Port ESD Protection

The AZC002-04S can be also used to protect the SIM port. The ESD protection scheme for a SIM port is shown in Fig. 6. In the Fig.6, the voltage bus (VCC) of SIM port is connected to the power pin (pin 5) of AZC002-04S. The ground bus (GND) of SIM port is connected to the ground pin (pin 2) of AZC002-04S. The other three signal lines, I/O, Clock, and Reset, are connected three ESD protection pins of AZC002-04S, respectively. The rest ESD protection pin of AZC002-04S is left to be floated.

When ESD voltage pulse appears on the one of the signal lines, the ESD pulse current will be conducted by AZC002-04S away from the controller chip. In addition, the ESD pulse current also can be conducted by AZC002-04S away from the controller chip when the ESD voltage pulse appears on the voltage bus (VCC) of SIM port. Therefore, the signal lines (I/O, Clock, and Reset) and voltage bus (VCC) of the SIM ports are all protected with an AZC002-04S.

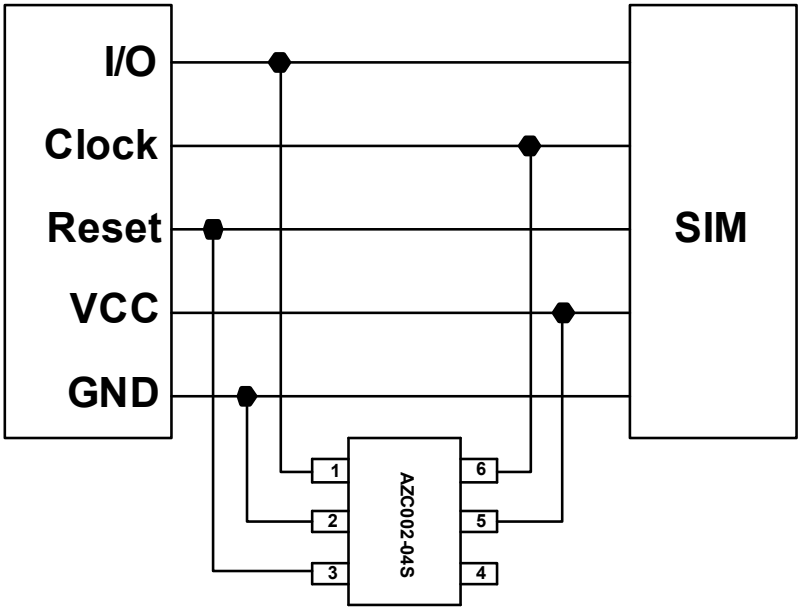


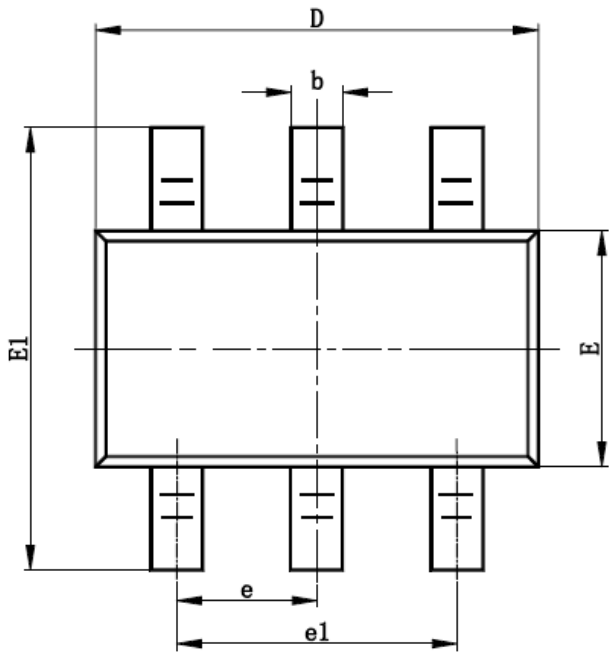
Fig. 6 ESD Protection scheme for SIM port by using AZC002-04S

Mechanical Details

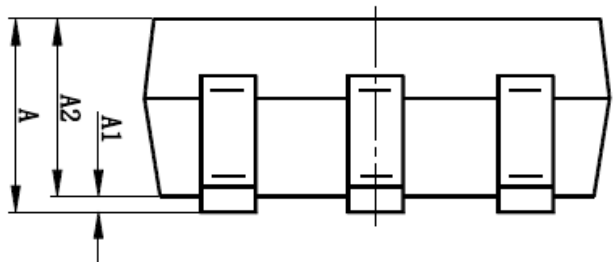
SOT23-6L

PACKAGE DIAGRAMS

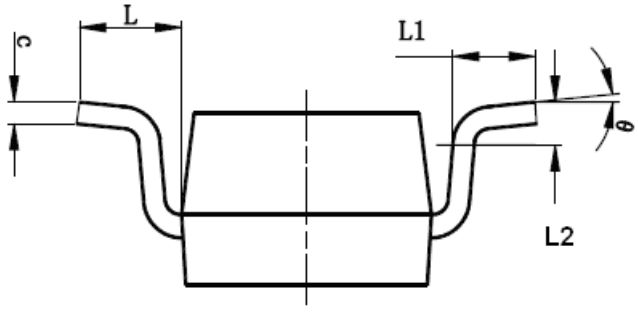
TOP VIEW



SIDE VIEW



END VIEW



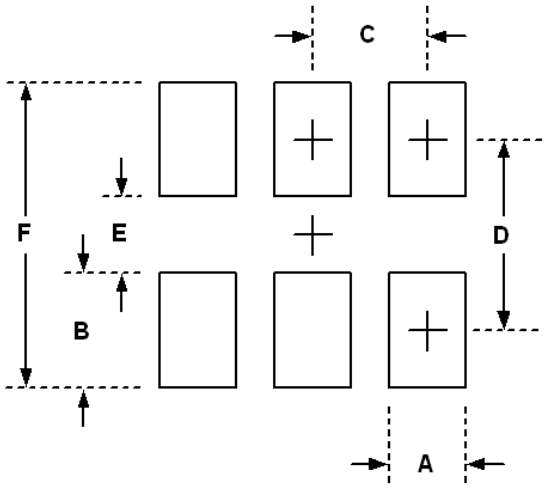
PACKAGE DIMENSIONS

SYMBOL	Millimeters		
	MIN.	NOMINAL	MAX.
A	-	-	1.45
A1	0	-	0.15
A2	0.90	1.15	1.30
b	0.30	0.40	0.45
c	0.08	0.13	0.20
D	2.90 BSC		
E	1.60 BSC		
E1	2.80 BSC		
e	0.95 BSC		
e1	1.90 BSC		
L1	0.30	0.45	0.60
L	0.60 REF		
L2	0.25 BSC		
θ	0^o	4^o	8^o

Notes:

- This dimension complies with JEDEC outline standard MO-178 Variation AB.
- Dimensioning and tolerancing per ASME Y14.5M-1994.

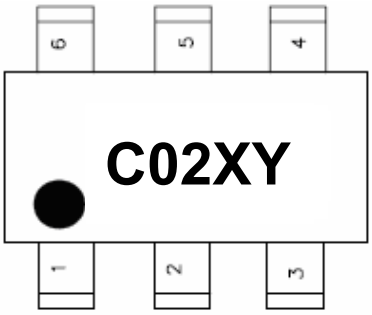
LAND LAYOUT



Dimensions		
Index	**Millimeter**	**Inches**
A	0.60	0.024
B	1.10	0.043
C	0.95	0.037
D	2.50	0.098
E	1.40	0.055
F	3.60	0.141

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



C02 = Device Code
X = Date Code
Y = Control Code

Part Number	Marking Code
AZC002-04S	C02XY
AZC002-04S (Green part)	C08XY

Revision History

Revision	Modification Description
Revision 2006/12/08	Original Release.
Revision 2007/01/23	1. Add EFT characterization. 2. Update the Absolute Max. Ratings: I_{PP}, V_{ESD}, and T_{OP}. 3. Update the values of V_{BV}, V_{CL}, C_{IN}, and C_{CROSS} in Electrical Characteristics. 4. Update the Clamping Voltage, Forward Voltage and C_{IN} vs V_{IN} curves. 5. Add the TLP characterization.
Revision 2007/02/02	1. Add characterization of C_{IN} vs temp.
Revision 2007/05/15	Update the Marking Code from C02X to C02XY.
Revision 2008/01/23	Present the Mechanical Details by JEDEC formation.
Revision 2008/09/29	Add the marking code for Green part.