OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

TC74AC373P/F/FW NON-INVERTING
TC74AC533P/F/FW INVERTING

The TC74AC373 and TC74AC533 are advanced high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

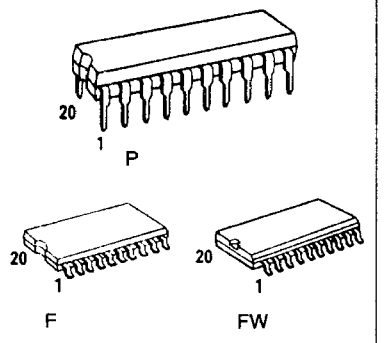
They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74AC373 has non-inverting outputs, and TC74AC533 has inverting outputs.

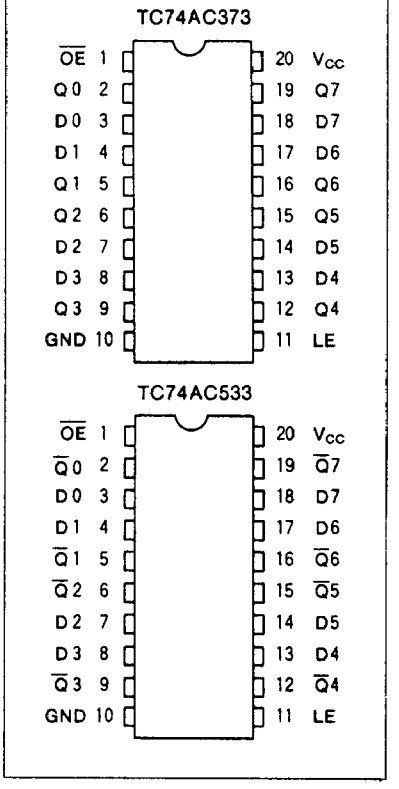
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



FEATURES:

- High Speed ..... t_{pd}=4.8 ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8 μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 373/533

PIN ASSIGNMENT (TOP VIEW)



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q(373)	$\overline{Q}$(533)
H	X	X	Z	Z
L	L	X	Q_n	$\overline{Q_n}$
L	H	L	L	H
L	H	H	H	L

X : Don't Care
Z : High Impedance
Q_n ($\overline{Q_n}$) : Q ($\overline{Q}$) outputs are latched at the time when the LE input is taken to a low logic level.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~7.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

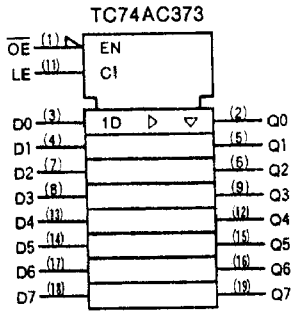
DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
3−State Output Off−State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	−	−	8.0	−	80.0	

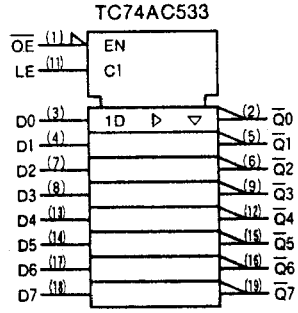
* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

IEC LOGIC SYMBOL

TC74AC373

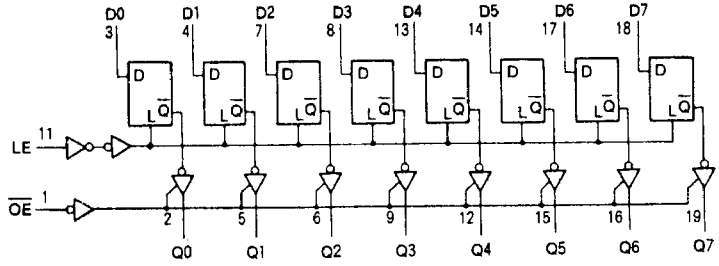


TC74AC533

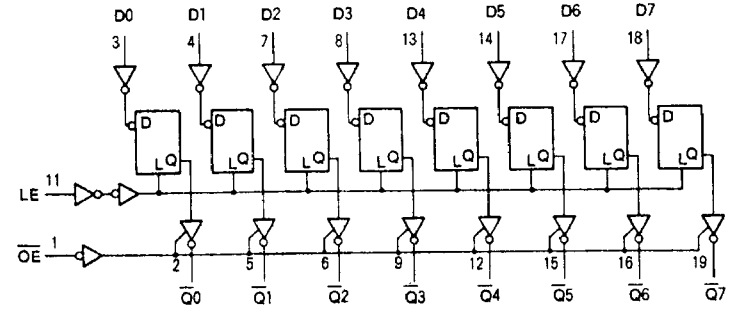


SYSTEM DIAGRAM

TC74AC373



TC74AC533



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40-85℃ LIMIT	UNIT
Minimum Pulse Width (LE)	$t_{W(H)}$		3.3±0.3	−	7.0	7.0	ns
			5.0±0.5	−	5.0	5.0	
Minimum Set−up Time	t_s		3.3±0.3	−	6.0	6.0	
			5.0±0.5	−	3.5	3.5	
Minimum Hold Time	t_h		3.3±0.3	−	1.0	1.0	
			5.0±0.5	−	1.0	1.0	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Propagation Delay Time (LE−Q, $\overline{Q}$)	t_{pLH}		3.3±0.3	−	7.7	13.2	1.0	15.0	ns
	t_{pHL}		5.0±0.5	−	6.1	8.7	1.0	10.0	
Propagation Delay Time (Dn−Q, $\overline{Q}$)	t_{pLH}		3.3±0.3	−	7.6	12.9	1.0	14.7	
	t_{pHL}		5.0±0.5	−	5.8	8.3	1.0	9.5	
Output Enable Time	t_{pZL}		3.3±0.3	−	7.6	12.9	1.0	14.7	
	t_{pZH}		5.0±0.5	−	6.1	8.7	1.0	10.0	
Output Disable Time	t_{pLZ}		3.3±0.3	−	7.0	11.0	1.0	12.5	
	t_{pHZ}		5.0±0.5	−	5.4	7.5	1.0	8.5	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)			−	26	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/8(\text{per Latch})$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

$$C_{PD}(\text{total})=26+12 \cdot n$$