Octal D-type flip-flop | 74ALS273

FEATURES

- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous master reset
- See 74ALS377 for clock enable version
- See 74ALS373 for transparent latch version
- See 74ALS374 for 3-State version

DESCRIPTION

The 74ALS273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) and master reset ($\overline{MR}$) inputs load and reset all flip-flops simultaneously.

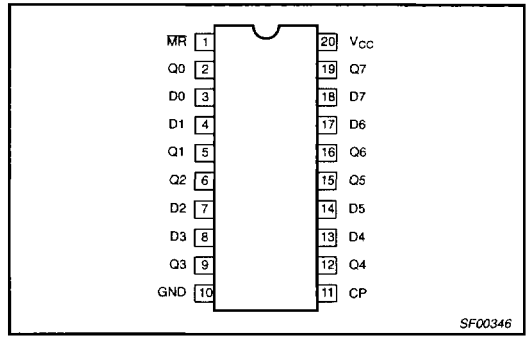
The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independently of clock or data inputs by a Low voltage level on the $\overline{MR}$ input.

The device is useful for applications where the true output only is required and the CP and $\overline{MR}$ are common to all flip-flops.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS273	95MHz	16mA

PIN CONFIGURATION



ORDERING INFORMATION

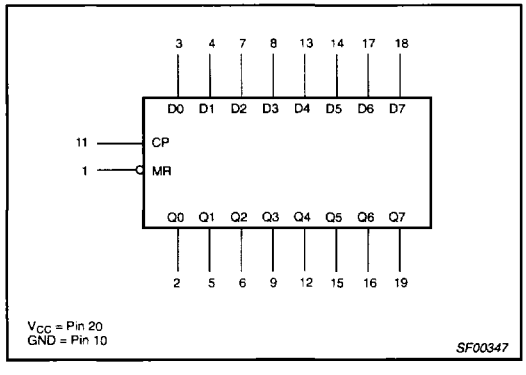
DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
20-pin plastic DIP	74ALS273N	SOT146-1
20-pin plastic SO	74ALS273D	SOT163-1
20-pin plastic SSOP Type II	74ALS273DB	SOT339-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

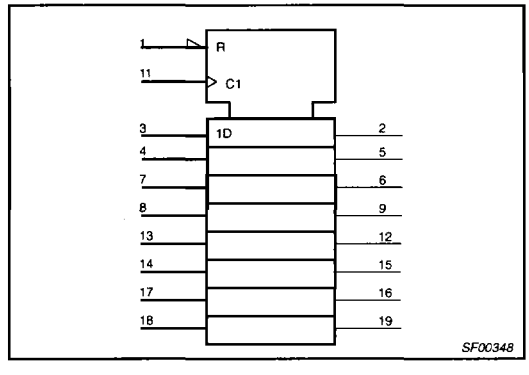
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D7	Data inputs	1.0/2.0	20µA/0.2mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20µA/0.1mA
$\overline{MR}$	Master Reset input (active-Low)	1.0/1.0	20µA/0.1mA
Q0 – Q7	3-State outputs	130/240	2.6mA/24mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

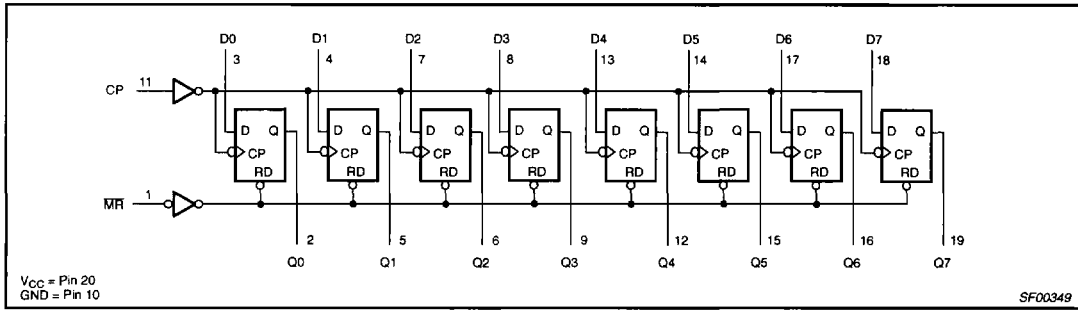
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{MR}$	CP	Dn	Qn	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"

H = High-voltage level
h = High state must be present one setup time before the Low-to-High clock transition
L = Low-voltage level
l = Low state must be present one setup time before the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−2.6	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –0.4mA	V_{CC} – 2			V
				I_{OH} = MAX	2.4	3.2		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
				I_{OL} = 24mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	$\overline{MR}$, CP	V_{CC} = MAX, V_I = 0.4V				–0.1	mA
		Dn					–0.2	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			12	18	mA
		I_{CCL}				21	29	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

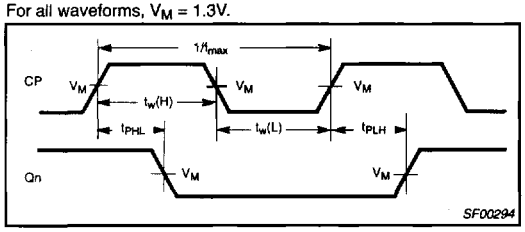
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	65		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	Waveform 1	2.0 3.0	8.0 11.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	Waveform 2	4.0	12.0	ns

AC SETUP REQUIREMENTS

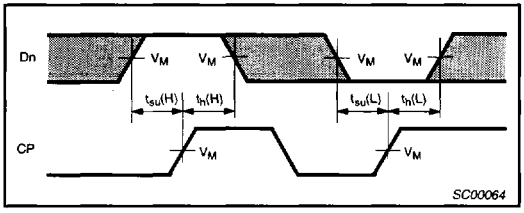
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, High or Low Dn to CP	Waveform 3	5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	Waveform 3	0.0 0.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low	Waveform 1	6.0 8.0		ns
$t_w(L)$	$\overline{MR}$ pulse width, Low	Waveform 2	7.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 2	12.0		ns

AC WAVEFORMS

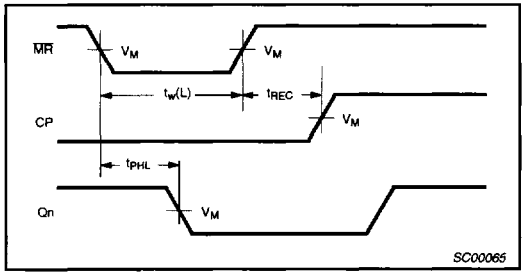
For all waveforms, V_M = 1.3V.



Waveform 1. Propagation Delay for Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

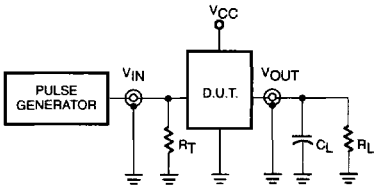


Waveform 3. Data Setup and Hold Times

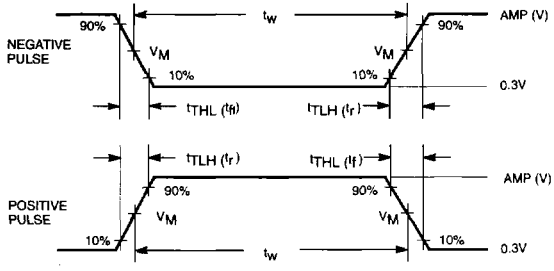


Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

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