National Semiconductor

November 1995

74VHC240 • 74VHCT240
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'VHC240 is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The 'VHC240 is an inverting TRI-STATE buffer having two active-low output enables. These devices are designed to drive buslines or buffer memory address registers.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High noise immunity: $V_{NIH} = V_{NIL} = 28\%\ V_{CC}$ (min)
- Power down protection: inputs only
- Low noise: $V_{OLP} = 0.9V$ (max)
- Low power dissipation: $I_{CC} = 4\ \mu A$ (max) @ $T_A = 25°C$
- Balanced propagation delays: $t_{PLH} \cong t_{PHL}$
- Pin and function compatible with 74HC/HCT240

THE 74VHCT240 IS ADVANCE INFORMATION ONLY

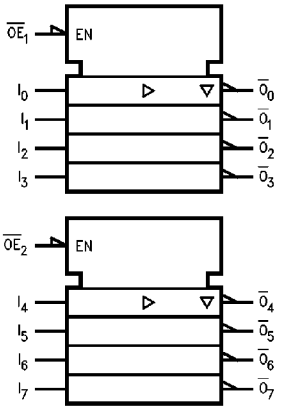
NOTE: ADD EXTERNAL PULL UP RESISTOR TO VHCT OUTPUTS TO DRIVE CMOS INPUTS

Commercial	Package Number	Package Description
74VHC240M	M20B	20-Lead Molded JEDEC SOIC
74VHC240SJ	M20D	20-Lead Molded EIAJ SOIC
74VHC240MSC	MSC20	20-Lead Molded EIAJ Type 1 SSOP
74VHC240MTC	MTC20	20-Lead Molded JEDEC Type 1 TSSOP
74VHC240N	N20A	20-Lead Molded DIP

Note: Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code. EIAJ Type 1 SSOP available on tape and reel only, order MSCX.

Logic Symbol

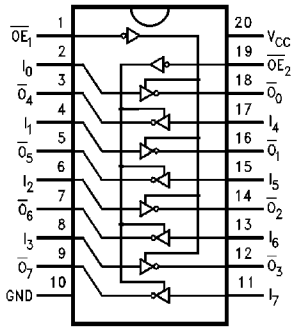
IEEE/IEC



TL/F/11506–1

Connection Diagram

Pin Assignment for DIP, SSOP, TSSOP and SOIC



TL/F/11506–2

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_1$	I_n	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs TRI-STATE Outputs

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	
VHC	−0.5V to V_{CC} + 0.5V
VHCT*	−0.5V to +7.0V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	
VHC	±20 mA
VHCT	−20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

*V_{OUT} > V_{CC} only if output is in H or Z state.

Note 1: *Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
VHC	2.0V to 5.5V
VHCT	4.5V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	
74VHC/VHCT	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ±0.3V (VHC Only)	0 ns/V ~ 100 ns/V
V_{CC} = 5.0V ±0.5V	0 ns/V ~ 20 ns/V

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC T_A = 25°C			74VHC T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0	1.50			1.50		V		
		3.0–5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	Low Level Input Voltage	2.0			0.50		0.50	V		
		3.0–5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		I_{OH} = −4 mA
		4.5	3.94			3.80				I_{OH} = −8 mA
V_{OL}	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		I_{OL} = 4 mA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{OZ}	TRI-STATE Output Off-State Current	5.5			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL}; V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$ Typ	74VHC $T_A = 25°C$ Limits	Units	Conditions
**V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	0.6	0.9	V	C_L = 50 pF
**V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−0.9	V	C_L = 50 pF
**V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0		3.5	V	C_L = 50 pF
**V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0		1.5	V	C_L = 50 pF

**Parameter guaranteed by design.

DC Characteristics for 'VHCT Family Devices (Preliminary)

Symbol	Parameter	V_{CC} (V)	74VHCT $T_A = 25°C$ Min	Typ	Max	54VHCT $T_A = -40°C$ to $+85°C$ Min	Max	Units	Conditions	
V_{IH}	High Level Input Voltage	4.5 5.5	2.0 2.0			2.0 2.0		V		
V_{IL}	Low Level Input Voltage	4.5 5.5			0.8 0.8		0.8 0.8	V		
V_{OH}	High Level Output Voltage	4.5	3.15	3.65		3.15		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		4.5	2.5			2.4				I_{OH} = −8 mA
V_{OL}	Low Level Output Voltage	4.5		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{OZ}	TRI-STATE Output Off-State Current	5.5			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	μA	V_{IN} = V_{CC} or GND	
I_{CCT}	Maximum I_{CC}/Input	5.5			1.35		1.50	mA	V_{IN} = 3.4V, Other Inputs = V_{CC} or GND	
I_{OPD}	Output Leakage (Power Down State)	0.0			+0.5		+5.0	μA	V_{OUT} = 5.5V	

DC Characteristics for 'VHCT Family (Preliminary) :

Symbol	Parameter	V_{CC} (V)	74VHCT $T_A = 25°C$ Typ	74VHCT $T_A = 25°C$ Limits	Units	Conditions
V_{OLP}**	Quiet Output Maximum Dynamic V_{OL}		0.7	1.0	V	$C_L = 50$ pF
V_{OLV}**	Quiet Output Minimum Dynamic V_{OL}		−0.7	−1.0	V	$C_L = 50$ pF
V_{IHD}**	Minimum High Level Dynamic Input Voltage			2.0	V	$C_L = 50$ pF
V_{ILD}**	Maximum High Level Dynamic Input Voltage			0.8	V	$C_L = 50$ pF

**Parameter guaranteed by design.

AC Electrical Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$ Min	Typ	Max	74VHC $T_A = -40°C$ to $+85°C$ Min	Max	Units	Conditions	
t_{PLH} t_{PHL}	Propagation Delay Time	3.3 ±0.3		5.3	7.5	1.0	9.0	ns		$C_L = 15$ pF
				7.8	11.0	1.0	12.5			$C_L = 50$ pF
		5.0 ±0.5		3.6	5.5	1.0	6.5	ns		$C_L = 15$ pF
				5.1	7.5	1.0	8.5			$C_L = 50$ pF
t_{PZL} t_{PZH}	TRI-STATE Output Enable Time	3.3 ±0.3		6.6	10.6	1.0	12.5	ns	$R_L = 1$ kΩ	$C_L = 15$ pF
				9.1	14.1	1.0	16.0			$C_L = 50$ pF
		5.0 ±0.5		4.7	7.3	1.0	8.5	ns		$C_L = 15$ pF
				6.2	9.3	1.0	10.5			$C_L = 50$ pF
t_{PLZ} t_{PHZ}	TRI-STATE Output Disable Time	3.3 ±0.3		10.3	14.0	1.0	16.0	ns	$R_L = 1$ kΩ	$C_L = 50$ pF
		5.0 ±0.5		6.7	9.2	1.0	10.5			$C_L = 50$ pF
t_{OSLH} t_{OSHL}	Output to Output Skew	3.3 ±0.3			1.5		1.5	ns	(Note 1)	$C_L = 50$ pF
		5.0 ±0.5			1.0		1.0			$C_L = 50$ pF
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open	
C_{OUT}	Output Capacitance			6				pF	$V_{CC} = 5.0$V	
C_{PD}	Power Dissipation Capacitance			17				pF	(Note 2)	

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHmax} - t_{PLHmin}|$; $t_{OSHL} = |t_{PHLmax} - t_{PHLmin}|$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = $C_{PD} * V_{CC} * f_{IN} + I_{CC}/8$ (per bit).

AC Electrical Characteristics for 'VHCT (Preliminary)

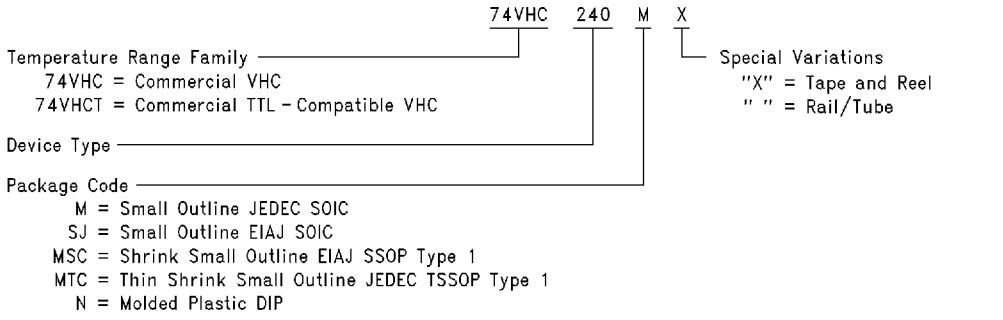
Symbol	Parameter	V_{CC} (V)	74VHCT $T_A = 25°C$			74VHCT $T_A = -40°C$ to $+85°C$		Units	Conditions	
			Min	Typ	Max	Min	Max			
t_{PLH}, t_{PHL}	Propagation Delay Time	5.0 ±0.5		5.4	7.4	1.0	8.5	ns		C_L = 15 pF
				5.9	8.4	1.0	9.5			C_L = 50 pF
t_{PZL}, t_{PZH}	TRI-STATE Output Enable Time	5.0 ±0.5		7.7	10.4	1.0	12.0	ns	R_L = 1 kΩ	C_L = 15 pF
				8.2	11.4	1.0	13.0			C_L = 50 pF
t_{PLZ}, t_{PHZ}	TRI-STATE Output Disable Time	5.0 ±0.5		8.8	11.4	1.0	13.0	ns	R_L = 1 kΩ	C_L = 50 pF
t_{OSLH}, t_{OSHL}	Output to Output Skew	5.0 ±0.5			1.0		1.0	ns	(Note 1)	C_L = 50 pF
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open	
C_{OUT}	Output Capacitance			9				pF	V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance			18				pF	(Note 2)	

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHmax} - t_{PLHmin}|$; $t_{OSHL} = |t_{PHLmax} - t_{PHLmin}|$.

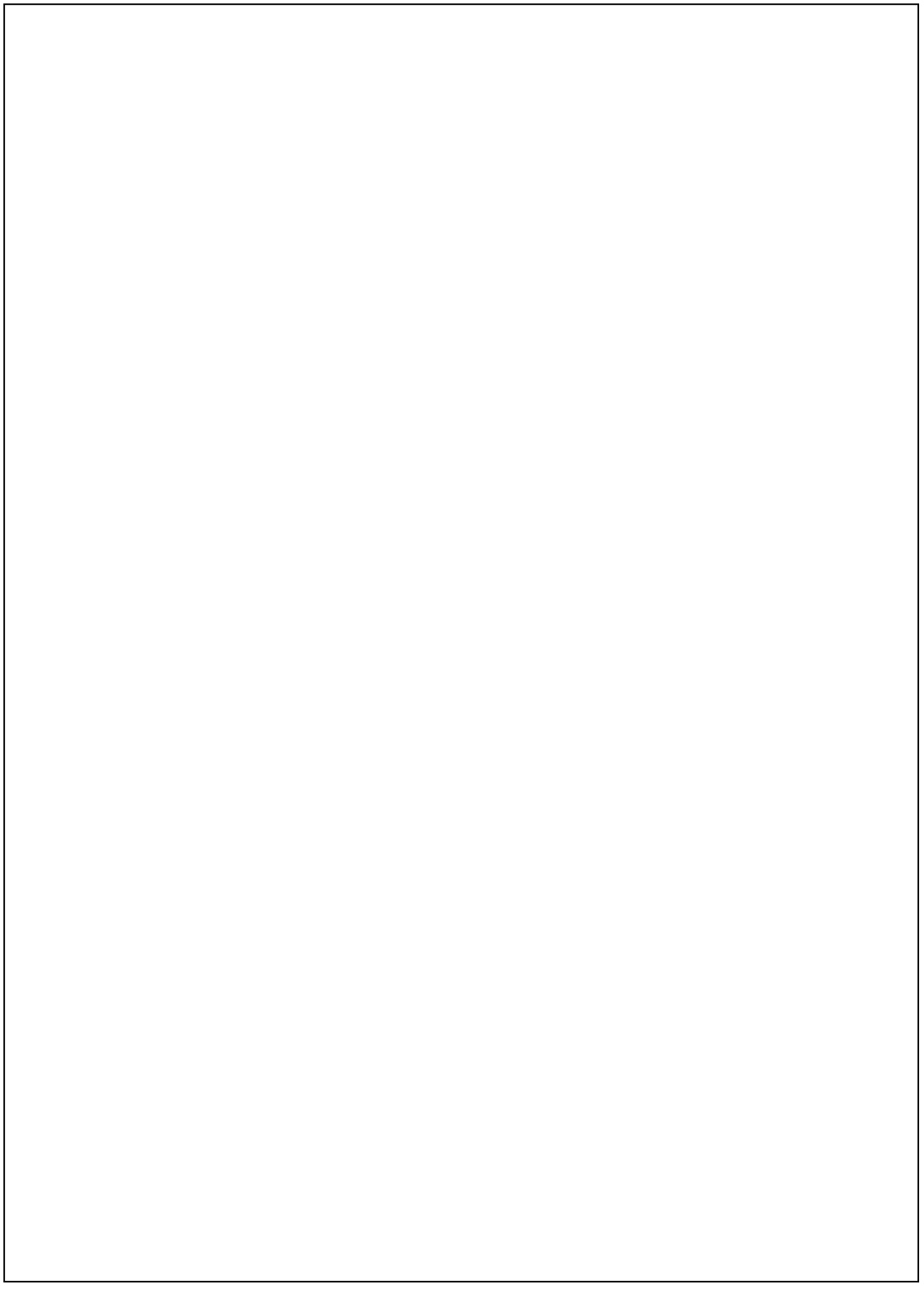
Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (OPR.) = C_{PD} * V_{CC} * f_{IN} + I_{CC}/8 (per bit).

Ordering Information

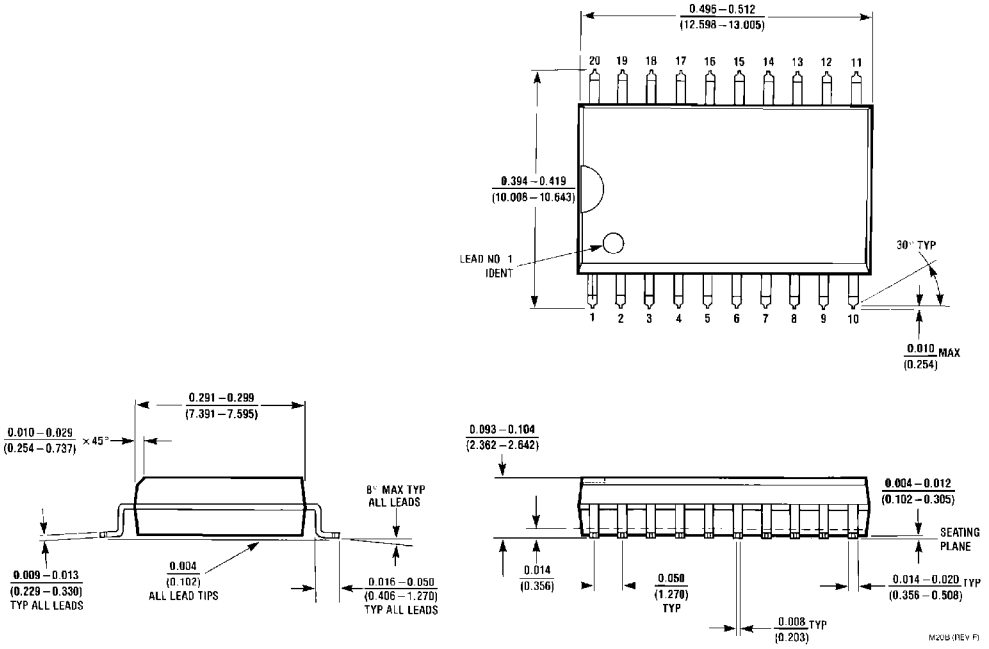
The device number is used to form part of a simplified purchasing code, where the package type and temperature range are defined as follows:



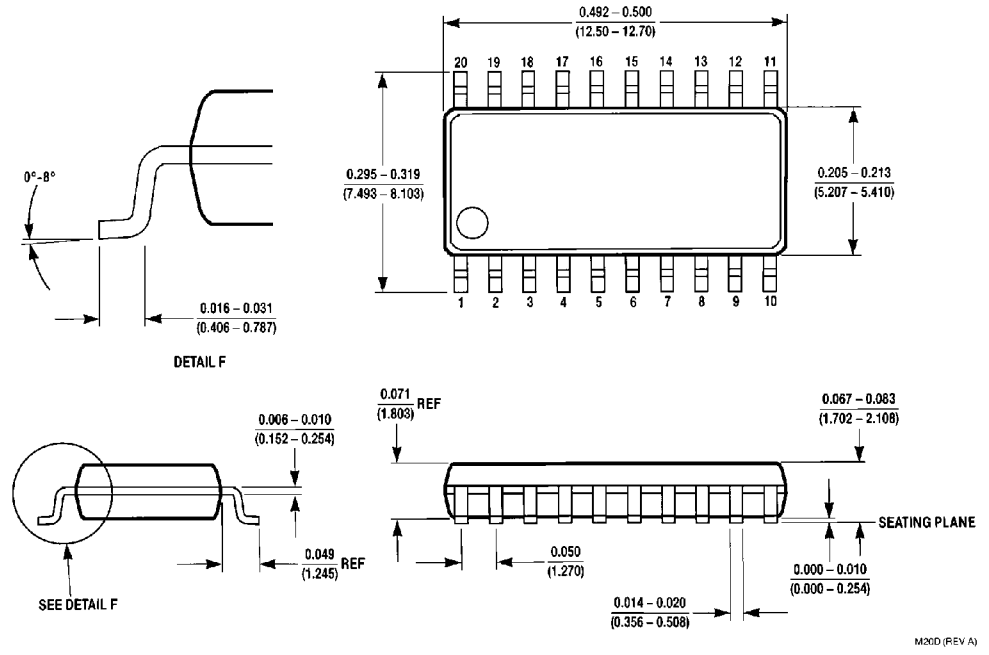
TL/F/11506–4



Physical Dimensions inches (millimeters)

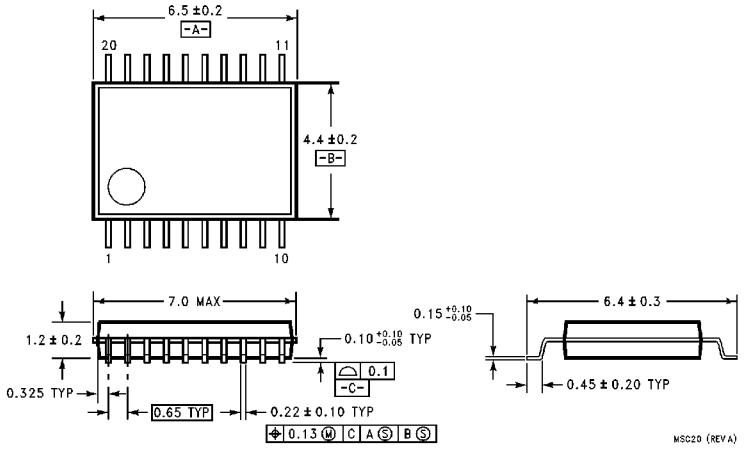


20-Lead Small Outline Integrated Circuit—JEDEC SOIC (M)
Order Number 74VHC240M or 74VHC240MX
NS Package Number M20B

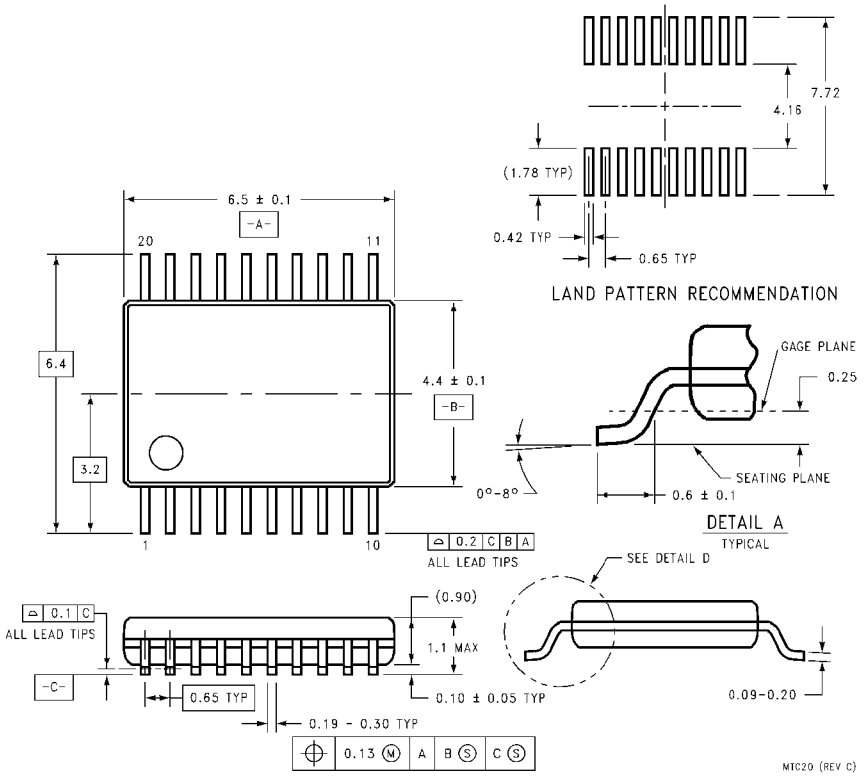


20-Lead Plastic EIAJ SOIC (SJ)
Order Number 74VHC240SJ or 74VHC240SJX
NS Package Number M20D

Physical Dimensions (millimeters) (Continued)

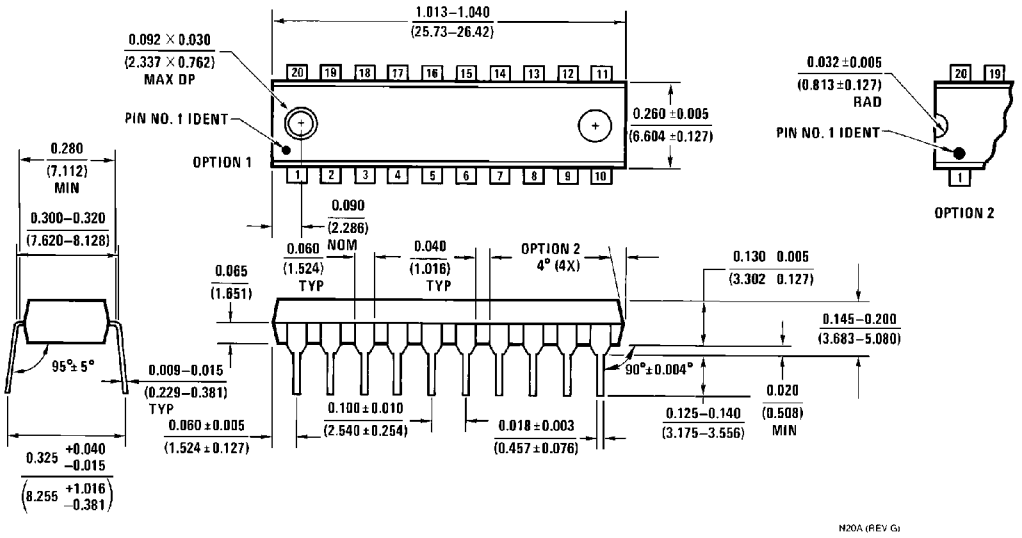


20-Lead Plastic EIAJ SSOP Type I (MSC)
Order Number 74VHC240MSCX
NS Package Number MSC20



20-Lead Plastic JEDEC TSSOP Type I (MTC)
Order Number 74VHC240MTC or 74VHC240MTCX
NS Package Number MTC20

Physical Dimensions inches (millimeters) (Continued)



20-Lead Molded DIP
Order Number 74VHC240N
NS Package Number N20A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408