Signetics

74LS257A, S257
Data Selectors/Multiplexers

Quad 2-Line To 1-Line Data Selector/Multiplexer (3-State)
Product Specification

Logic Products

FEATURES
- **Multifunction capability**
- **Non-inverting data path**
- **3-State outputs**

DESCRIPTION
The '257 has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Data Select input (S). The I_0 inputs are selected when the Select input is LOW and the I_1 inputs are selected when the Select input is HIGH. Data appears at the outputs in true (non-inverted) form from the selected outputs.

The '257 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS257A	13ns	9mA
74S257	6.6ns	56mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74S257N, N74S257AN
Plastic SO-16	N74S257D
Plastic SOL-16	CD7193D
Plastic SOL-16	N74LS257D

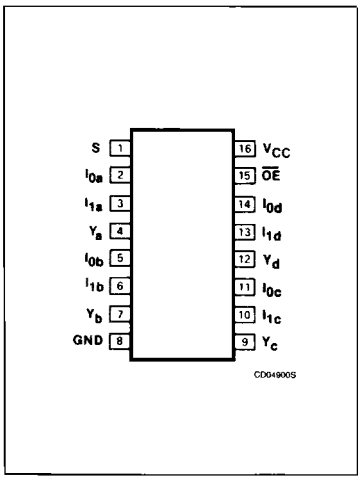
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

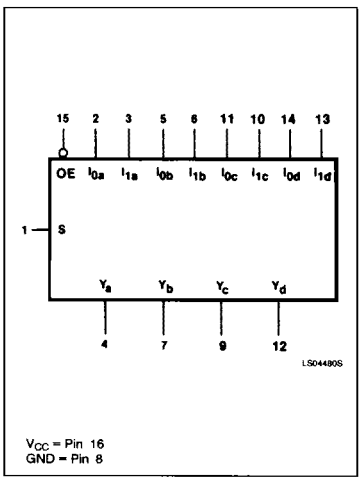
PINS	DESCRIPTION	74	74S
S	Inputs	2Sul	2LSul
Other	Inputs	1Sul	1LSul
All	Outputs	10Sul	30LSul

NOTE:
A 74S unit load (Sul) is understood to be 50μA I_{IH} and −2.0mA I_{IL}, and a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

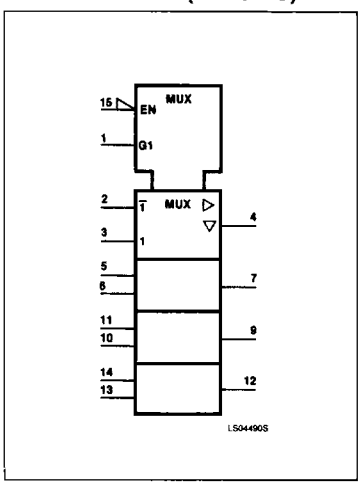
PIN CONFIGURATION



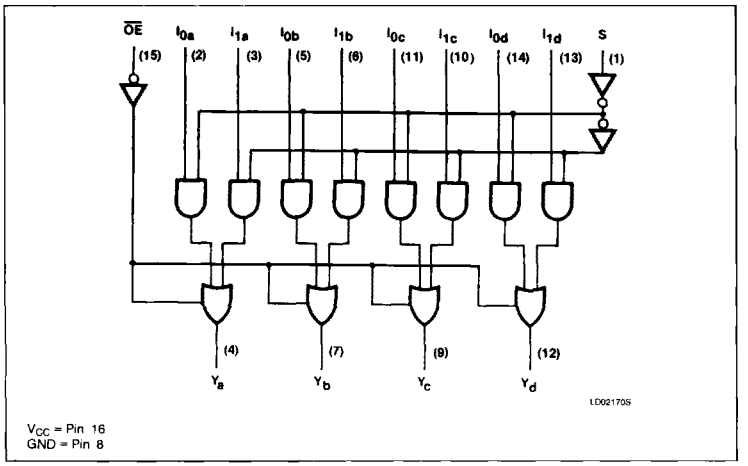
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



Outputs are forced to a HIGH impedance "off" state when the Output Enable input ($\overline{OE}$) is HIGH. All but one device must be in the HIGH impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the output enable signals must ensure that there is no overlap when outputs of 3-state devices are tied together.

FUNCTION TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{OE}$	S	I_0	I_1	Y
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			74S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	HIGH-level output current			−2.6			−6.5	mA
I_{OL}	LOW-level output current			24			20	mA
T_A	Operating free-air temperature	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

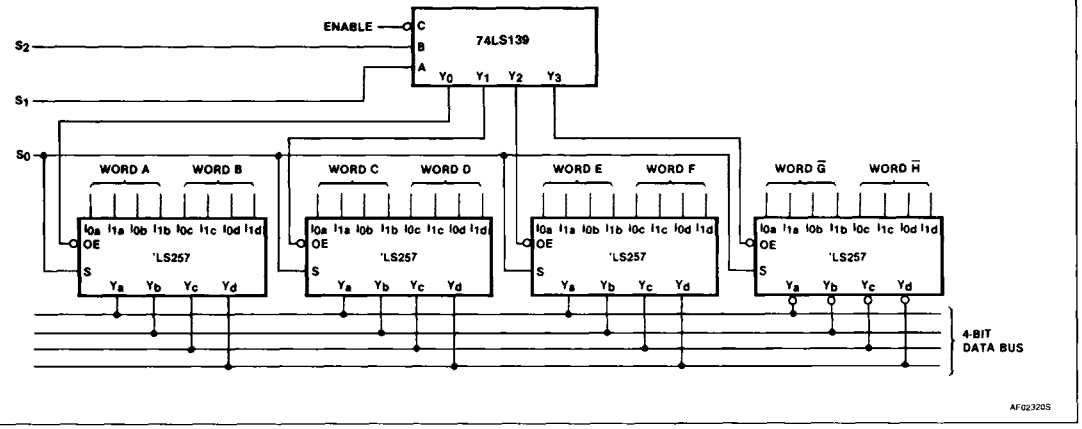
PARAMETER		TEST CONDITIONS[1]		74LS257A			74S257			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = MAX	2.4	3.1		2.4	3.2		V
			I_{OH} = −1mA (74S)				2.7			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX		0.35	0.5			0.5	V
			I_{OL} = 12mA (74LS)		0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5			−1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 2.7V			20				μA
			V_O = 2.4V						50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 0.4V			−20				μA
			V_O = 0.5V						−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V						1.0	mA
			V_I = 7.0V, S input			0.2				mA
			V_I = 7.0V, Other inputs			0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.7V, S input			40			100	μA
			V_I = 2.7V, Other inputs			20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V, S input			−0.8				mA
			V_I = 0.4V, Other inputs			−0.4				mA
			V_I = 0.5V, S input						−4	mA
			V_I = 0.5V, Other inputs						−2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−30		−130	−40		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		6.2	10		44	68	mA
			I_{CCL} Outputs LOW		10	16		60	93	mA
			I_{CCZ} Outputs OFF		12	19		64	99	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all outputs open and all possible inputs grounded while achieving the stated output conditions.

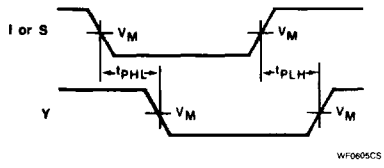
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	74LS C_L = 45pF, R_L = 667Ω		74S C_L = 15pF, R_L = 280Ω		UNIT
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		18 18		7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1		21 21		15 15	ns
t_{PZH}	Output enable to HIGH level	Waveform 2		30		19.5	ns
t_{PZL}	Output enable to LOW level	Waveform 3		30		21	ns
t_{PHZ}	Output disable from HIGH level	Waveform 2, C_L = 5pF		30		8.5	ns
t_{PLZ}	Output disable from LOW level	Waveform 3, C_L = 5pF		25		14	ns

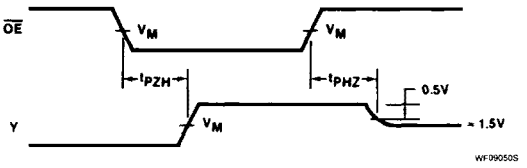
APPLICATION DIAGRAM



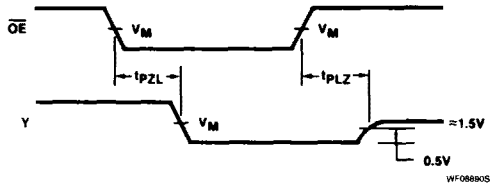
AC WAVEFORMS



Waveform 1. Propagation Delay Data And Select To Output



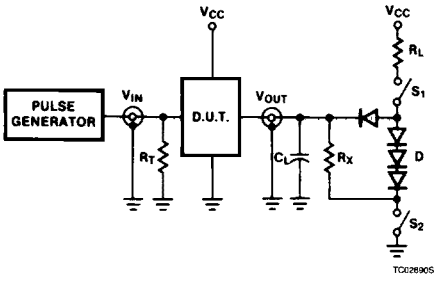
Waveform 2. 3-State Enable Time To High Level And Disable Time From High Level



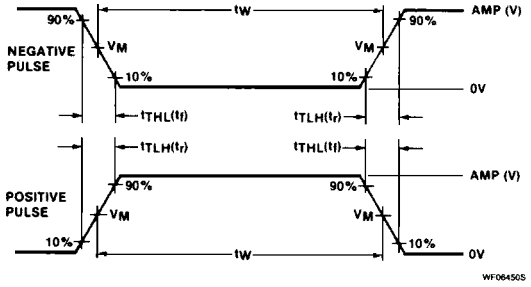
For all waveforms, V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Waveform 3. 3-State Enable Time To Low Level And Disable Time From Low Level

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

R_X = 1kΩ for 74, 74S, R_X = 5kΩ for 74LS.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

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