

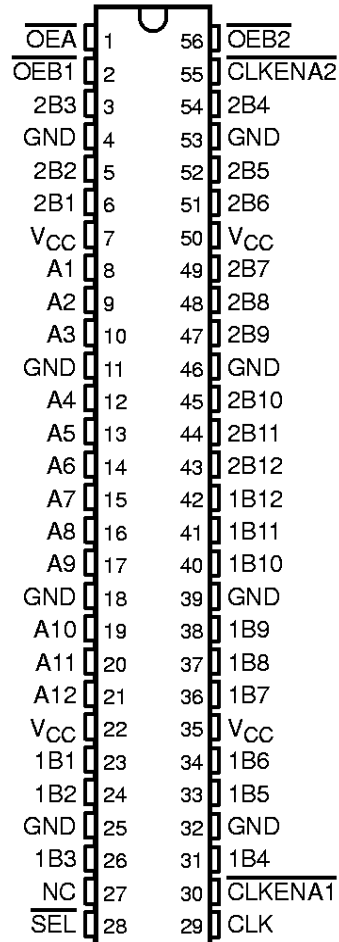
SN74ALVCHR162269A

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES050G – AUGUST 1995 – REVISED JANUARY 1998

- Member of the Texas Instruments *Widebus*™ Family
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- All Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



NC – No internal connection

description

This 12-bit to 24-bit registered bus exchanger is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCHR162269A is used in applications in which two separate ports must be multiplexed onto, or demultiplexed from, a single port. It is particularly suitable as an interface between synchronous DRAMs and high-speed microprocessors.

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable (\overline{CLKENA}) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. For data transfer in the B-to-A direction, a single storage register is provided. The select (\overline{SEL}) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period during which the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables (\overline{OEA} , $\overline{OEB1}$, and $\overline{OEB2}$).

To ensure the high-impedance state during power up or power down, a clock pulse should be applied as soon as possible and \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Due to \overline{OE} being routed through a register, the active state of the outputs cannot be determined prior to the arrival of the first clock pulse.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.



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description (continued)

All outputs are designed to sink up to 12 mA and include equivalent 26-Ω resistors to reduce overshoot and undershoot.

The SN74ALVCHR162269A is characterized for operation from –40°C to 85°C.

Function Tables

OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	\overline{OEA}	\overline{OEB}	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE ($\overline{OEB} = L$)

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
L	H	↑	L	L	2B ₀ †
L	H	↑	H	H	2B ₀ †
L	L	↑	L	L	L
L	L	↑	H	H	H
H	L	↑	L	1B ₀ †	L
H	L	↑	H	1B ₀ †	H
H	H	X	X	1B ₀ †	2B ₀ †

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OEA} = L$)

INPUTS				OUTPUT
CLK	\overline{SEL}	1B	2B	A
X	H	X	X	A ₀ †
X	L	X	X	A ₀ †
↑	H	L	X	L
↑	H	H	X	H
↑	L	X	L	L
↑	L	X	H	H

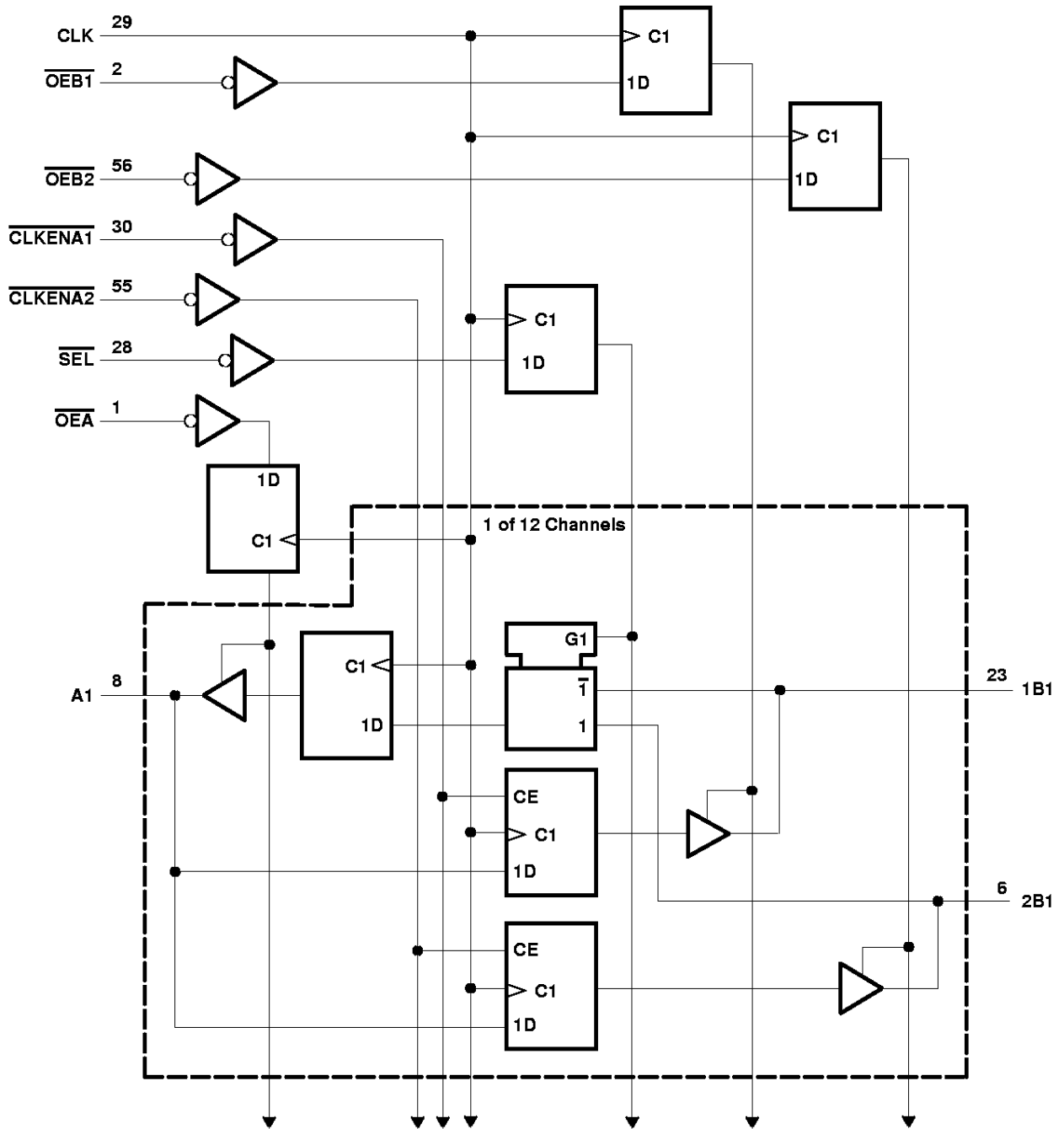
† Output level before the indicated steady-state input conditions were established



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logic diagram (positive logic)



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}	I _{OH} = -100 μA	2.3 V to 3.6 V	V _{CC} -0.2			V
	I _{OH} = -4 mA	V _{IH} = 1.7 V	2.3 V	1.9		
		V _{IH} = 2 V	2.7 V	2.2		
	I _{OH} = -6 mA	V _{IH} = 1.7 V	2.3 V	1.7		
		V _{IH} = 2 V	3 V	2.4		
	I _{OH} = -8 mA,	V _{IH} = 2 V	2.7 V	2		
I _{OH} = -12 mA,	V _{IH} = 2 V	3 V	2			
V _{OL}	I _{OL} = 100 μA	2.3 V to 3.6 V			0.2	V
	I _{OL} = 4 mA	V _{IL} = 0.7 V	2.3 V		0.4	
		V _{IL} = 0.8 V	2.7 V		0.4	
	I _{OL} = 6 mA	V _{IL} = 0.7 V	2.3 V		0.55	
		V _{IL} = 0.8 V	3 V		0.55	
	I _{OL} = 8 mA,	V _{IL} = 0.8 V	2.7 V		0.6	
I _{OL} = 12 mA,	V _{IL} = 0.8 V	3 V		0.8		
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _I (hold)	V _I = 0.7 V	2.3 V	45		μA	
	V _I = 1.7 V		-45			
	V _I = 0.8 V	3 V	75			
	V _I = 2 V		-75			
	V _I = 0 to 3.6 V‡	3.6 V	±500			
I _{OZ} §	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			40	μA
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	5		pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V	8.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.

§ For I/O ports, the parameter I_{OZ} includes the input leakage current.



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f_{clock}	Clock frequency	95		115		135		135		MHz	
t_w	Pulse duration, CLK high or low	5.2		4.3		3.3		3.3		ns	
t_{su}	Setup time	A data before CLK \uparrow		1.4		1.4		0.9		1	
		B data before CLK \uparrow		1.6		1.5		1		1.1	
		$\overline{\text{SEL}}$ before CLK \uparrow		0.8		1.1		1.3		1.3	
		$\overline{\text{CLKENA1}}$ or $\overline{\text{CLKENA2}}$ before CLK \uparrow		0.8		1		0.7		0.8	
		$\overline{\text{OE}}$ before CLK \uparrow		1.7		1.6		1.1		1.2	
t_{h}	Hold time	A data after CLK \uparrow		0.9		0.9		1.1		1.2	
		B data after CLK \uparrow		0.8		0.6		0.8		1	
		$\overline{\text{SEL}}$ after CLK \uparrow		1.1		0.8		1.6		1.7	
		$\overline{\text{CLKENA1}}$ or $\overline{\text{CLKENA2}}$ after CLK \uparrow		1.4		1		1.4		1.6	
		$\overline{\text{OE}}$ after CLK \uparrow		0.9		0.8		1		1.2	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			95		115		135		135		MHz
t_{pd}	CLK	B	1.8	7.1	6.9		2.3	5.6	2.2	5.8	ns
		A	1.4	5.8	5.8		2	5	2	5.2	
t_{en}	CLK	B	2.4	7.2	6.9		2.3	5.6	2.3	5.8	ns
		A	2.1	6.2	6		2.1	5.2	2.1	5.3	
t_{dis}	CLK	B	2.6	7.9	6.7		2.3	5.8	2.4	6	ns
		A	2	7.8	6.2		2.2	5.9	2.1	6	

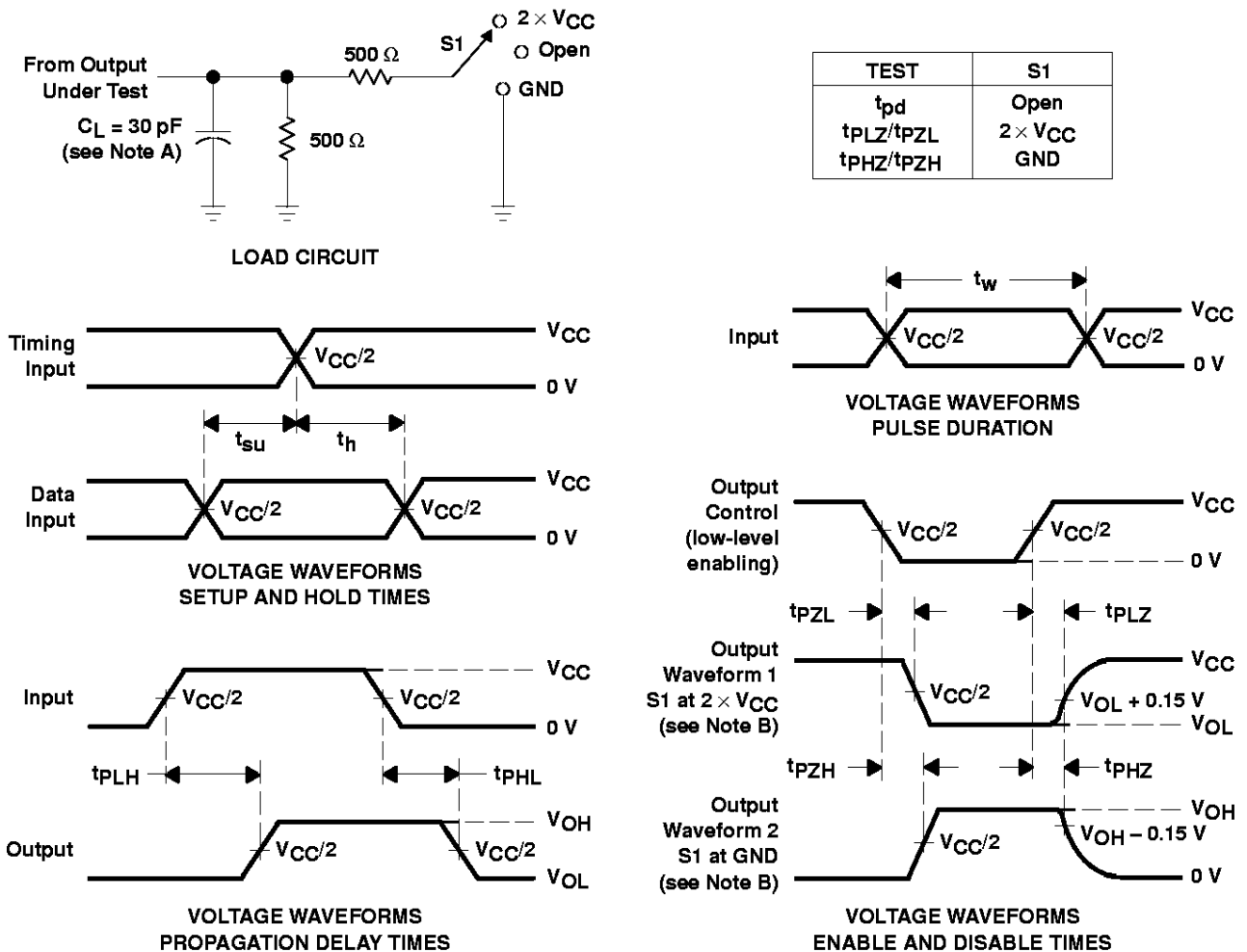
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.15\text{ V}$		UNIT
			TYP		TYP		
C_{pd}	Power dissipation capacitance per exchanger	All outputs enabled	142		172		pF
		All outputs disabled	115		129		



PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

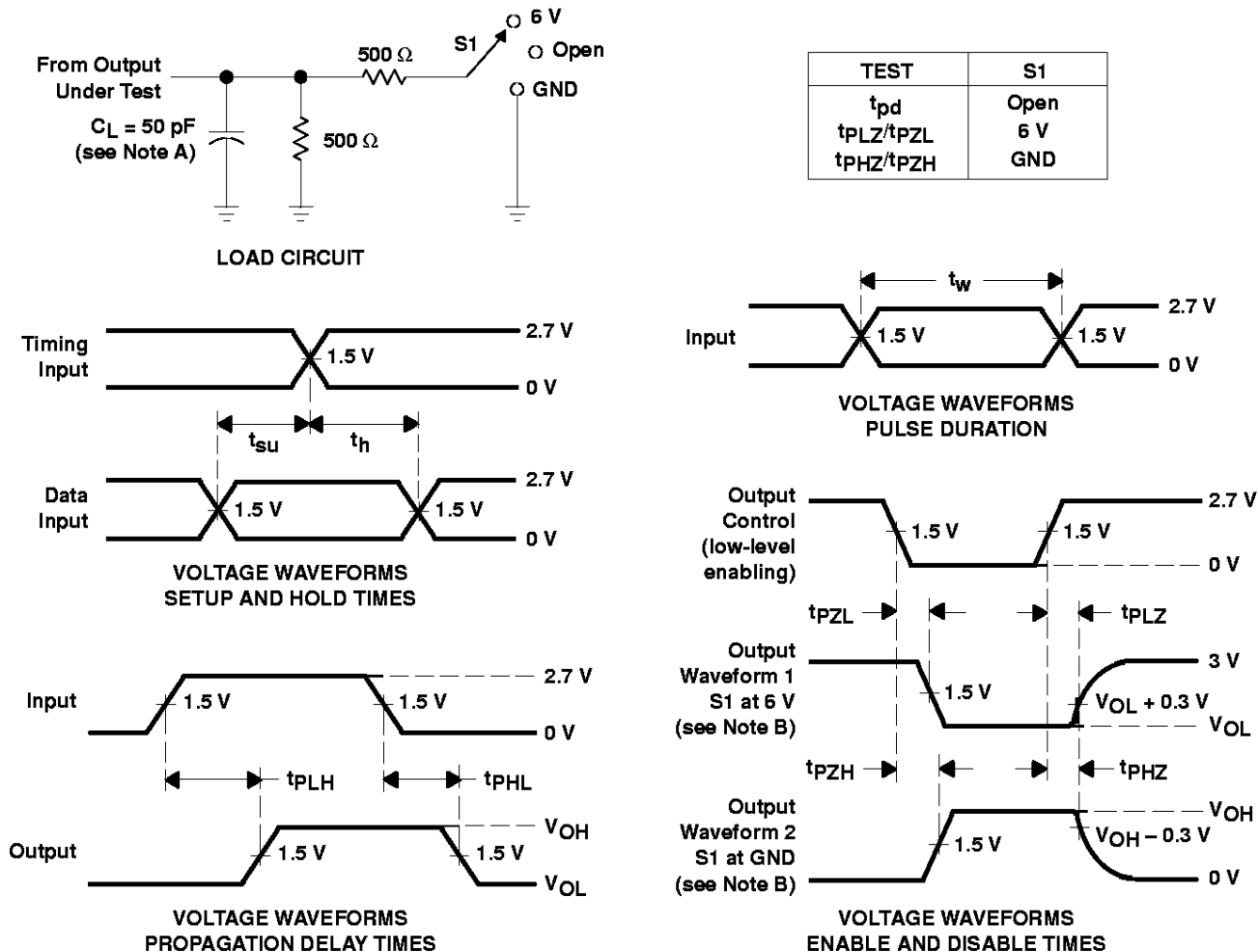
Figure 1. Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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